US Micro Products
ENGINEERED DISPLAY SOLUTIONS

TFT IPS SPECIFICATION

Part Number	USMP-TT024Q-01K
Size	2.4"
Resolution	240 X 320
Brightness	200
Contrast	500
Viewing Angle	80/80/80/80
Operating Temp.	-20 to 70°C

TFT IPS Benefits:

- High Brightness
- Great viewing angles
- Low profile
- Great contrast
- Vivid colors

FOR ADDITIONAL INFORMATION PLEASE CONTACT:
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Issue Date	Approved by (customer use)	Checked by	Prepared by

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History of Version

Date (mm / dd / yyyy)	Ver.	Edi.	Description	Page	Design by
10/25/2012	01	001	New Drawing	-	Yuan
11/02/2012	01	002	Modify Optical Characteristics Modify Backlight & LED Characteristics Modify interface Modify FPC	6 9 12,13 Appendix	Yuan
11/19/2012	01	003	Modify Counter Drawing Modify interface Modify Timing Characteristics Modify FPC	10 11~14 16~20 Appendix	Yuan
01/07/2013	01	004	Modify interface Modify Drawing	11~14 Appendix	Yuan
12/18/2015	01	005	Modify Technology Description	4, 32 Appendix	Mihm

Contents

Note：For detailed information please refer to IC data sheet：ILITEK – ILI9341

1. SPECIFICATIONS

1.1 Features

Main LCD Panel

Item	Standard Value
Display Type	240 * (R、G、B) * 320 Dots
LCD Type	a-Si TFT IPS, Normally Black, Transmissive
Screen size(inch)	2.4 (Diagonal)
Color configuration	R.G.B. vertical stripe
Backlight	White LED
Interface	8 /9/16/18 Bit Interface for i80 system and serial /RGB interface
Driver IC	ILI9341
ROHS	THIS PRODUCT CONFORMS TO THE ROHS OF USMP Detailed information please to refer website : http://www.usmicroproducts.com

1.2 Mechanical Specifications

Item	Standard Value	Unit
Outline Dimension	41.87 (W) * 59.35 (L) * 2.6 (H)max	mm

LCD Panel

Item	Standard Value	Unit
Viewing Area	38.5 (W) * 50.96(L)	mm
Active Area	36.72(W) * 48.96(L)	mm

Note : For detailed information please refer to LCM drawing

1.3 Absolute Maximum Ratings

Module

Item	Symbol	Condition	Min.	Max.	Unit
System Power Supply Voltage	VDD	-	-0.3	4.6	V
	VGH-VGL	GND	0	+32	
Logic Input Voltage	VIN	-	-0.3	VDD+0.3	V
Operating Temperature	TOP	-	-20	70	°C
Storage Temperature	TST	-	-30	80	°C

1.4 DC Electrical Characteristics

Module GND = 0V, Ta = 25°C

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Power Supply Voltage	VDD	-	-	2.8	-	V
Input High Voltage	V_{IH}	-	0.7*VDD	-	VDD	V
Input Low Voltage	V_{IL}	-	GND	-	0.3*VDD	V
Output High Voltage	V_{OH}	IOH=-0.1mA	0.8*VDD	-	VDD	V
Output Low Voltage	V_{OL}	IOL=0.1mA	GND	-	0.2*VDD	V
Supply Current	IDD	VDD = 2.8V Pattern= Full display *1	-	(10)	(15)	mA

Note 1: Maximum current display

1.5 Optical Characteristics

TFT LCD panel VDD= 2.8 V, Ta=25°C

Item		Symbol	Condition	Min.	Typ.	Max.	unit	
Response time	Rise	Tr+Tf	Ta = 25°C θX, θY = 0°	-	(35)	-	ms	Note2
	Fall							
Viewing angle	Top	θY+	CR ≥ 10	-	(80)	-	Deg.	Note4
	Bottom	θY-		-	(80)	-		
	Left	θX-		-	(80)	-		
	Right	θX+		-	(80)	-		
Contrast ratio		CR	Ta = 25°C θX , θY = 0°	-	(500)	-	-	Note3
Color of CIE Coordinate (With B/L & T/P)	White	X	Ta = 25°C θX , θY = 0°	(0.286)	(0.306)	(0.326)	-	Note1
		Y		(0.298)	(0.318)	(0.338)		
	Red	X		(0.637)	(0.657)	(0.677)		
		Y		(0.306)	(0.326)	(0.346)		
	Green	X		(0.249)	(0.269)	(0.289)		
		Y		(0.569)	(0.589)	(0.609)		
	Blue	X		(0.129)	(0.149)	(0.169)		
		Y		(0.060)	(0.080)	(0.100)		
Average Brightness Pattern=white display (With B/L)		IV	IF=TBD mA	(180)	(200)	-	cd/m^2	Note1
Uniformity (With B/L)		△B	IF=TBD mA	80	-	-	%	Note1

Note1:

*1：△B=B(min) / B(max) * 100%

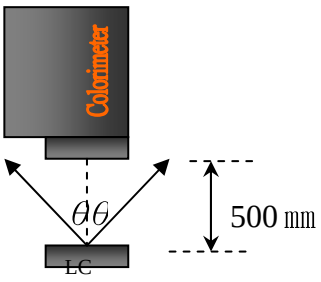
*2：Measurement Condition for Optical Characteristics:

a：Environment: 25℃±5℃ / 60±20%R.H，no wind，dark room below 10 Lux at typical lamp current and typical operating frequency.

b：Measurement Distance: 500 ± 50 ㎜ ，(θ= 0°)

c：Equipment: TOPCON BM-7 fast，(field 1°)，after 10 minutes operation.

d：The uncertainty of the C.I.E coordinate measurement ±0.01，Average Brightness ± 4%



Colorimeter=BM-7

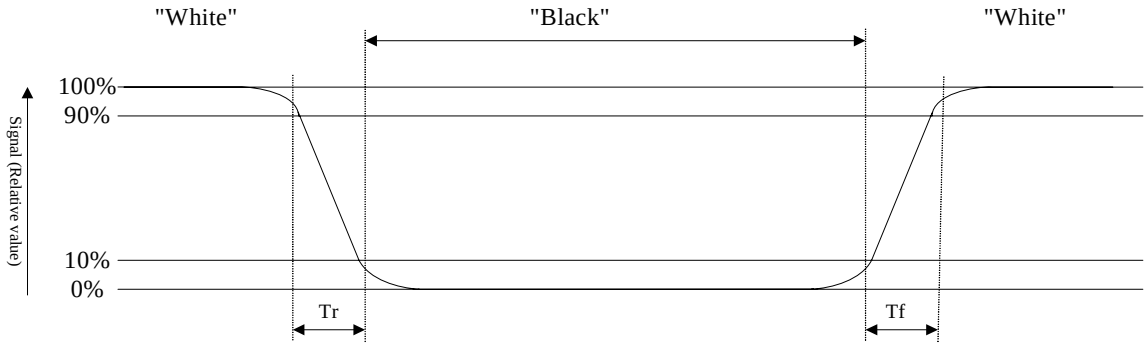
To be measured at the center area of panel with a viewing cone of 1? by Topcon luminance meter BM-7, after 10 minutes operation (module)

Note2: Definition of response time:

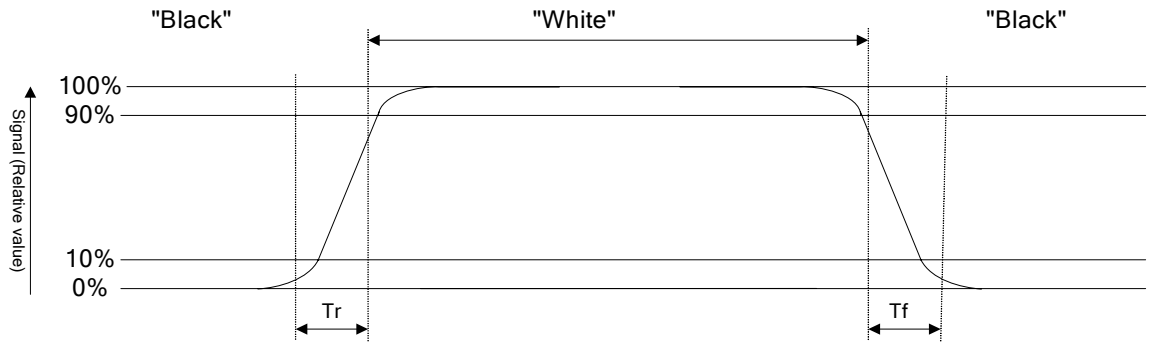
The output signals of photo detector are measured when the input signals are changed from “black” to “white”(falling time) and from “white” to “black”(rising time), respectively. The response time is defined as the time interval between the 10% and 90% of Amplitudes.

Refer to figure as below:

Normally White



Normally Black



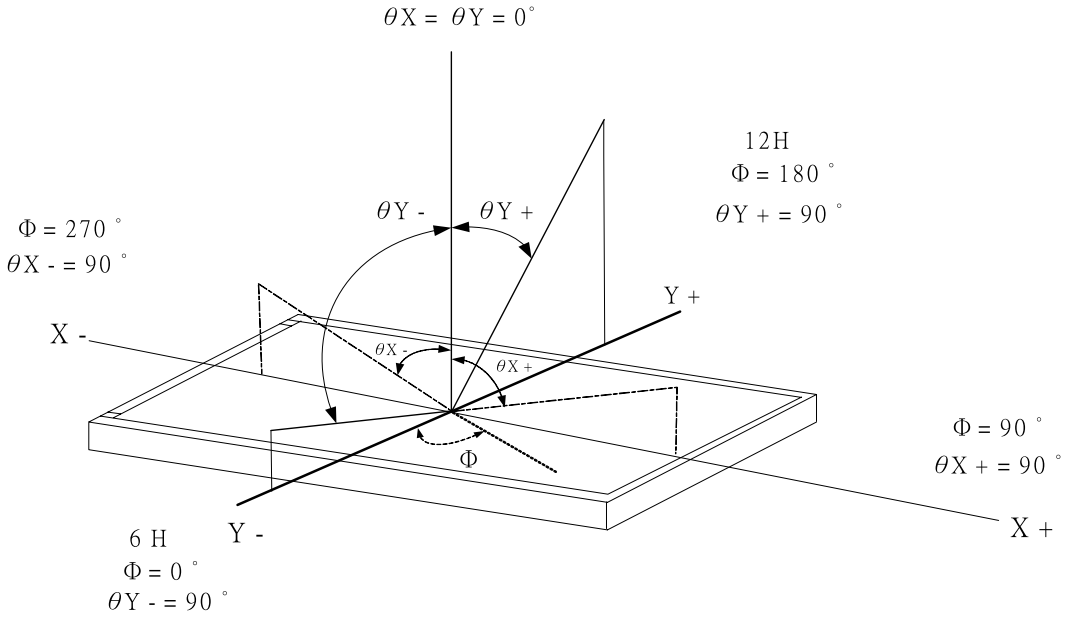
Note3: Definition of contrast ratio:

Contrast ratio is calculated with the following formula

$$\text{Contrast ratio (CR)} = \frac{\text{Photo detector output when LCD is at “White” state}}{\text{Photo detector output when LCD is at “Black” state}}$$

Note4: Definition of viewing angle:

Refer to figure as below:



1.6 Backlight & LED Characteristics

LCD Module with LED Backlight

Maximum Ratings

Item	Symbol	Conditions	Min.	Max.	Unit
Forward Current	IF	Ta =25℃	-	TBD	mA
Reverse Voltage	VR	Ta =25℃	-	TBD	V

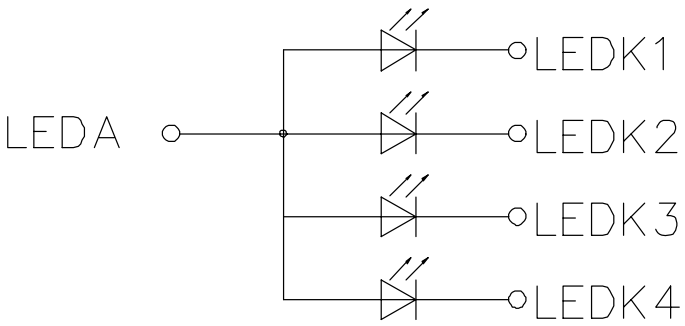
Electrical / Optical Characteristics

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Forward Voltage	VF	IF= TBD mA	(2.9)	(3.2)	(3.5)	V
Average Brightness (without LCD)	IV		(5000)	-	-	cd/m^2
Color of CIE Coordinate*1 (Without LCD)	X		(0.25)	(0.275)	(0.3)	*2
	Y		(0.25)	(0.275)	(0.3)	
Color	White					

*1：This value will be changed while mass production.

*2：△B=B(min) / B(max) *100%

B/L Internal Circuit Diagram



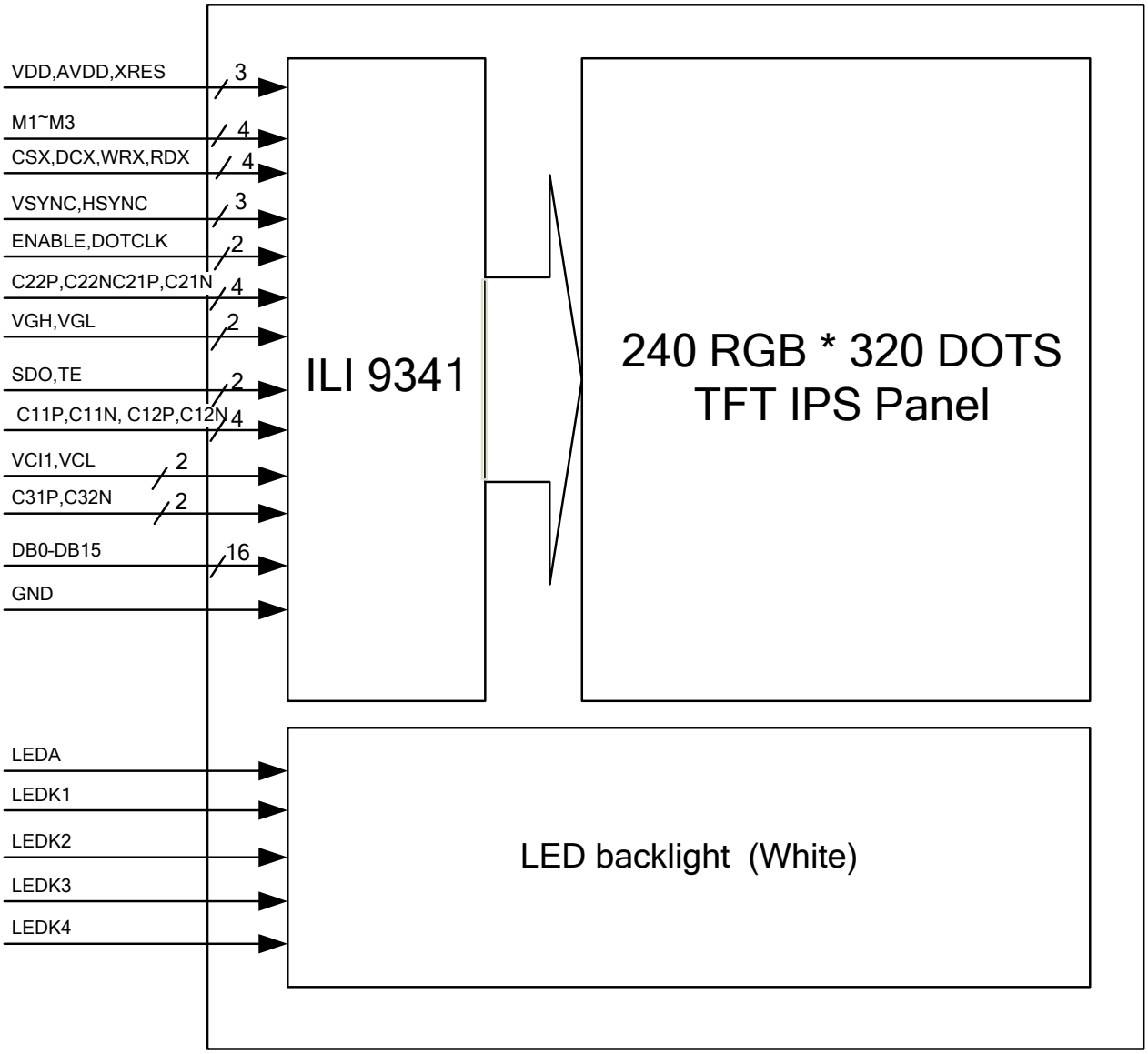
2. MODULE STRUCTURE

2.1 Counter Drawing

2.1.1 LCM Mechanical Diagram

* See Appendix

2.1.2 Block Diagram



2.2 Interface Pin Description

Pin No.	Symbol	Function
1	GND	System Ground.(0V)
2	GND	System Ground.(0V)
3	LEDK4	Power supply for LED Backlight Cathode input.
4	LEDK3	Power supply for LED Backlight Cathode input.
5	LEDK2	Power supply for LED Backlight Cathode input.
6	LEDK1	Power supply for LED Backlight Cathode input.
7	LEDA	Power supply for LED Backlight Anode input.
8	C22P	Place a 1uF/25V capacitor between C22P and C22N.
9	C22N	Place a 1uF/25V capacitor between C22N and C22P.
10	C21P	Place a 1uF/10V capacitor between C21P and C21N.
11	C21N	Place a 1uF/10V capacitor between C21N and C21P.
12	VGH	VGH pad. Place a 1uF/25V capacitor to GND.
13	VGL	VGL pad. Place a 1uF/25V capacitor to GND.
14	AVDD	AVDD pad. Place a 1uF/10V capacitor to GND.
15	C12P	Place a 1uF/10V capacitor between C12P and C12N.
16	C12N	Place a 1uF/10V capacitor between C12N and C12P.
17	C11P	Place a 1uF/10V capacitor between C11P and C11N.
18	C11N	Place a 1uF/10V capacitor between C11N and C11P.
19	GND	System Ground.(0V)
20	GND	System Ground.(0V)
21	GND	System Ground.(0V)
22	IM3	MPU Parallel interface bus and serial interface select If use RGB Interface must select serial interface. * : Fix this pin at VDDI or VSS.
23	IM2	

Pin No.	Symbol	Function
24	IM1	MPU Parallel interface bus and serial interface select If use RGB Interface must select serial interface. * : Fix this pin at VDDI or VSS.
25	IM0	
26	RESX	This signal will reset the device and must be applied to properly initialize the chip. Signal is active low.
27	CSX	Chip select input pin (“Low” enable).
28	D/CX (SCL)	This pin is used to select “Data or Command” in the parallel interface or 4-wire 8-bit serial data interface. When DCX = ’1’, data is selected. When DCX = ’0’, command is selected. This pin is used serial interface clock in 3-wire 9-bit / 4-wire 8-bit serial data interface. If not used, this pin should be connected to VDDI or VSS.
29	WRX (D/CX)	- 8080-Ⅰ/8080-Ⅱ system (WRX): Serves as a write signal and writes data at the rising edge. - 4-line system (D/CX): Serves as command or parameter select. Fix to VDDI level when not in use.
30	RDX	8080-Ⅰ/8080-Ⅱ system (RDX): Serves as a read signal and MCU read data at the rising edge. Fix to VDDI level when not in use.
31	VSYNC	Frame synchronizing signal for RGB interface operation. Fix to VDDI or VSS level when not in use.
32	HSYNC	Line synchronizing signal for RGB interface operation. Fix to VDDI or VSS level when not in use
33	ENABLE	Data enable signal for RGB interface operation. Fix to VDDI or VSS level when not in use
34	DOTCLK	Dot clock signal for RGB interface operation. Fix to VDDI or VSS level when not in use
35	SDA	The data is applied on the rising edge of the SCL signal. If not used, fix this pin at VDDI or VSS.
36	DB0	Bi-directional data bus.
37	DB1	Bi-directional data bus.
38	DB2	Bi-directional data bus.
39	DB3	Bi-directional data bus.

Pin No.	Symbol	Function
40	DB4	Bi-directional data bus.
41	DB5	Bi-directional data bus.
42	DB6	Bi-directional data bus.
43	DB7	Bi-directional data bus.
44	DB8	Bi-directional data bus.
45	DB9	Bi-directional data bus.
46	DB10	Bi-directional data bus.
47	DB11	Bi-directional data bus.
48	DB12	Bi-directional data bus.
49	DB13	Bi-directional data bus.
50	DB14	Bi-directional data bus.
51	DB15	Bi-directional data bus.
52	DB16	Bi-directional data bus.
53	DB17	Bi-directional data bus.
54	TE	Tearing effect output pin to synchronize MPU to frame writing, activated by S/W command. When this pin is not activated, this pin is low. If not used, open this pin.
55	VDD	Power supply.(2.8V) .
56	VDD	Power supply.(2.8V) .
57	VDD	Power supply.(2.8V) .
58	VCI1	VCI1 pad. Place a 1uF/10V capacitor to GND.
59	VCL	VCL pad. Place a 1uF/10V capacitor to GND.
60	GND	System Ground.(0V)
61	GND	System Ground.(0V)

IM3	IM2	IM1	IM0	Interface	Register/Content	GRAM
0	1	0	1	3-wire 9-bit data serial I	SDA: In/OUT	
0	1	1	0	4-wire 8-bit data serial I	SDA: In/OUT	
1	1	0	1	3-wire 9-bit data serial II	SDA: In / SDO: Out	
1	1	1	0	4-wire 8-bit data serial II	SDA: In / SDO: Out	
0	0	0	0	8080 MCU 8-bit Parallel I	D[7:0]	D[7:0]
0	0	0	1	8080 MCU 16-bit Parallel I	D[7:0]	D[15:0]
0	0	1	0	8080 MCU 9-bit Parallel I	D[7:0]	D[8:0]
0	0	1	1	8080 MCU 18-bit Parallel I	D[7:0]	D[17:0]
1	0	0	0	8080 MCU 16-bit Parallel II	D[8:1]	D[17:10] D[8:1]
1	0	0	1	8080 MCU 8-bit Parallel II	D[17:10]	D[17:10]
1	0	1	0	8080 MCU 18-bit Parallel II	D[8:11]	D[17:0]
1	0	1	1	8080 MCU 9-bit Parallel II	D[17:10]	D[17:9]

2.2.1 Application Notes:

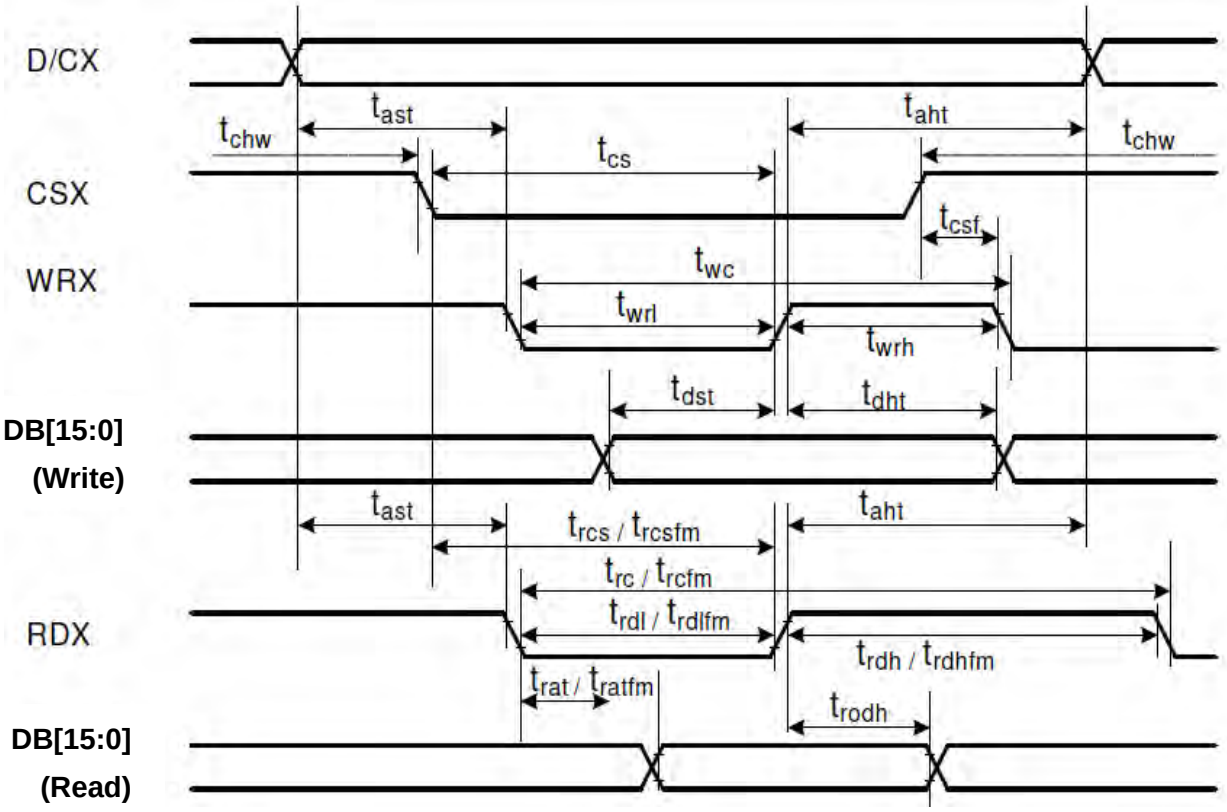
TBD

2.2.2 Refer Initial code:

TBD

2.3 Timing Characteristics

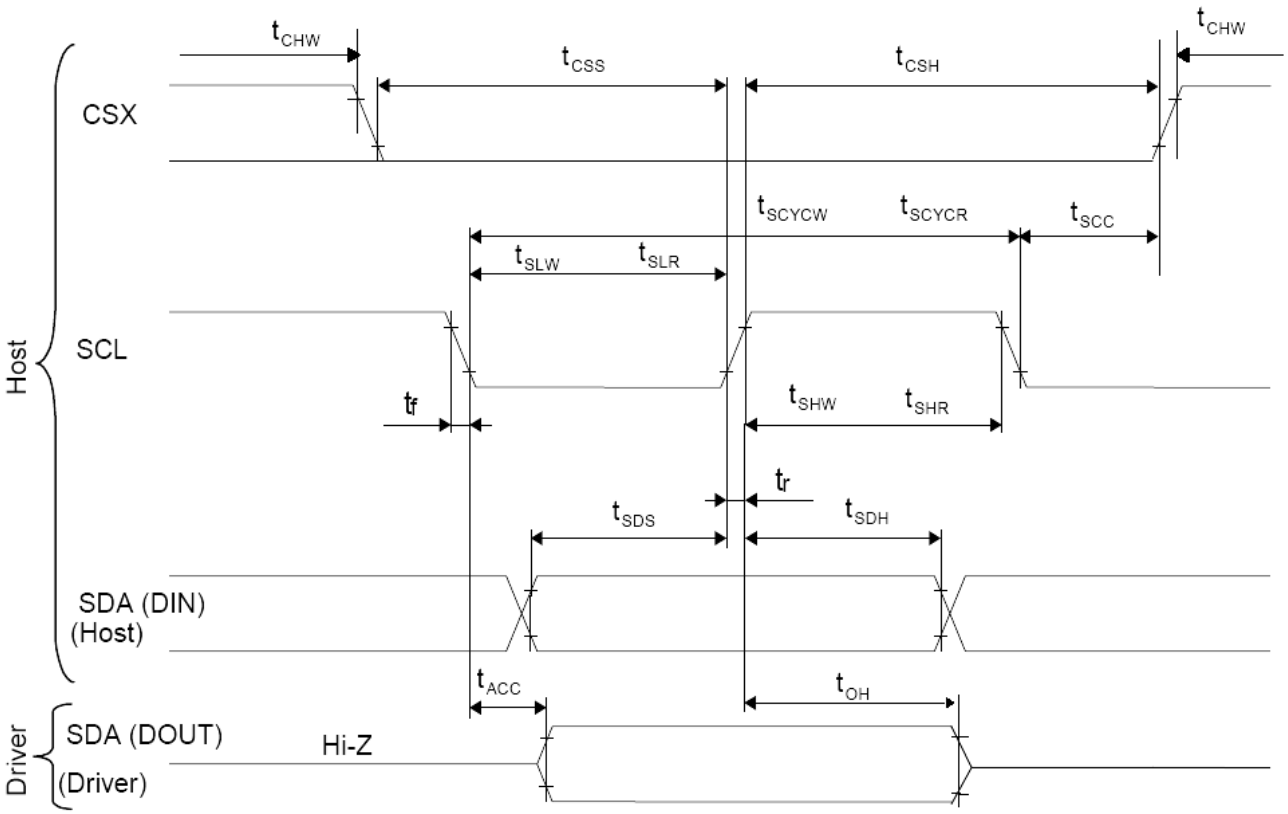
Display Parallel 8080 system 16/8-bit Interface Timing Characteristics



Signal	Symbol	Parameter	min	max	Unit	Description
DCX	tast	Address setup time	0	-	ns	
	taht	Address hold time (Write/Read)	0	-	ns	
CSX	tchw	CSX "H" pulse width	0	-	ns	
	tcs	Chip Select setup time (Write)	15	-	ns	
	trcs	Chip Select setup time (Read ID)	45	-	ns	
	trcsfm	Chip Select setup time (Read FM)	355	-	ns	
	tcsf	Chip Select Wait time (Write/Read)	10	-	ns	
WRX	twc	Write cycle	66	-	ns	
	twrh	Write Control pulse H duration	15	-	ns	
	twrl	Write Control pulse L duration	15	-	ns	
RDX (FM)	trcfm	Read Cycle (FM)	450	-	ns	
	trdhfm	Read Control H duration (FM)	90	-	ns	
	trdlfm	Read Control L duration (FM)	355	-	ns	
RDX (ID)	trc	Read cycle (ID)	160	-	ns	
	trdh	Read Control pulse H duration	90	-	ns	
	trdl	Read Control pulse L duration	45	-	ns	
DB[15:0] DB[7:0]	tdst	Write data setup time	10	-	ns	For maximum CL=30pF For minimum CL=8pF
	tdht	Write data hold time	10	-	ns	
	trat	Read access time	-	40	ns	
	tratfm	Read access time	-	340	ns	
	trod	Read output disable time	20	80	ns	

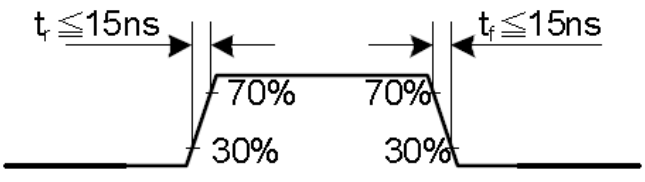
Note: Ta = -30 to 70 °C, VCC=1.65V to 3.3V, VCI=2.5V to 3.3V, GND=0V

Display Serial Interface Timing Characteristics (3-line SPI system)

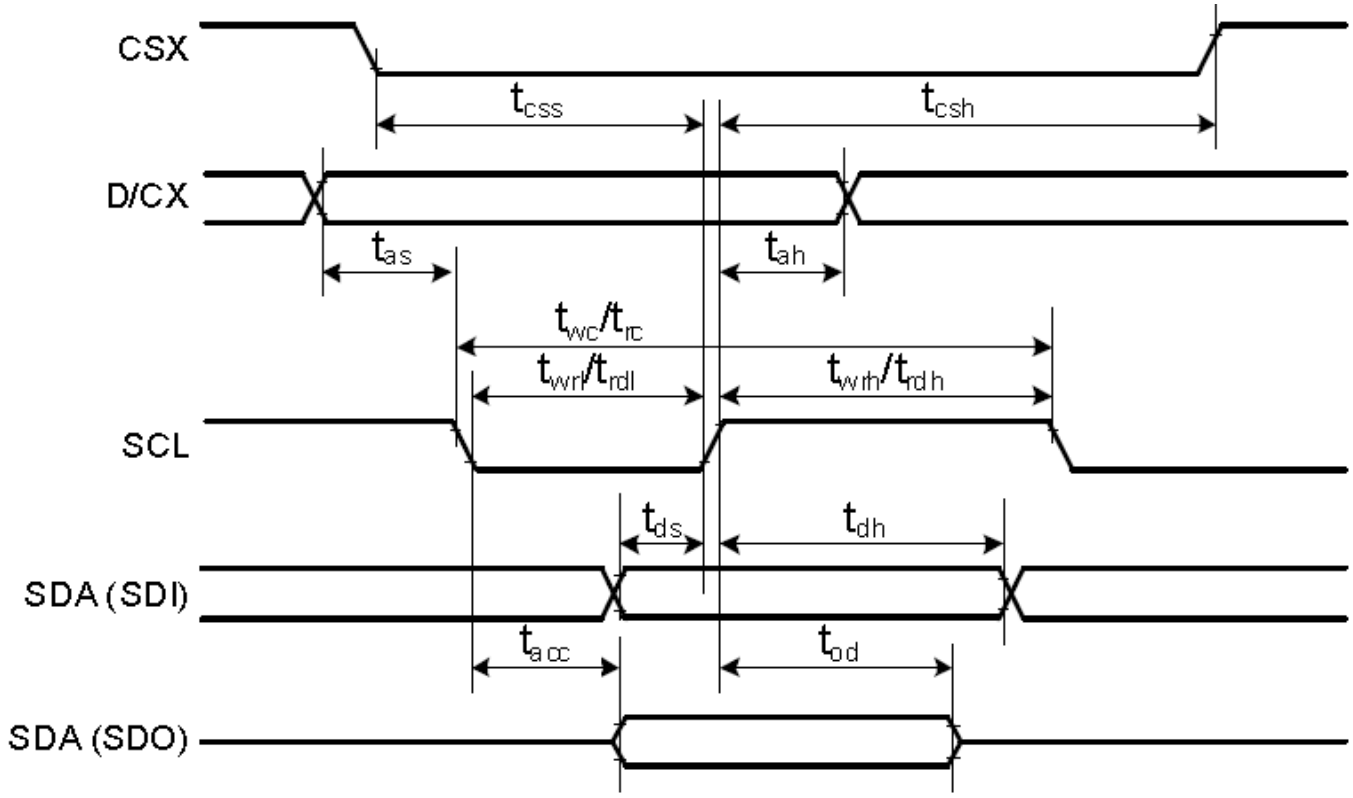


Signal	Symbol	Parameter	min	max	Unit	Description
SCL	tscycw	Serial Clock Cycle (Write)	100	-	ns	
	tshw	SCL "H" Pulse Width (Write)	40	-	ns	
	tslw	SCL "L" Pulse Width (Write)	40	-	ns	
	tscycr	Serial Clock Cycle (Read)	150	-	ns	
	tshr	SCL "H" Pulse Width (Read)	60	-	ns	
	tslr	SCL "L" Pulse Width (Read)	60	-	ns	
SDA / SDI (Input)	tsds	Data setup time (Write)	30	-	ns	
	tsdh	Data hold time (Write)	30	-	ns	
SDA / SDO (Output)	tacc	Access time (Read)	10	-	ns	
	toh	Output disable time (Read)	10	50	ns	
CSX	tscc	SCL-CSX	20	-	ns	
	tchw	CSX "H" Pulse Width	40	-	ns	
	tcss	CSX-SCL Time	60	-	ns	
	tcsh		65	-	ns	

Note: Ta = 25 °C, VDDI=1.65V to 3.3V, VCI=2.5V to 3.3V, AGND=VSS=0V

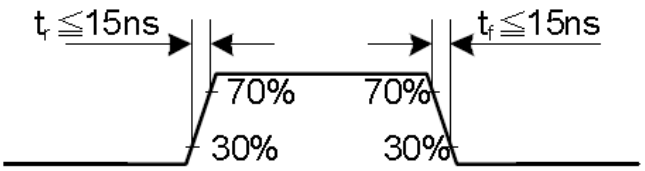


Display Serial Interface Timing Characteristics (4-line SPI system)

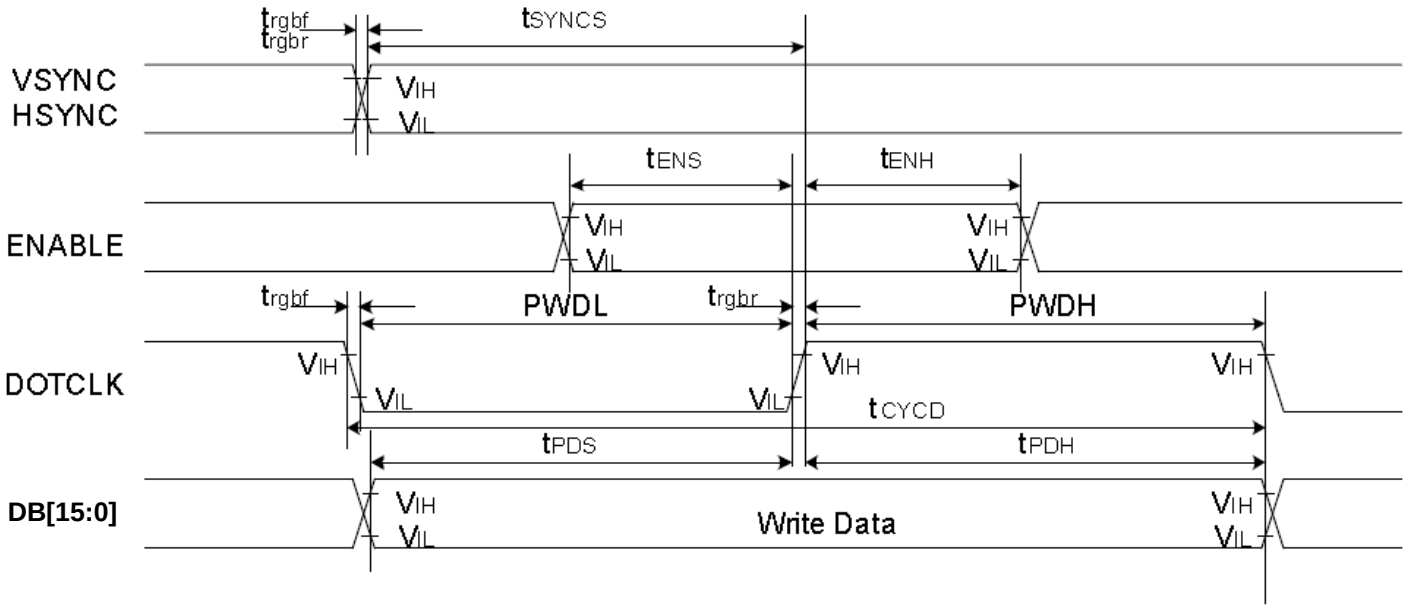


Signal	Symbol	Parameter	min	max	Unit	Description
CSX	tcss	Chip select time (Write)	40	-	ns	
	tcsh	Chip select hold time (Read)	40	-	ns	
SCL	twc	Serial clock cycle (Write)	100	-	ns	
	twrh	SCL “H” pulse width (Write)	40	-	ns	
	twrl	SCL “L” pulse width (Write)	40	-	ns	
	trc	Serial clock cycle (Read)	150	-	ns	
	trdh	SCL “H” pulse width (Read)	60	-	ns	
	trdl	SCL “L” pulse width (Read)	60	-	ns	
D/CX	tas	D/CX setup time	10	-		
	tah	D/CX hold time (Write / Read)	10	-		
SDA / SDI (Input)	tds	Data setup time (Write)	30	-	ns	
	tdh	Data hold time (Write)	30	-	ns	
SDA / SDO (Output)	tacc	Access time (Read)	10	-	ns	For maximum CL=30pF
	tod	Output disable time (Read)	10	50	ns	For minimum CL=8pF

Note: Ta = 25 °C, VDDI=1.65V to 3.3V, VCI=2.5V to 3.3V, AGND=VSS=0V

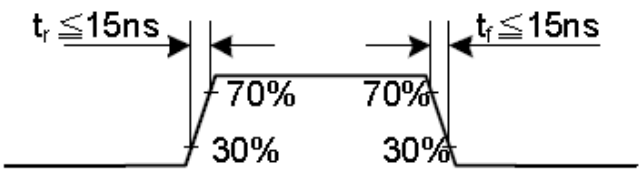


Parallel 16-bit RGB Interface Timing Characteristics

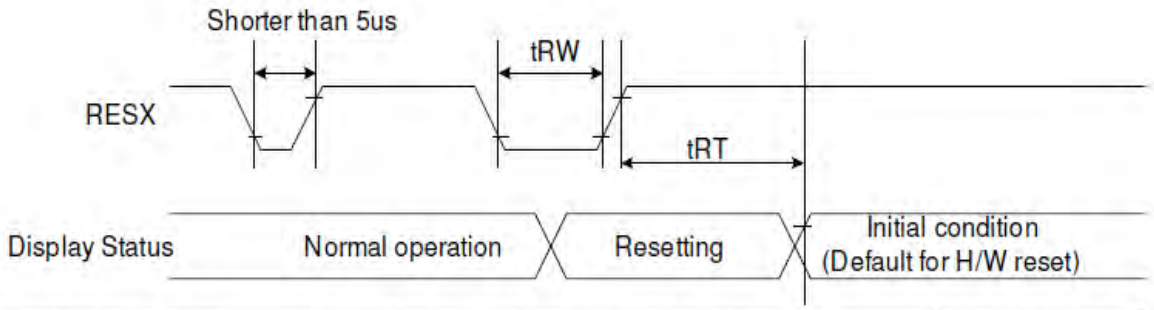


Signal	Symbol	Parameter	min	max	Unit	Description
VSYNC / HSYNC	t_{SYNCS}	VSYNC/HSYNC setup time	15	-	ns	18/16-bit bus RGB interface mode
	t_{SYNCH}	VSYNC/HSYNC hold time	15	-	ns	
DE	t_{ENS}	DE setup time	15	-	ns	
	t_{ENH}	DE hold time	15	-	ns	
DB[15:0]	t_{POS}	Data setup time	15	-	ns	
	t_{PDH}	Data hold time	15	-	ns	
DOTCLK	PWDH	DOTCLK high-level period	15	-	ns	
	PWDL	DOTCLK low-level period	15	-	ns	
	t_{CYCD}	DOTCLK cycle time	100	-	ns	
	t_{rgbr} , t_{rgbf}	DOTCLK,HSYNC,VSYNC rise/fall time	-	15	ns	
VSYNC / HSYNC	t_{SYNCS}	VSYNC/HSYNC setup time	15	-	ns	6-bit bus RGB interface mode
	t_{SYNCH}	VSYNC/HSYNC hold time	15	-	ns	
DE	t_{ENS}	DE setup time	15	-	ns	
	t_{ENH}	DE hold time	15	-	ns	
DB[15:0]	t_{POS}	Data setup time	15	-	ns	
	t_{PDH}	Data hold time	15	-	ns	
DOTCLK	PWDH	DOTCLK high-level pulse period	15	-	ns	
	PWDL	DOTCLK low-level pulse period	15	-	ns	
	t_{CYCD}	DOTCLK cycle time	100	-	ns	
	t_{rgbr} , t_{rgbf}	DOTCLK,HSYNC,VSYNC rise/fall time	-	15	ns	

Note: Ta = -30 to 70 °C, VDDI=1.65V to 3.3V, VCI=2.5V to 3.3V, AGND=VSS=0V



Reset Timing



Signal	Symbol	Parameter	Min	Max	Unit
RESX	tRW	Reset pulse duration	10		uS
	tRT	Reset cancel		5 (note 1,5)	mS
				120 (note 1,6,7)	mS

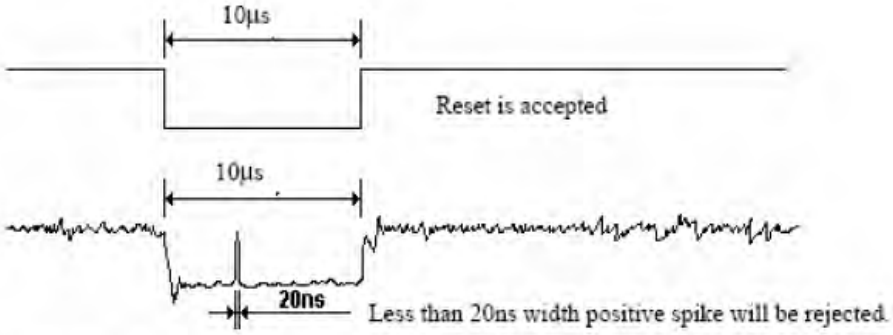
Note 1: The reset cancel includes also required time for loading ID bytes, VCOM setting and other settings from NV memory to registers. This loading is done every time when there is HW reset cancel time (tRT) within 5 ms after a rising edge of RESX.

Note 2: Spike due to an electrostatic discharge on RESX line does not cause irregular system reset according to the table below: -

RESX Pulse	Action
Shorter than 5us	Reset Rejected
Longer than 10us	Reset
Between 5us and 10us	Reset starts

Note 3: During the Resetting period, the display will be blanked (The display is entering blanking sequence, which maximum time is 120 ms, when Reset Starts in Sleep Out –mode. The display remains the blank state in Sleep In -mode.) And then return to Default condition for Hardware Reset.

Note 4: Spike Rejection also applies during a valid reset pulse as shown below:



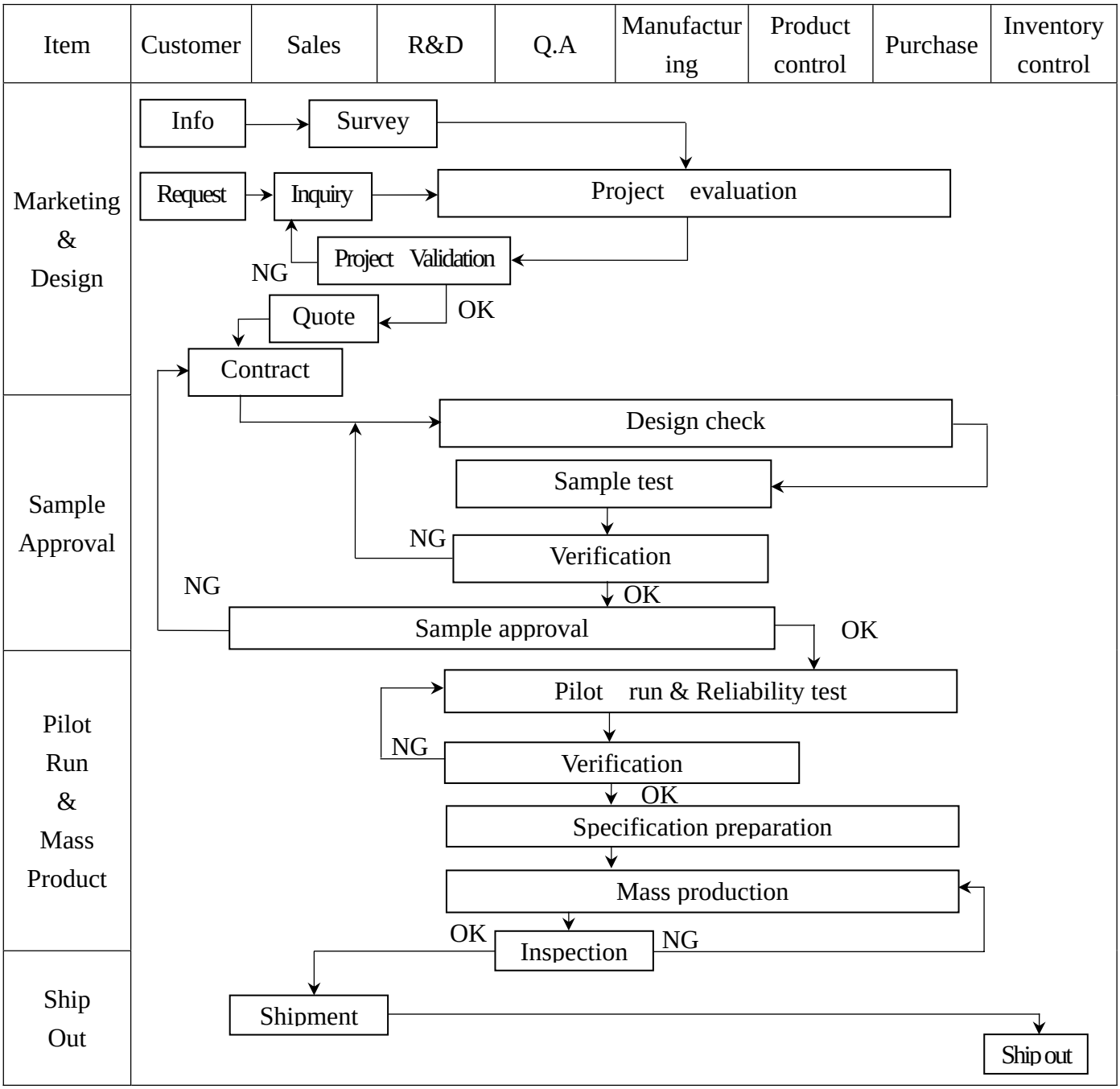
Note 5: When Reset applied during Sleep In Mode.

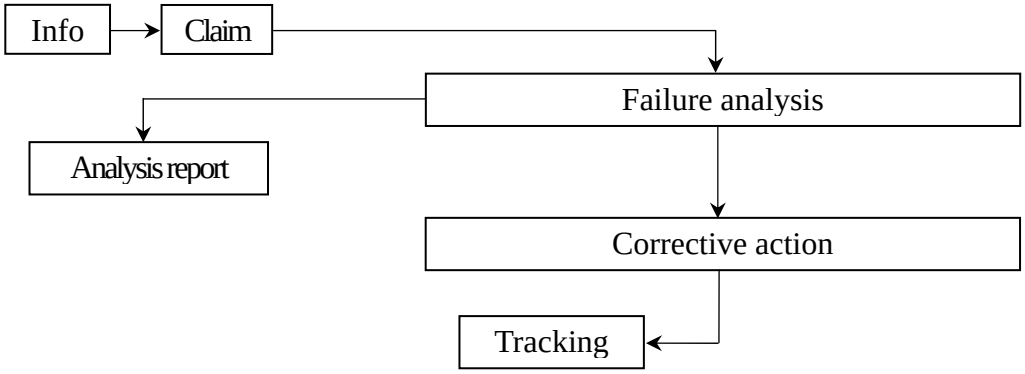
Note 6: When Reset applied during Sleep Out Mode.

Note 7: It is necessary to wait 5msec after releasing RESX before sending commands. Also Sleep Out command cannot be sent for 120msec.

3. QUALITY ASSURANCE SYSTEM

3.1 Quality Assurance Flow Chart



Item	Customer	Sales	R&D	Q.A	Manufactu ring	Product control	Purchase	Inventory control
Sales Service								
Q.A Activity	1. ISO 9001 Maintenance Activities 2. Process improvement proposal 3. Equipment calibration 4. Education And Training Activities 5. Standardization Management							

3.2. Inspection Specification

◆Scope ：The document shall be applied to TFT-LCD Module for less than 3.5" (Ver.B01).

◆Inspection Standard：MIL-STD-105E Table Normal Inspection Single Sampling Level Ⅱ.

◆Equipment：Gauge、MIL-STD、Powertip Tester、Sample

◆Defect Level：Major Defect AQL： 0.4 ； Minor Defect AQL： 1.5

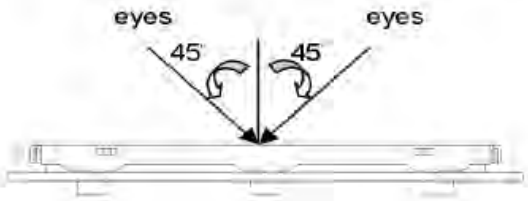
◆OUT Going Defect Level：Sampling.

◆Standard of the product appearance test：

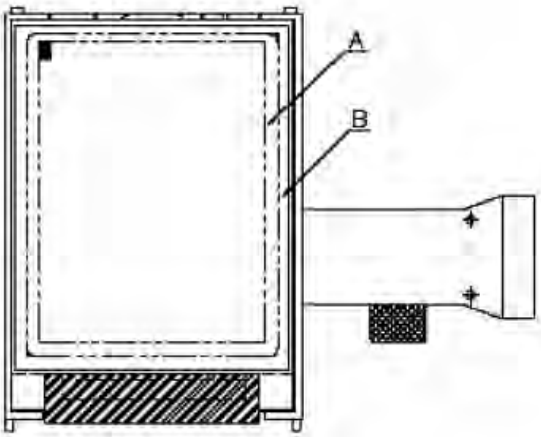
a. Manner of appearance test：

(1). The test best be under 20W×2 fluorescent light，and distance of view must be at 30 cm.

(2). The test direction is base on about around 45° of vertical line.



(3). Definition of area.



A area：viewing area

B area：Outside of viewing area

(4). Standard of inspection： (Unit：mm)

◆Specification For TFT-LCD Module Less Than 3.5″ : (Ver.B01)

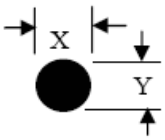
<table>
<tr><th>NO</th><th>Item</th><th>Criterion</th><th>Level</th></tr>
<tr><td rowspan="3">01</td><td rowspan="3">Product condition</td><td>1.1 The part number is inconsistent with work order of production.</td><td>Major</td></tr>
<tr><td>1.2 Mixed product types.</td><td>Major</td></tr>
<tr><td>1.3 Assembled in inverse direction.</td><td>Major</td></tr>
<tr><td>02</td><td>Quantity</td><td>2.1 The quantity is inconsistent with work order of production.</td><td>Major</td></tr>
<tr><td>03</td><td>Outline dimension</td><td>3.1 Product dimension and structure must conform to structure diagram.</td><td>Major</td></tr>
<tr><td rowspan="5">04</td><td rowspan="5">Electrical Testing</td><td>4.1 Missing line character and icon.</td><td>Major</td></tr>
<tr><td>4.2 No function or no display.</td><td>Major</td></tr>
<tr><td>4.3 Display malfunction.</td><td>Major</td></tr>
<tr><td>4.4 LCD viewing angle defect.</td><td>Major</td></tr>
<tr><td>4.5 Current consumption exceeds product specifications.</td><td>Major</td></tr>
<tr><td>05</td><td>Dot defect

(Bright dot、Dark dot)

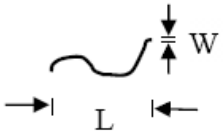
On -display</td><td>
<table>
<tr><th colspan="2">Item</th><th>Acceptance (Q'ty)</th></tr>
<tr><td rowspan="4">Dot Defect</td><td>Bright Dot</td><td>≦ 2</td></tr>
<tr><td>Dark Dot</td><td>≦ 3</td></tr>
<tr><td>Joint Dot</td><td>≦ 2</td></tr>
<tr><td>Total</td><td>≦ 3</td></tr>
</table>
5.1 Inspection pattern：full white , full black , Red , Green and blue screens.
5.2 It is defined as dot defect if defect area ＞1/2 dot.
5.3 The distance between two dot defect ≧5 mm.
</td><td>Minor</td></tr>
</table>

◆Specification For TFT-LCD Module Less Than 3.5″ : (Ver.B01)

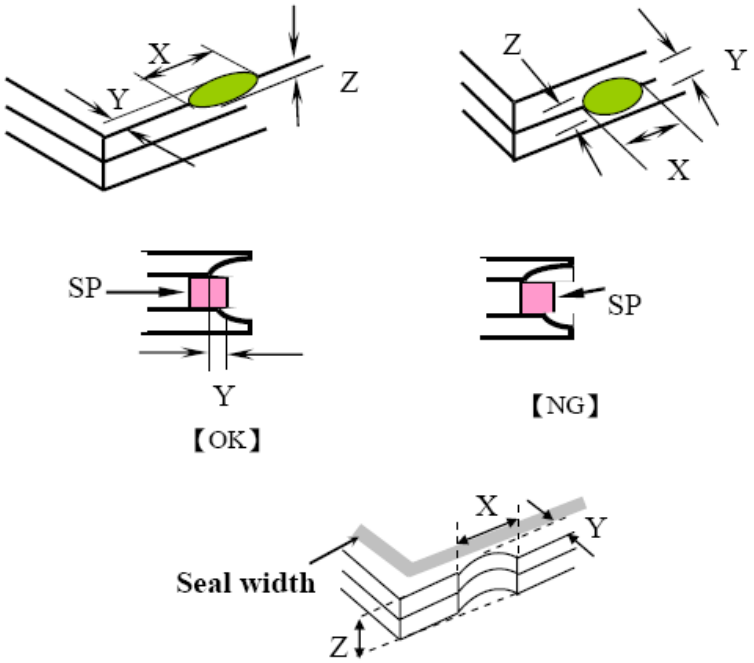
<table>
<tr><th>NO</th><th>Item</th><th>Criterion</th><th>Level</th></tr>
<tr><td>06</td><td>Black or white dot、scratch、contamination

Round type
 

Φ=(x+y) / 2

Line type
 
</td><td>6.1 Round type (Non-display or display) :
<table>
<tr><th rowspan="2">Dimension
(diameter : Φ)</th><th colspan="2">Acceptance (Q'ty)</th></tr>
<tr><th>A area</th><th>B area</th></tr>
<tr><td>Φ ≦ 0.15</td><td>Ignore</td><td rowspan="5">Ignore</td></tr>
<tr><td>0.15 < Φ ≦ 0.20</td><td>2</td></tr>
<tr><td>0.20 < Φ ≦ 0.30</td><td>2</td></tr>
<tr><td>Φ > 0.30</td><td>0</td></tr>
<tr><td>Total</td><td>3</td></tr>
</table>
6.2 Line type(Non-display or display) :
<table>
<tr><th colspan="2">Dimension</th><th colspan="2">Acceptance (Q'ty)</th></tr>
<tr><th>Length (L)</th><th>Width (W)</th><th>A area</th><th>B area</th></tr>
<tr><td>---</td><td>W ≦ 0.03</td><td>Ignore</td><td rowspan="4">Ignore</td></tr>
<tr><td>L ≦5.0</td><td>0.03 <W ≦ 0.05</td><td>3</td></tr>
<tr><td>---</td><td>W >0.05</td><td>As round type</td></tr>
<tr><td colspan="2">Total</td><td>3</td></tr>
</table></td><td>Minor</td></tr>
<tr><td>07</td><td>Polarizer Bubble</td><td>
<table>
<tr><th rowspan="2">Dimension
(diameter : Φ)</th><th colspan="2">Acceptance (Q'ty)</th></tr>
<tr><th>A area</th><th>B area</th></tr>
<tr><td>Φ ≦ 0.20</td><td>Ignore</td><td rowspan="4">Ignore</td></tr>
<tr><td>0.20 < Φ ≦ 0.50</td><td>3</td></tr>
<tr><td>Φ > 0.50</td><td>0</td></tr>
<tr><td>Total</td><td>3</td></tr>
</table></td><td>Minor</td></tr>
</table>

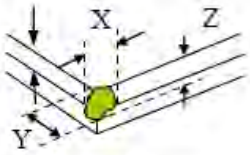
◆Specification For TFT-LCD Module Less Than 3.5″ : (Ver.B01)

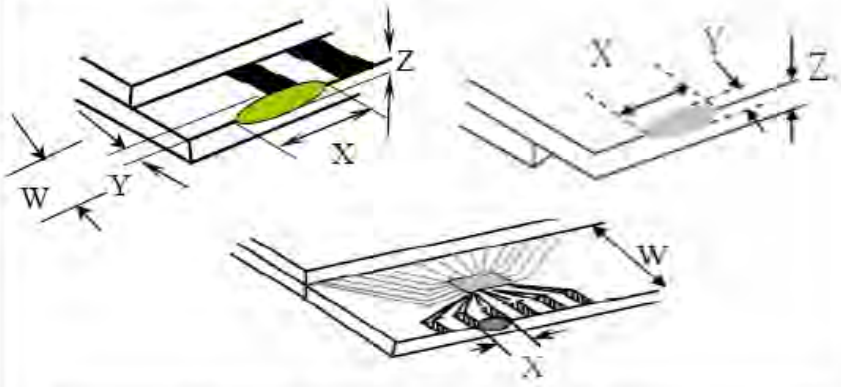
NO	Item	Criterion	Level
08	The crack of glass	Symbols : X : The length of crack Y : The width of crack. Z : The thickness of crack W : terminal length t : The thickness of glass a : LCD side length 8.1 General glass chip : 8.1.1 Chip on panel surface and crack between panels: 	Minor

X	Y	Z
≦ a	Crack can't enter viewing area	≦1/2 t
≦ a	Crack can't exceed the half of SP width.	1/2 t < Z ≦2 t

◆Specification For TFT-LCD Module Less Than 3.5″ : (Ver.B01)

<table>
<tr><th>NO</th><th>Item</th><th>Criterion</th><th>Level</th></tr>
<tr><td rowspan="3">08</td><td rowspan="3">The crack of glass</td><td>Symbols :

X : The length of crack
Z : The thickness of crack
t : The thickness of glass
Y : The width of crack.
W : terminal length
a : LCD side length</td><td rowspan="3">Minor</td></tr>
<tr><td>8.1.2 Corner crack :
 

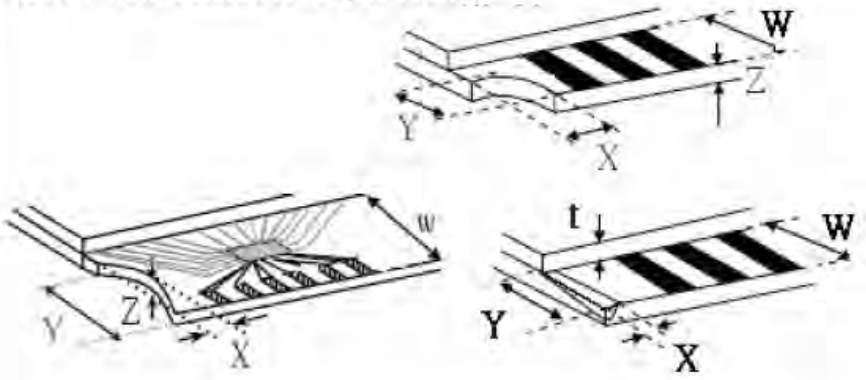
<table>
<tr><th>X</th><th>Y</th><th>Z</th></tr>
<tr><td>≦1/5 a</td><td>Crack can't enter viewing area</td><td>Z ≦ 1/2 t</td></tr>
<tr><td>≦1/5 a</td><td>Crack can't exceed the half of SP width.</td><td>1/2 t < Z ≦ 2 t</td></tr>
</table></td></tr>
<tr><td>8.2 Protrusion over terminal :
8.2.1 Chip on electrode pad :
 

<table>
<tr><th></th><th>X</th><th>Y</th><th>Z</th></tr>
<tr><td>Front</td><td>≦ a</td><td>≦ 1/2 W</td><td>≦ t</td></tr>
<tr><td>Back</td><td>≦ a</td><td>≦ W</td><td>≦ 1/2 t</td></tr>
</table></td></tr>
</table>

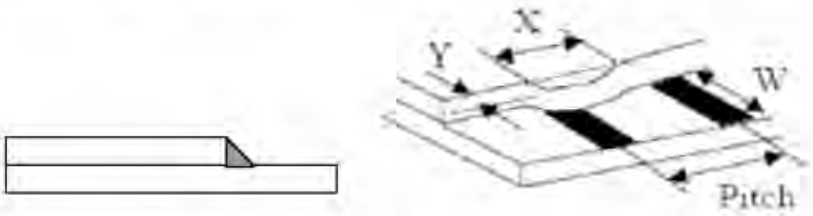
◆Specification For TFT-LCD Module Less Than 3.5″ : (Ver.B01)

<table>
<tr><th>NO</th><th>Item</th><th>Criterion</th><th>Level</th></tr>
<tr><td>08</td><td>The crack of glass</td><td>
Symbols :

X : The length of crack　　Y : The width of crack.
Z : The thickness of crack　　W : terminal length
t : The thickness of glass　　a : LCD side length

8.2.2 Non-conductive portion :


<table>
<tr><th>X</th><th>Y</th><th>Z</th></tr>
<tr><td>≦ 1/3 a</td><td>≦W</td><td>≦t</td></tr>
</table>
⊙ If the chipped area touches the ITO terminal, over 2/3 of the ITO must remain and be inspected according to electrode terminal specifications.

8.2.3 Glass remain :


<table>
<tr><th>X</th><th>Y</th><th>Z</th></tr>
<tr><td>≦ a</td><td>≦ 1/3 W</td><td>≦t</td></tr>
</table>
</td><td>Minor</td></tr>
</table>

◆Specification For TFT-LCD Module Less Than 3.5″ : (Ver.B01)

NO	Item	Criterion	Level
09	Backlight elements	9.1 Backlight can't work normally.	Major
		9.2 Backlight doesn't light or color is wrong.	Major
		9.3 Illumination source flickers when lit.	Major
10	General appearance	10.1 Pin type、quantity、dimension must match type in structure diagram.	Major
		10.2 No short circuits in components on PCB or FPC .	Major
		10.3 Parts on PCB or FPC must be the same as on the production characteristic chart .There should be no wrong parts , missing parts or excess parts.	Major
		10.4 Product packaging must the same as specified on packaging specification sheet.	Minor
		10.5 The folding and peeled off in polarizer are not acceptable.	Minor
		10.6 The PCB or FPC between B/L assembled distance(PCB or FPC) is ≦1.5 mm.	Minor

4. RELIABILITY TEST

4.1 Reliability Test Condition (Ver.B01)

<table>
<tr><th>NO.</th><th>TEST ITEM</th><th colspan="2">TEST CONDITION</th></tr>
<tr><td>1</td><td>High Temperature Storage Test</td><td colspan="2">Keep in +80 ±2℃ 96 hrs
Surrounding temperature, then storage at normal condition 4hrs.</td></tr>
<tr><td>2</td><td>Low Temperature Storage Test</td><td colspan="2">Keep in -30 ±2℃ 96 hrs
Surrounding temperature, then storage at normal condition 4hrs.</td></tr>
<tr><td>3</td><td>High Temperature / High Humidity Storage Test</td><td colspan="2">Keep in +60℃ / 90% R.H duration for 96 hrs
Surrounding temperature, then storage at normal condition 4hrs.
(Excluding the polarizer)</td></tr>
<tr><td rowspan="2">4</td><td rowspan="2">ESD Test</td><td>Air Discharge:
Apply 2 KV with 5 times
Discharge for each polarity +/-</td><td>Contact Discharge:
Apply 250V with 5 times
discharge for each polarity +/-</td></tr>
<tr><td colspan="2">1. Temperature ambiance:15℃～35℃
2. Humidity relative:30%～60%
3. Energy Storage Capacitance(Cs+Cd):150pF±10%
4. Discharge Resistance(Rd):330Ω±10%
5. Discharge, mode of operation:
Single Discharge (time between successive discharges at least 1 s)
(Tolerance if the output voltage indication: ±5%)</td></tr>
<tr><td>5</td><td>Temperature Cycling Storage Test</td><td colspan="2">-30℃ → +25℃ → +80℃ → +25℃
(30mins) (5mins) (30mins) (5mins)
10 Cycle
Surrounding temperature, then storage at normal condition 4hrs.</td></tr>
<tr><td>6</td><td>Vibration Test (Packaged)</td><td colspan="2">1. Sine wave 10～55 Hz frequency (1 min)
2. The amplitude of vibration :1.5 mm
3. Each direction (X、Y、Z) duration for 2 Hrs</td></tr>
<tr><td>7</td><td>Drop Test (Packaged)</td><td colspan="2"><table><tr><th>Packing Weight (Kg)</th><th>Drop Height (cm)</th></tr><tr><td>0 ~ 45.4</td><td>122</td></tr><tr><td>45.4 ~ 90.8</td><td>76</td></tr><tr><td>90.8 ~ 454</td><td>61</td></tr><tr><td>Over 454</td><td>46</td></tr></table>Drop direction :※ 1 corner / 3 edges / 6 sides each 1times</td></tr>
</table>

5. PRECAUTION RELATING PRODUCT HANDLING

5.1 SAFETY

5.1.1 If the LCD panel breaks , be careful not to get the liquid crystal to touch your skin.

5.1.2 If the liquid crystal touches your skin or clothes , please wash it off immediately by using soap and water.

5.2 HANDLING

5.2.1 Avoid any strong mechanical shock which can break the glass.

5.2.2 Avoid static electricity which can damage the CMOS LSI—When working with the module , be sure to ground your body and any electrical equipment you may be using.

5.2.3 Do not remove the panel or frame from the module.

5.2.4 The polarizing plate of the display is very fragile. So , please handle it very carefully ,do not touch , push or rub the exposed polarizing with anything harder than an HB pencil lead (glass , tweezers , etc.)

5.2.5 Do not wipe the polarizing plate with a dry cloth , as it may easily scratch the surface of plate.

5.2.6 Do not touch the display area with bare hands , this will stain the display area.

5.2.7 Do not use ketonics solvent & aromatic solvent. Use with a soft cloth soaked with a cleaning naphtha solvent.

5.2.8 To control temperature and time of soldering is 320±10℃and 3-5 sec.

5.2.9 To avoid liquid (include organic solvent) stained on LCM .

5.3 STORAGE

5.3.1 Store the panel or module in a dark place where the temperature is 25℃ ±5℃ and the humidity is below 65% RH.

5.3.2 Do not place the module near organics solvents or corrosive gases.

5.3.3 Do not crush , shake , or jolt the module.

5.4 TERMS OF WARRANTY

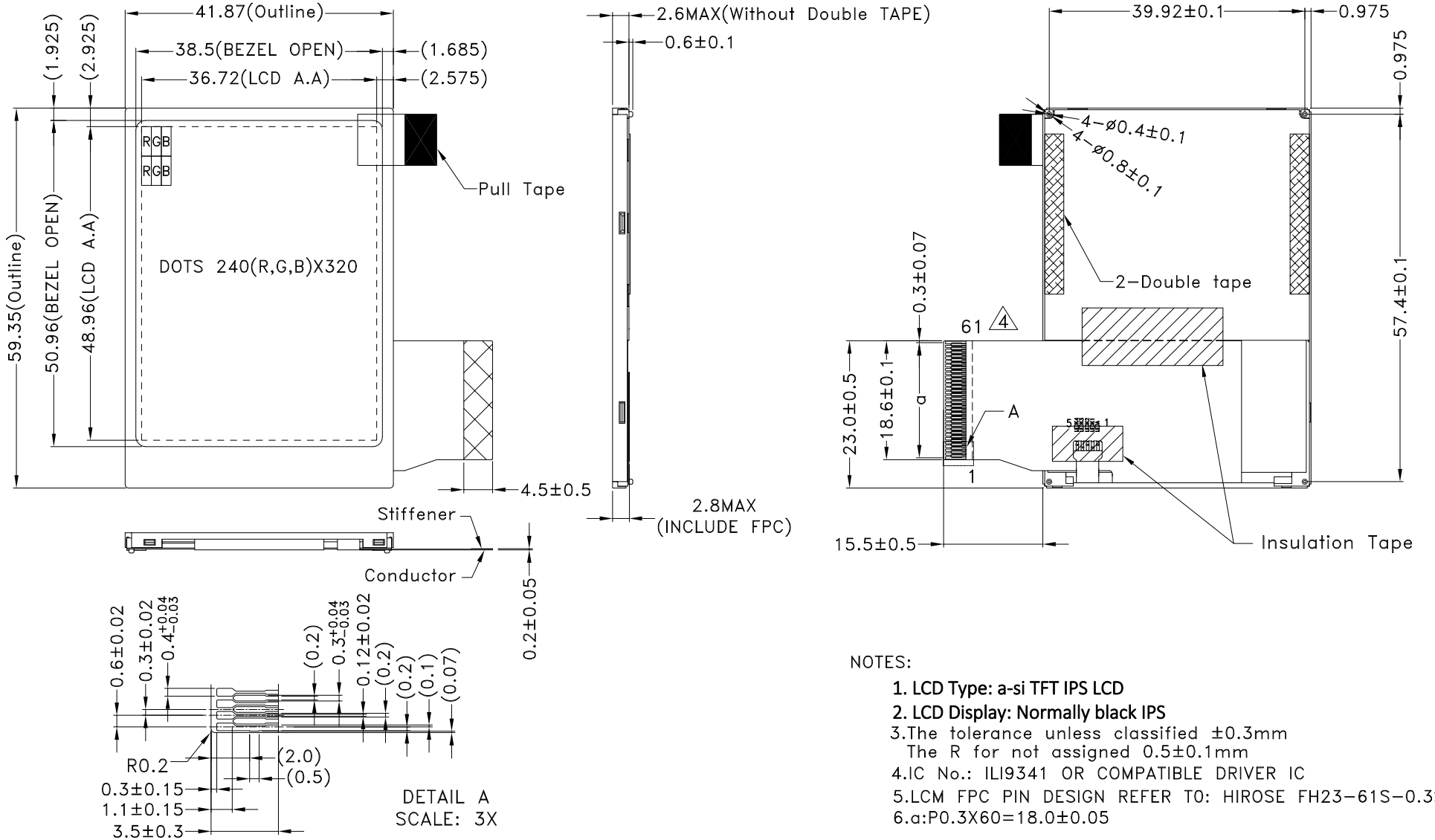
5.4.1 Applicable warrant period

The period is within Twenty-four months since the date of shipping out under normal using and storage conditions.

5.4.2 Unaccepted responsibility

This product has been manufactured to your company’s specification as a part for use in your company’s general electronic products. It is guaranteed to perform according to delivery specifications. For any other use apart from general electronic equipment , we cannot take responsibility if the product is used in nuclear power control equipment , aerospace equipment , fire and security systems or any other applications in which there is a direct risk to human life and where extremely high levels of reliability are required.

USMP-TT024Q-01K



NOTES:

1. LCD Type: a-si TFT IPS LCD
2. LCD Display: Normally black IPS
3. The tolerance unless classified ±0.3mm
   The R for not assigned 0.5±0.1mm
4. IC No.: ILI9341 OR COMPATIBLE DRIVER IC
5. LCM FPC PIN DESIGN REFER TO: HIROSE FH23-61S-0.3SHW
6. a:P0.3X60=18.0±0.05

REV	REV BY	REVISER	DATE
007			
006			
005			
004	Modify FPC PIN NO.	Sunny	2012/12/18
003	Modify FPC & C/N	Sunny	2012/11/16
002	Modify FPC	Sunny	2012/11/01
001	NEW DRAWING	Sunny	2012/10/24

PART NO: USMP-TT024Q-01K

DRAWING NAME : LMD-USMP-TT024Q-01K

TITLE: LCD MODULE DRAWING

US Micro Products
ENGINEERED DISPLAY SOLUTIONS
6207 Bee Caves Rd., Ste. 330; Austin, TX 78746 USA
Tel: (800) 741-7755, sales@usmicroproducts.com
www.usmicroproducts.com

Design	Sunny Chen	(3)	Surface		
Check	Tina Chen	Unit	MM	Material	
Approve	Linda Lee	Scale	FIT	Thickness	
		Page	1/1	Quantity	

Length(Min) (mm)	Precision Level
1 ~ 4	-
4 ~ 16	-
16 ~ 63	-
63 ~ 250	-
250 ~ 1000	-