US Micro Products
ENGINEERED DISPLAY SOLUTIONS

TFT SPECIFICATION

Part Number	USMP-T042-680680NAV-A0
Size	4.21"
Resolution	680 x 680
Brightness	1000 cd/m²
Contrast	TBD
Viewing Angle	80/80/80/80
Operating Temp.	-30 ~ 85°C

FOR ADDITIONAL INFORMATION
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Issue Date	Approved by (customer use)	Checked by	Prepared by

(800) 741-7755
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2. RECORD OF REVISION

Rev	Date	Item	Page	Comment	Source
1	11/JUL/17’			Preliminary	

3. INTRODUCTION

The 4.21 inch round LCD is a kind of Transmissive TFT, active matrix color liquid crystal display (LCD) comprising an amorphous silicon TFT attached to each signal electrode. This module is consisting of TFT-LCD module, a driver circuit, a back-light unit. The resolution is 680 x 680 pixels.

4. GENERAL SPECIFICATIONS

Parameter	Specifications	Unit
Screen Size	4.21 (Diameter)	inch
Display Format	680(H) x (R,G,B) x 680(V)	Dots
Active Area	106.68 (Diameter)	mm
Pixel Pitch	(T.B.D.)	mm
Outline Dimension	116.48(W) x 116.9 (H) x 5.65 (D)	mm
Back-light	LED	
TFT-LCD Display mode	Normally Black	
Weight	(T.B.D.)	g
View Angle direction(TFT)	All	
our components and processes are compliant to RoHS standard		

5. ABSOLUTE MAXIMUM RATINGS

GND=0V

Parameter	Symbol	Min.	Max.	Unit	Remark
Power supply voltage	VDD	-0.3	4.6	V	
	VDDI	-0.3	4.6	V	
Operating temperature	Top	-30	85	°C	
Storage temperature	Tst	-40	90	°C	

6. ELECTRICAL CHARACTERISTICS

6.1 Operating Conditions

GND=0V,Ta=25°C

Parameter	Symbol	Min.	Typ.	Max.	Unit	Remark
Power Supply voltage	VDD	2.5	-	3.3	V	
	VDDI	1.65	-	3.3	V	
“H” level logical input voltage	V_{IH}	0.7*VDDI	-	VDDI	V	
“L” level logical input voltage	V_{IL}	0	-	0.3*VDDI	V	

6.2 Backlight Driving Consumption

Ta= 25°C

Parameter	Symbol	Min.	Typ.	Max.	Unit	Remark
LED voltage	V_L			19.8	V	Note1
LED current	I_L	-	130	-	mA	Note1
LED dice Life Time		30000			hr	Note2

7. FUNCTIONAL DESCRIPTION

7.1 AC Characteristics

Serial interface characteristic (3-pin Serial)

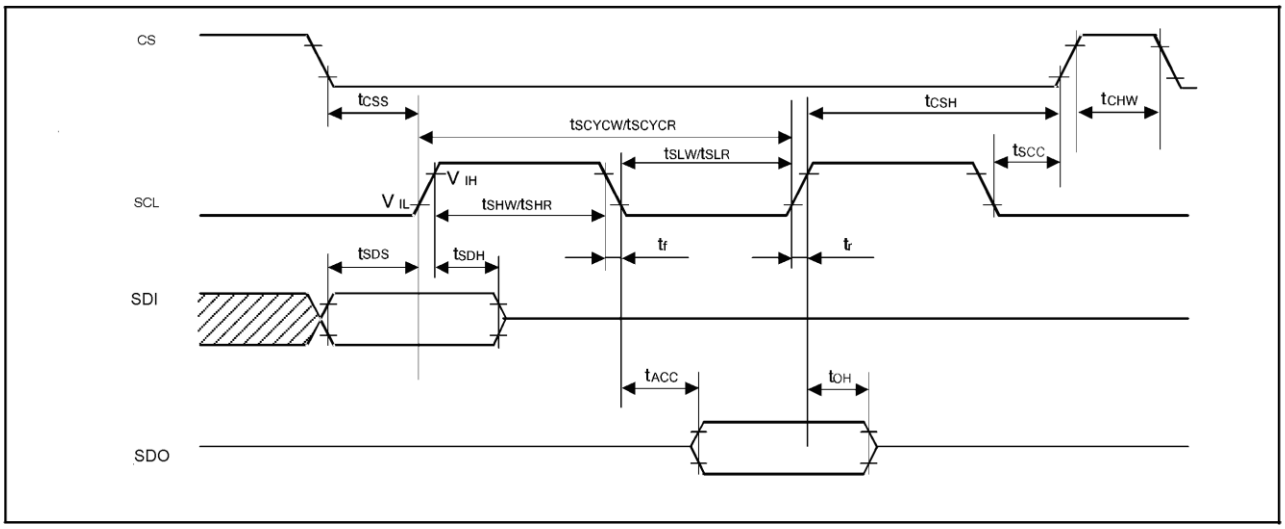
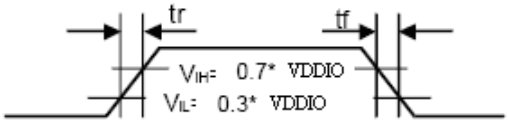


Figure 7.1-1 Serial Interface Characteristics

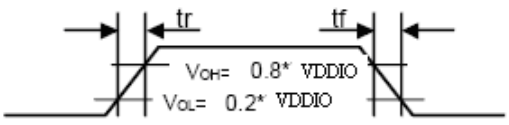
Parameter	Symbol	Conditions	MIN	TYP	MAX	Unit
Serial clock cycle (Write) SCL "H" pulse width (Write) SCL "L" pulse width (Write)	t_{SCYCW} t_{SHW} t_{SLW}	SCL	80 30 30		--	ns
Data setup time (Write) Data hold time (Write)	t_{SDS} t_{SDH}	SDI	10 10		--	ns
Serial clock cycle (Read) SCL "H" pulse width (Read) SCL "L" pulse width (Read)	t_{SCYCR} t_{SHR} t_{SLR}	SCL	150 60 60		--	ns
Access rime	t_{ACC}	SDO For maximum C_L=30pF For maximum C_L=8pF	10		60	ns
Output disable time	t_{OH}	SDO For maximum C_L=30pF For maximum C_L=8pF	15		100	ns
SCL to Chip select	t_{SCC}	CS	30		--	ns
CS "H" pulse width	t_{CHW}	CS	60		--	ns
CS -SCL time (write) CS -SCL time (write)	t_{CSS} t_{CSH}	CS	30 30		--	ns
CS -SCL time (Read) CS -SCL time (Read)	t_{CSS} t_{CSH}	CS	60 65		--	ns

Note: The input signal rise time and fall time (tr, tf) is specified at 15 ns or less.
Logic high and low levels are specified as 30% and 70% of VDDIO for Input signals.

Input Signal Slope



Output Signal Slope



7.2 RGB interface characteristic

Vertical Timings for RGB I/F

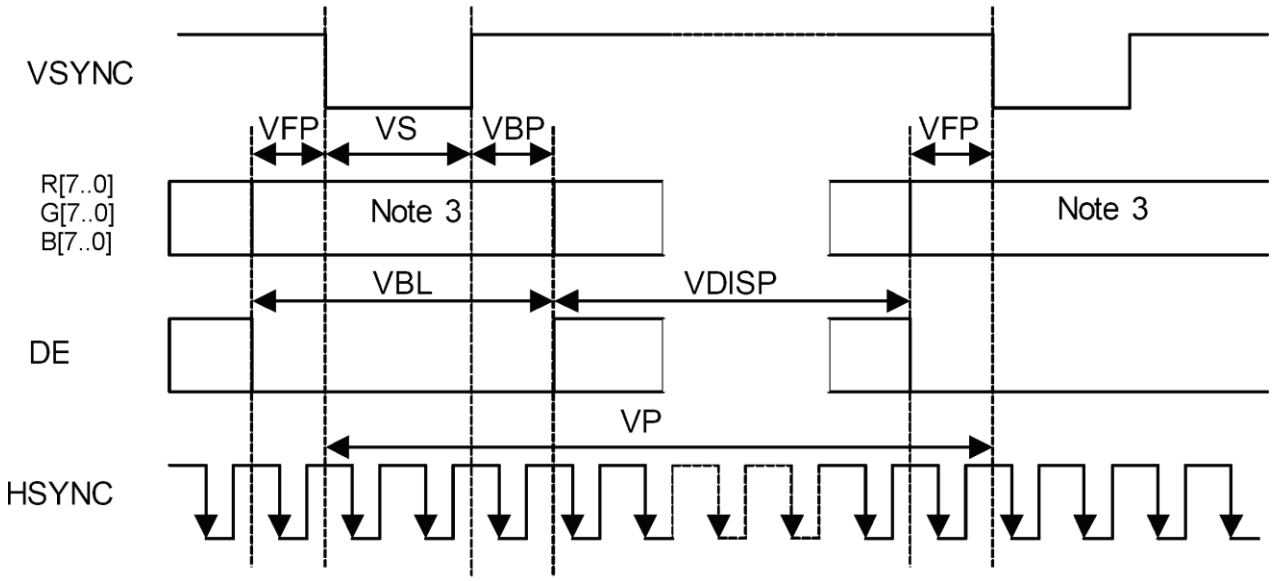


Figure7.1-2 Vertical Timings for RGB I/F

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Vertical cycle	VP	-	806	-	810	Line
Vertical low pulse width	VS	-	2	-	4	Line
Vertical front porch	VFP	-	2	-	4	Line
Vertical back porch	VBP	-	2	-	4	Line
Vertical data start point	-	VS+VBP	4	-	8	Line
Vertical blanking period	VBL	VS+VBP+VFP	6	-	10	Line
Vertical active area	-	VDISP	-	800	-	Line
Vertical Refresh rate	VRR	-	50	-	70	Hz
Vertical Refresh rate	VRR	-	50	-	70	Hz

Note: (1) Signal rise and fall times are equal to or less than 20 ns.

(2) Input signals are measured by 0.30 x VDDI for low state and 0.70 x VDDI for high state.

(3) Data lines can be set to “High” or “Low” during blanking time – Don’t care.

Horizontal Timings for RGB I/F

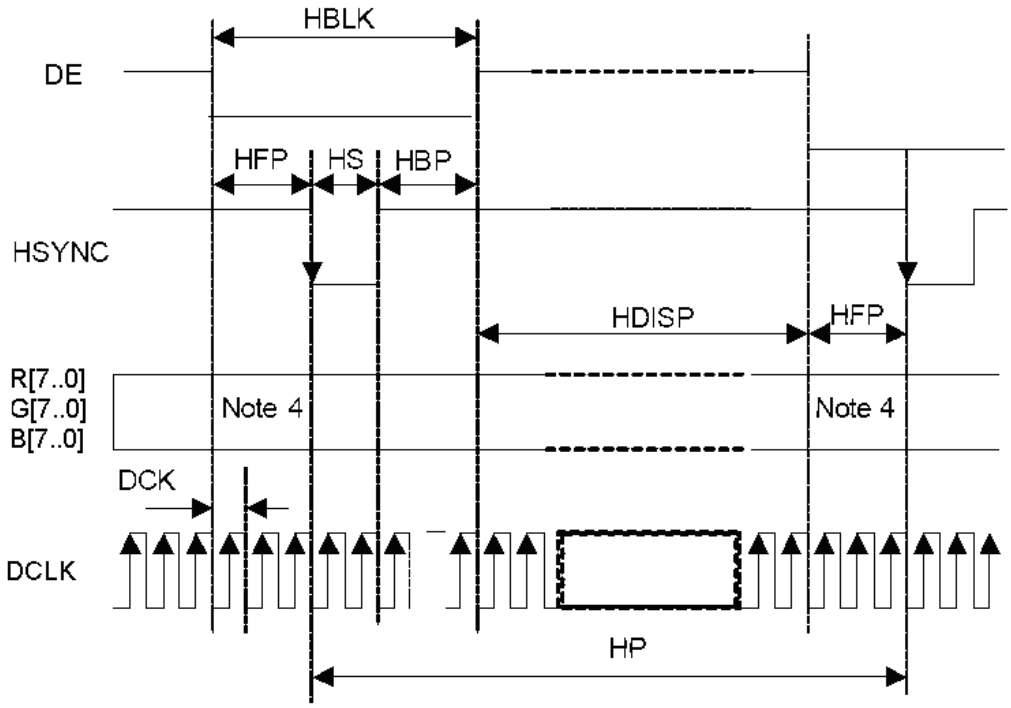
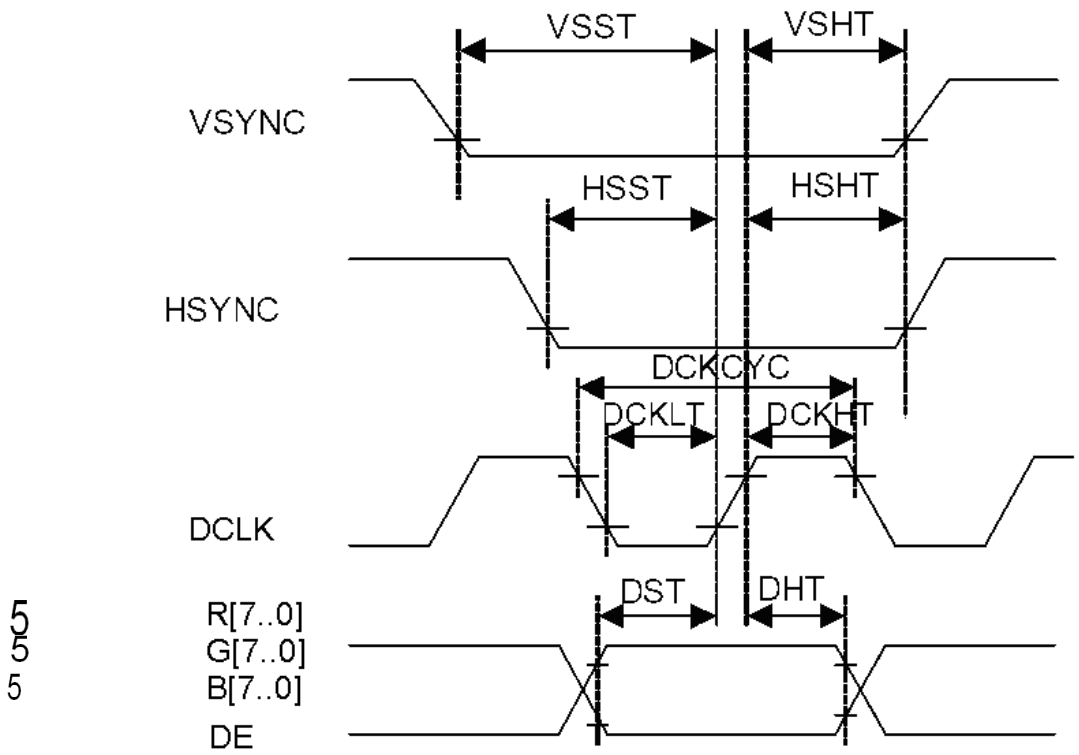


Figure 7.2-3 Horizontal Timing for RGB I/F

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
HSYNC cycle	HP	Note 3	504	-	568	DCLK
HSYNC low pulse width	HS	-	5	-	256	DCLK
Horizontal back porch	HBP	-	5	-	256	DCLK
Horizontal front porch	HFP	-	5	-	256	DCLK
Horizontal data start point	-	HS+HBP	19	-	83	DCLK
			700	-	-	ns
Horizontal blanking period	HBLK	HS+HBP+HFP	24	-	88	DCLK
Horizontal active area	HDISP	-	-	480	-	DCLK
Pixel clock frequency When RGB I/F is running	DCLK	VRR = Min. 50 Hz – Max. 70 Hz	20.3	-	32.2	MHz
			31	-	49.2	ns

Note: (1) Signal rise and fall times are equal to or less than 20 ns.
(2) Input signals are measured by 0.30 x VDDI for low state and 0.70 x VDDI for high state.
(3) HP is multiples of eight DCLK.
(4)Data lines can be set to “High” or “Low” during blanking time – Don’t care.
(5) B3h Command (09h): DPL=1, the data is read on the falling edge of DCLK signal.

7.3 RGB interface General Timing

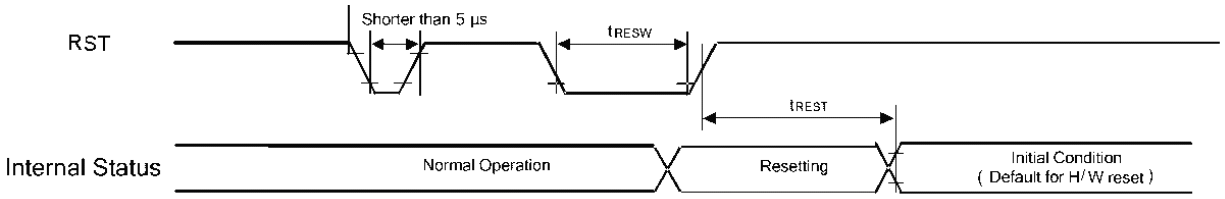


General Timings for RGB I/F

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Vertical sync. Setup time	VSST	-	5	-	-	ns
Vertical sync. Hold time	VSHT	-	5	-	-	ns
Horizontal sync. Setup time	HSST	-	5	-	-	ns
Horizontal sync. Hold time	HSHT	-	5	-	-	ns
Pixel clock cycle When RGB I/F is running	DCKCYC	VRR = Min. 50 Hz Max. 70 Hz	31 (Note3)	-	49.2 (Note 4)	ns
Pixel clock low time	DCKLT	-	5	-	-	ns
Pixel clock high time	DCKHT	-	5	-	-	ns
Data setup time DB[23:0]	DST	-	5	-	-	ns
Data Hold time DB[23:0]	DHT	-	5	-	-	ns

Note: (1) Signal rise and fall times are equal to or less than 20 ns.
(2) 32.2 MHz
(3) 20.3 MHz
(4) Input signals are measured by 0.30 x VDDIO for low state and 0.70 x VDDIO for high state.

7.4 Reset Input Timing



Write to Read and Read to Write Timing

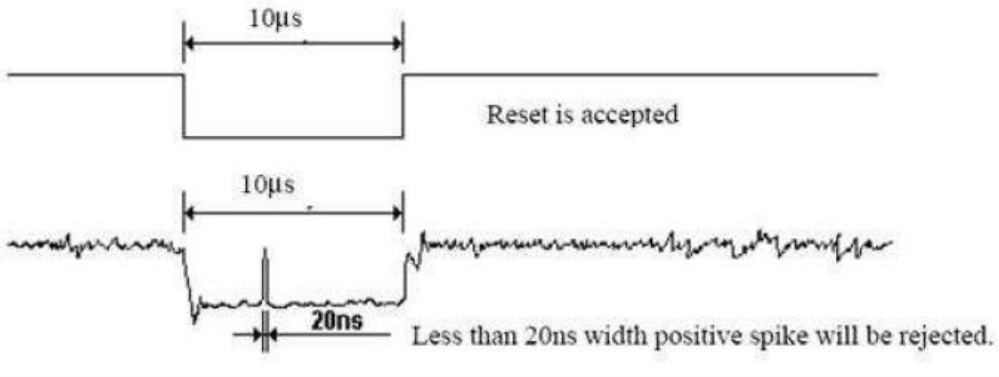
Symbol	Parameter	Related Pins	Min.	Typ.	Max.	Note	Unit
tRESW	Reset low pulse width	RST	10	-	-	-	µs
tREST	Reset complete time	-	-	-	5	When reset applied during STB mode	ms
		-		-	120	When reset applied during STB mode	ms

Note:

1. Spike due to an electrostatic discharge on RST line does not cause irregular system reset according to the table below.

NRESET Pulse	Action
Shorter than 5 µ	Reset Rejected
Longer than 10 µs	Reset
Between 5 µs and 10 µs	Reset Start

2. During the resetting period, the display will be blanked (The display is entering blanking sequence, which maximum time is 120 ms, when Reset Starts in Sleep Out –mode. The display remains the blank state in Sleep In –mode) and then returns to Default condition for H/W reset.
3. During Reset Complete Time, ID2 value in OTP will be latched to internal register during this period. This loading is done every time when there is H/W reset complete time (tREST) within 5ms after a rising edge of RST.
4. Spike Rejection also applies during a valid reset pulse as shown below:



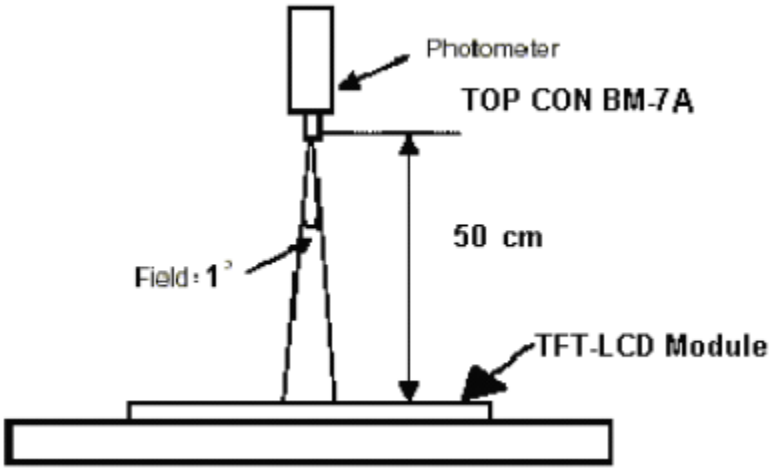
5. When Reset is applied during Sleep In Mode.
6. When Reset is applied during Sleep Out Mode.
7. It is necessary to wait 5msec after releasing RST before sending commands. Also Sleep Out command cannot be sent for 120msec.

8. OPTICAL CHARACTERISTIC

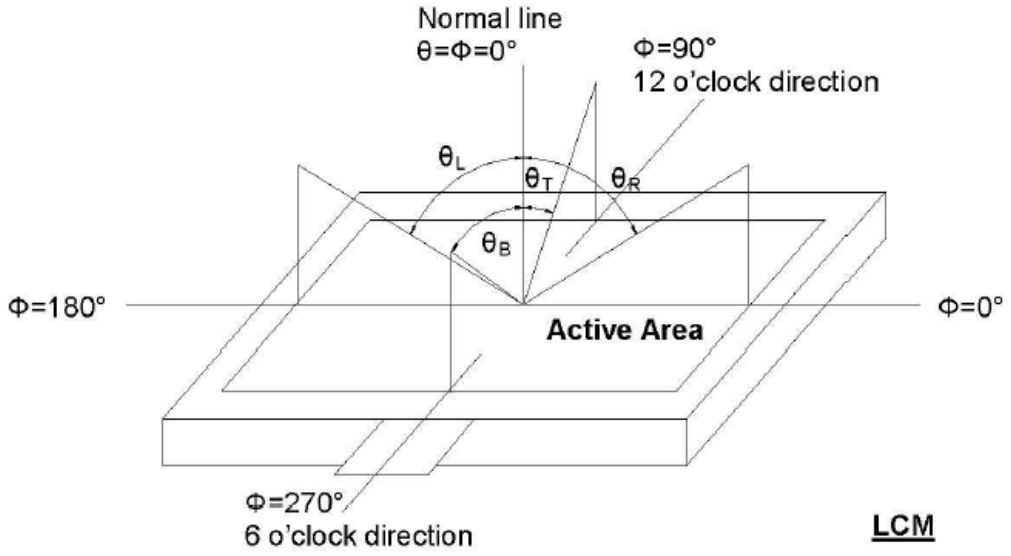
Parameter		Symbol	Condition	MIN.	TYP.	MAX.	Unit	Remarks
Response time		Tr+Tf	Center θ=Φ=0°	-	(T.B.D.)	-	ms	Note 1,6
Contrast Ratio		CR	At the center point of A.A	-	(T.B.D.)	-		Note 1,4
Viewing Angle		θL	Center CR≥10	70	80	-	deg	Note 1,2
		θR		70	80	-		
		θT		70	80	-		
		θB		70	80	-		
Brightness		L	Center θx=θy =0°	800	1000	-	cd/㎡	Note 1,3
Color chromaticity (CIE1931)	White	x	Normal θx=θy =0°	TYP-0.05	(T.B.D.)	TYP-0.05		Note 1,7
		y			(T.B.D.)			

The following optical specifications shall be measured in a darkroom or equivalent state (ambient luminance ≤1 lux, and at room temperature). The operation temperature is 25°C±2°C and LED Backlight Current IL=20mA. The measurement method is shown in Note1.

Note 1: The method of optical measurement:



Note 2: Definition of viewing angle range

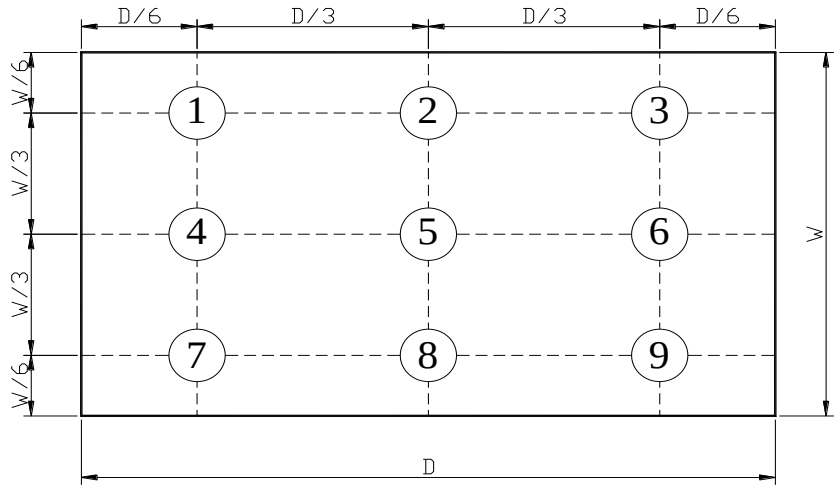


Note 3: Measured at the center area of the panel and at the viewing angle of the θx=θy =0°

Note 4: Definition of Contrast Ratio (CR):

$$CR = \frac{\text{Luminance with all pixels in white state}}{\text{Luminance with all pixels in Black state}}$$

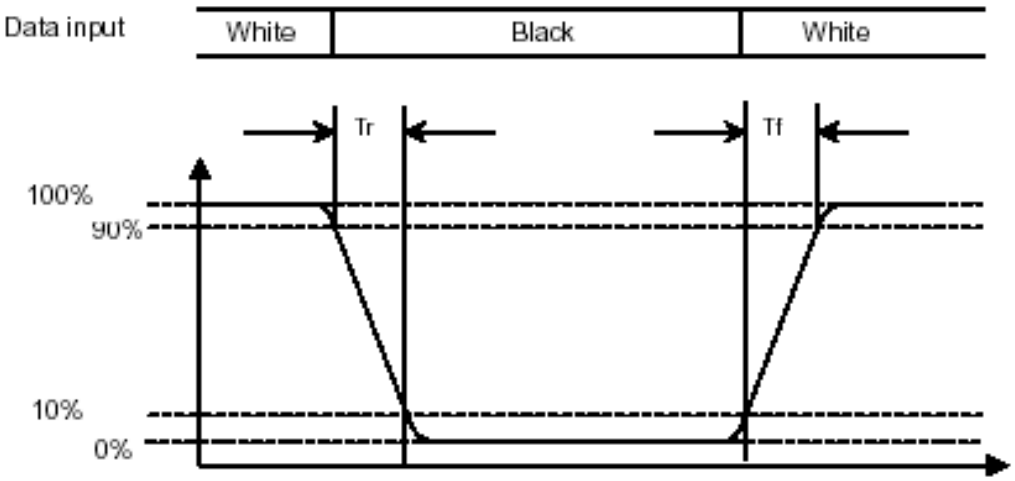
Note 5: Definition of Brightness Uniformity (B-uni):



$$\text{B-uni} = \frac{\text{Minimum luminance of 9 points}}{\text{Maximum luminance of 9points}}$$ (Note 5).

Note 6: Definition of Response Time:

The Response Time is set initially by defining the “Rising Time (Tr)” and the “Falling Time (Tf)” respectively. Tr and Tf are defined as following figure.



Note 7: The color coordinates (x_w,y_w),(x_R,y_R),(x_G,y_G),and (x_B,y_B) are obtained with all pixels in the viewing field at white, red, green, and blue states, respectively.

9. PIN CONNECTIONS

TFT-LCD PIN CONNECTIONS

Pin No	Symbol	Description	Remark
1	VDDI	Power supply for interface system	
2	VDD	Power supply for analog system	
3	VDD		
4	GND	Ground	
5	RESX	This signal will reset the device and must be applied to properly initialize the chip. Signal is active low.	
6	SDI	Serial data input signal.	
7	SDO	Serial data output signal.	
8	SCL	Serial data clock signal.	
9	CSX	Chip select input pin (“Low” enable).	
10	DCLK	Pixel clock signal.	
11	DE	Data enable signal.	
12	VSYNC	Vertical sync.	
13	HSYNC	Horizontal sync.	
14	GND	Ground	
15	DB0		
16	DB1	RGB data bus.	
17	DB2		
18	DB3		
19	DB4		
20	DB5		
21	DB6		
22	DB7		
23	GND	Ground	
24	DB8	RGB data bus.	
25	DB9		
26	DB10		
27	DB11		
28	DB12		
29	DB13		
30	DB14		
31	DB15		
32	GND	Ground	
33	DB16	RGB data bus.	
34	DB17		
35	DB18		
36	DB19		
37	DB20		
38	DB21		

39	DB22		
40	DB23		
41	GND	Ground	
42	LEDA	POWER SUPPLY FOR LED+	
43	LEDA		
44	LEDK	POWER SUPPLY FOR LED-	
45	LEDK		

10. INTERFACE PIXEL FORMAT

The 4.21” round LCD supports RGB interface that is used 3 wire serial data transfer interface to set pixel format in 16, 18 or 24 bit RGB.

16-BIT RGB

DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
			R4	R3	R2	R1	R0			G5	G4	G3	G2	G1	G0				B4	B3	B2	B1	B0

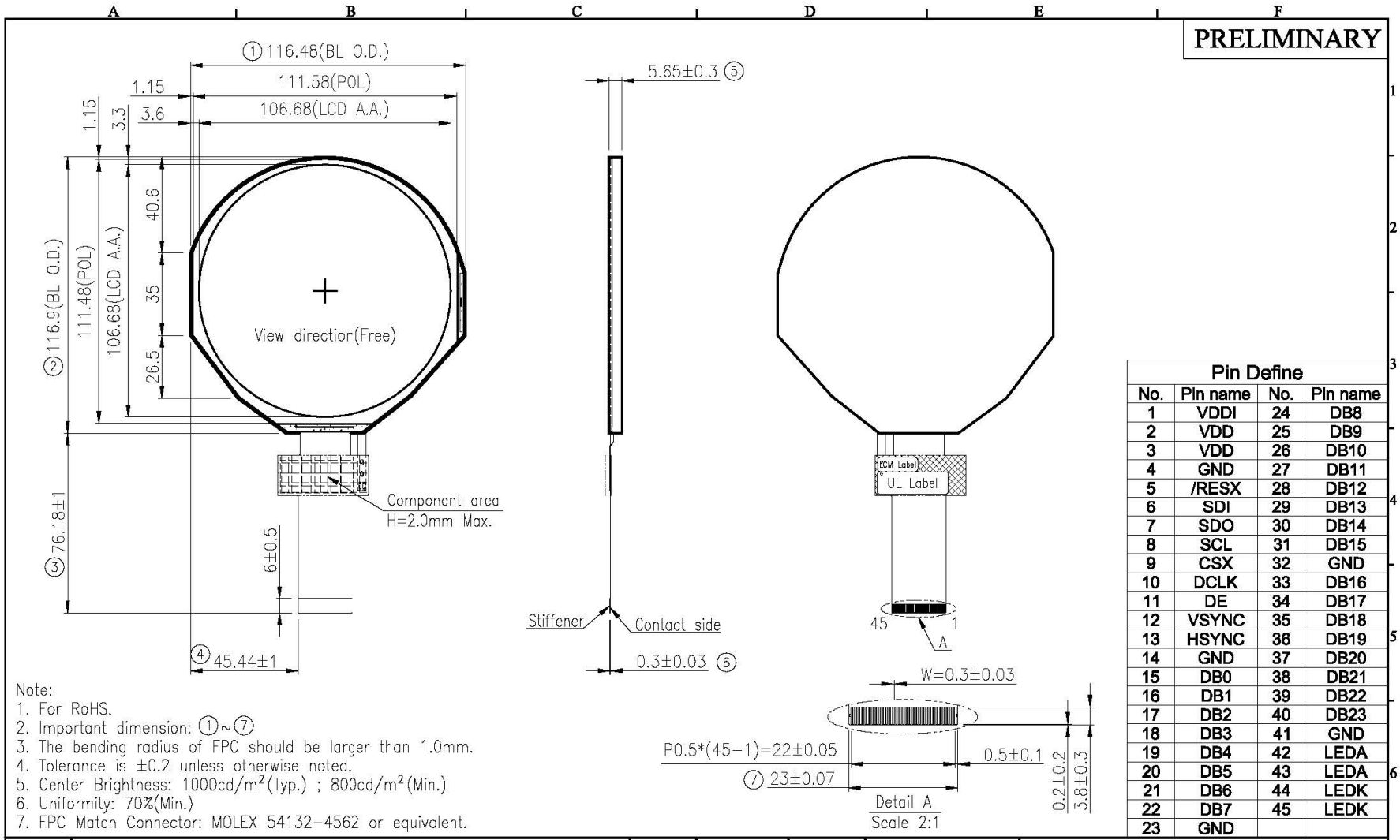
18-BIT RGB

DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
		R5	R4	R3	R2	R1	R0			G5	G4	G3	G2	G1	G0			B5	B4	B3	B2	B1	B0

24-BIT RGB

DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
R7	R6	R5	R4	R3	R2	R1	R0	G7	G6	G5	G4	G3	G2	G1	G0	B7	B6	B5	B4	B3	B2	B1	B0

11. OUTLINE DRAWING



Note:
1. For RoHS.
2. Important dimension: ①~⑦
3. The bending radius of FPC should be larger than 1.0mm.
4. Tolerance is ±0.2 unless otherwise noted.
5. Center Brightness: 1000cd/m²(Typ.) ; 800cd/m²(Min.)
6. Uniformity: 70%(Min.)
7. FPC Match Connector: MOLEX 54132-4562 or equivalent.

Pin Define

No.	Pin name	No.	Pin name
1	VDDI	24	DB8
2	VDD	25	DB9
3	VDD	26	DB10
4	GND	27	DB11
5	/RESX	28	DB12
6	SDI	29	DB13
7	SDO	30	DB14
8	SCL	31	DB15
9	CSX	32	GND
10	DCLK	33	DB16
11	DE	34	DB17
12	VSYNC	35	DB18
13	HSYNC	36	DB19
14	GND	37	DB20
15	DB0	38	DB21
16	DB1	39	DB22
17	DB2	40	DB23
18	DB3	41	GND
19	DB4	42	LEDA
20	DB5	43	LEDA
21	DB6	44	LEDK
22	DB7	45	LEDK
23	GND		

AUTH	DESCRIPTION	DATE	APPROVED
REVISIONS			

DATE:	2017/07/11
DRAWN:	
CHECK:	
APPROVE:	

LCM OUTLINE DIMENSION

DWG. NO.	4.2" LCM
UNITS M M	REV.
SCALE Scale	SHEET 1 OF 1

US Micro Products ENGINEERED DISPLAY SOLUTIONS