US Micro Products
ENGINEERED DISPLAY SOLUTIONS

TFT SPECIFICATION

Part Number	USMP-T024-024032MEG-A1
Size	2.4"
Resolution	240 x 320
Brightness	400 cd/m²
Contrast	500:1
Viewing Angle	80/80/80/80
Operating Temp.	-20 ~ 70°C

FOR ADDITIONAL INFORMATION
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Issue Date	Approved by (customer use)	Checked by	Prepared by

Revision History

Revision	Date	Originator	Detail	Remarks
1.0	2018.04.21	ZDT	Initial Release	
1.1	2018.07.18	ZDT	Modify Weight Modify Current Consumption Modify Chromaticity Transmissive Modify Outline Drawing	P4 P5 P6 P28
1.2	2018.07.23	ZDT	Modify Optical Characteristics Modify Reliability Specification	P6 P24
1.3	2018.09.28	ZDT	Modify Optical Characteristics Modify Reliability Specification	P6 P24
1.4	2018.11.01	ZDT	Modify details	P9
1.5	2019.03.04	ZDT	Modify Interface Pins Definition Modify Outline Drawing(F)	P9/P11 P28

Table of Contents

1. General Description

The specification is a transmissive type color active matrix liquid crystal display (LCD) which uses amorphous thin film transistor (TFT) as switching devices. This product is composed of a TFT-LCD panel, driver Ics and a backlight unit.

2. Module Parameter

Features	Details	Unit
Display Size(Diagonal)	2.4”	
LCD type	IPS TFT	
Display Mode	Transmissive /Normally black	
Resolution	240 RGB x320	Pixels
View Direction	FULL VIEW	Best Image
Module Outline	41.87 (H) x 59.35 (V) x 2.6 (T) (Note1)	mm
Active Area	36.72(H) x 48.96(V)	mm
Pixel Size	153(H) x 153(V)	um
Pixel Arrangement	RGB Vertical Stripe	
Display Colors	262K	
Interface	RGB 3/4 -wire SPI 8/9/16/18 bit for i80 system	
With or without touch panel	Without	
Driver IC	ILI9341V	-
Operating Temperature	**-20～70**	ºC
Storage Temperature	**-30～80**	ºC
Weight	11	g

Note 1: Exclusive hooks, posts, FFC/FPC tail etc.

3. Absolute Maximum Ratings

V_{SS}=0V, Ta=25ºC

Item	Symbol	Min.	Max.	Unit
Supply Voltage	VDD	-0.3	4.6	V
Storage temperature	T_{STG}	**-30**	**+80**	ºC
Operating temperature	T_{OP}	**-20**	**+70**	ºC

Note 1: If Ta below 50ºC, the maximal humidity is 90%RH, if Ta over 50ºC, absolute humidity should be less than 60%RH.

Note 2: The response time will be extremely slow when the operating temperature is around -10℃, and the back ground will become darker at high temperature operating.

4. DC Characteristics

Item		Symbol	Min.	Typ.	Max.	Unit
Power supply		VDD	2.5	2.8	3.3	V
Logic Low input voltage		V_{IL}	GND	-	0.3*VDD	V
Logic High input voltage		V_{IH}	0.7*VDD	-	VDD	V
Logic Low output voltage		V_{OL}	GND	-	0.2*VDD	V
Logic High output voltage		V_{OH}	0.8*VDD	-	VDD	V
Current Consumption All white	Logic	I_{CC+} I_{IN}	-	9	-	mA
	Analog					

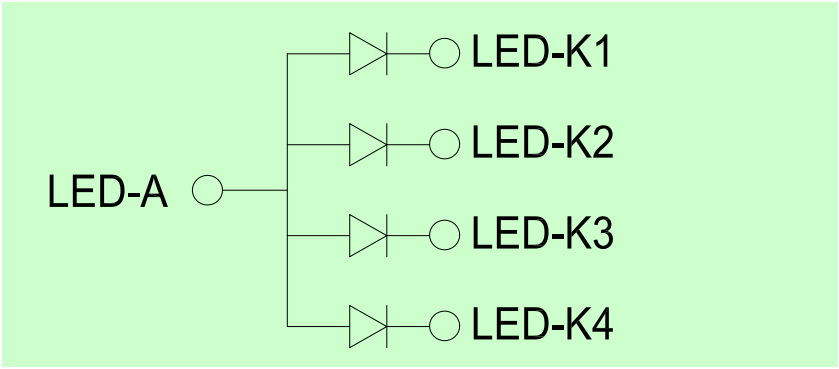
5. Backlight Characteristic

5.1. Backlight Characteristics

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Forward Voltage	V_F	Ta=25 ºC, I_F=18mA/LED	2.8	**3.2**	3.4	V
Forward Current	I_F	Ta=25 ºC, V_F=3.2V/LED	-	**72**	-	mA
Power dissipation	P_D		-	**230.4**	-	mW
Uniformity	Avg		-	80	-	%
LED working life(25℃)	-		-	30,000	-	Hrs
Drive method	**Constant current**					
LED Configuration	4 White LEDs in parallel					

Note1：LED life time defined as follows: The final brightness is at 50% of original brightness.
The environmental conducted under ambient air flow, at Ta=25±2 ºC,60%RH±5%, I_F=20mA/LED.

5.2. Backlighting circuit



6. Optical Characteristics

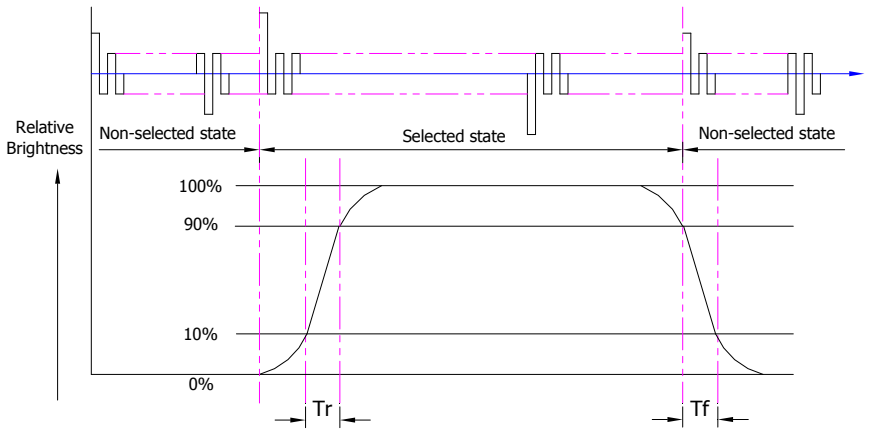
6.1. Optical Characteristics

Ta=25ºC, VDD=2.8V

	Item		Symbol	Condition	Specification			Unit
					Min.	Typ.	Max.	
Backlight On (Transmissive Mode)	Luminance on TFT(I_f =18mA/LED)		Lv	Normally viewing angle θX = φY =0º	**340**	**400**	-	cd/m²
	Contrast ratio(See 6.3)		CR		400	500	-	
	Response time (See 6.2)		TR+TF		-	35	45	ms
	Chromaticity Transmissive (See 6.5)	Red	XR		**0.591**	**0.641**	**0.691**	
			YR		**0.279**	**0.329**	**0.379**	
		Green	XG		**0.261**	**0.311**	**0.361**	
			YG		**0.580**	**0.630**	**0.680**	
		Blue	XB		**0.092**	**0.142**	**0.192**	
			YB		**0.009**	**0.059**	**0.109**	
		White	XW		**0.242**	**0.292**	**0.342**	
			YW		**0.287**	**0.337**	**0.387**	
	Viewing Angle (See 6.4)	Horizontal	θX+	Center CR≥10	**-**	**80**	-	Deg.
			θX-		**-**	**80**	-	
		Vertical	φY+		**-**	**80**	-	
			φY-		**-**	**80**	-	
	NTSC Ratio(Gamut)				-	70	-	%

6.2. Definition of Response Time

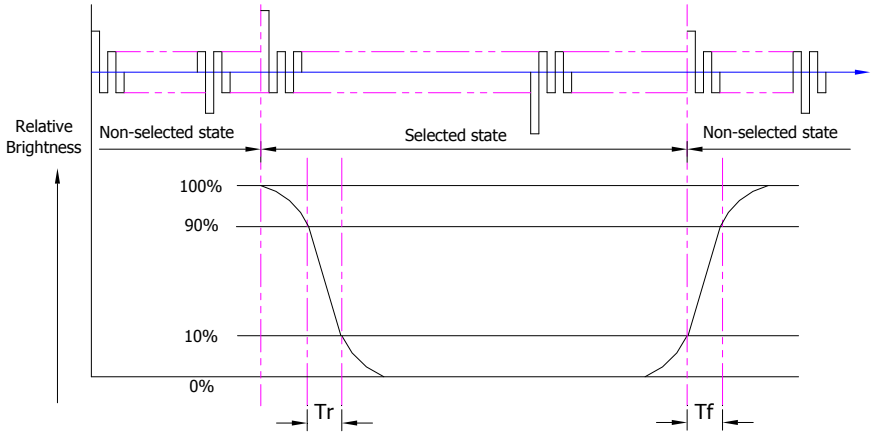
6.2.1. Normally Black Type (Negative)



Tr is the time it takes to change form non-selected stage with relative luminance 10% to selected state with relative luminance 90%;
Tf is the time it takes to change from selected state with relative luminance 90% to non-selected state with relative luminance 10%.

Note: Measuring machine: LCD-5100

6.2.2. Normally White Type (Positive)



Tr is the time it takes to change form non-selected stage with relative luminance 90% to selected state with relative luminance 10%;

Tf is the time it takes to change from selected state with relative luminance 10% to non-selected state with relative luminance 90%;

Note: Measuring machine: LCD-5100 or EQUI

6.3. Definition of Contrast Ratio

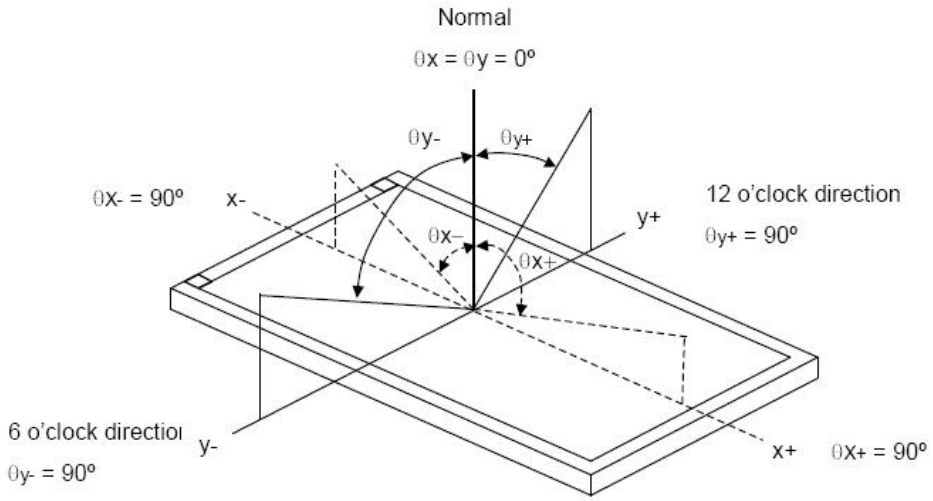
Contrast is measured perpendicular to display surface in reflective and transmissive mode.

The measurement condition is:

Measuring Equipment	Eldim or Equivalent
Measuring Point Diameter	3mm//1mm
Measuring Point Location	Active Area centre point
Test pattern	A: All Pixels white
	B: All Pixel black
Contrast setting	Maximum

Definitions: CR (Contrast) = Luminance of White Pixel / Luminance of Black Pixel

6.4. Definition of Viewing Angles



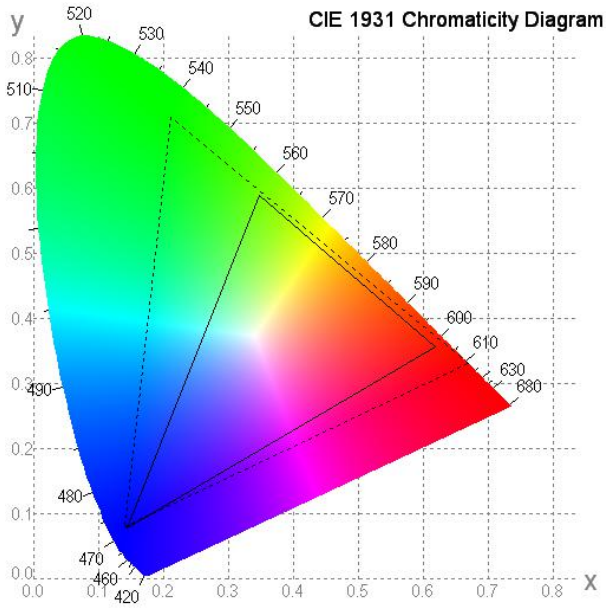
Measuring machine: LCD-5100 or EQUI

6.5. Definition of Color Appearance

R,G,B and W are defined by (x, y) on the IE chromaticity diagram

NTSC=area of RGB triangle/area of NTSC triangleX100%

Measuring picture: Red, Green, Blue and White (Measuring machine: BM-7)



6.6. Definition of Surface Luminance, Uniformity and Transmittance

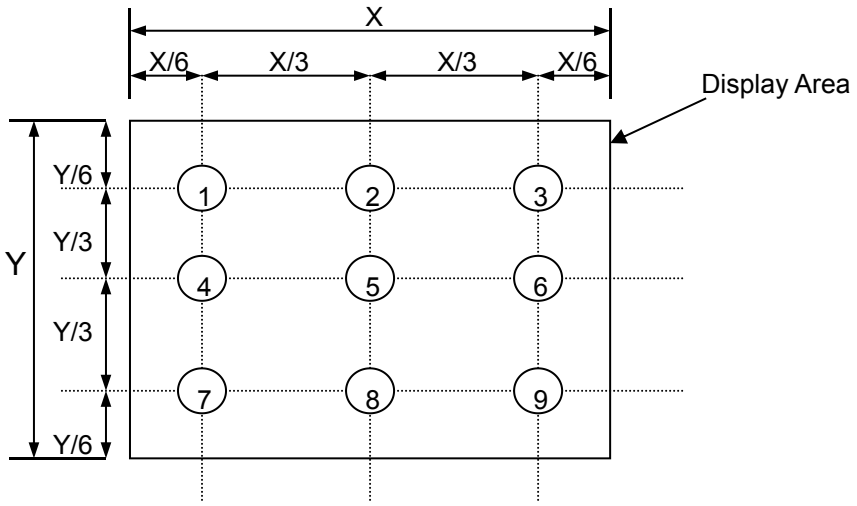
Using the transmissive mode measurement approach, measure the white screen luminance of the display panel and backlight.

6.6.1. Surface Luminance: L_V = average (L_{P1}:L_{P9})

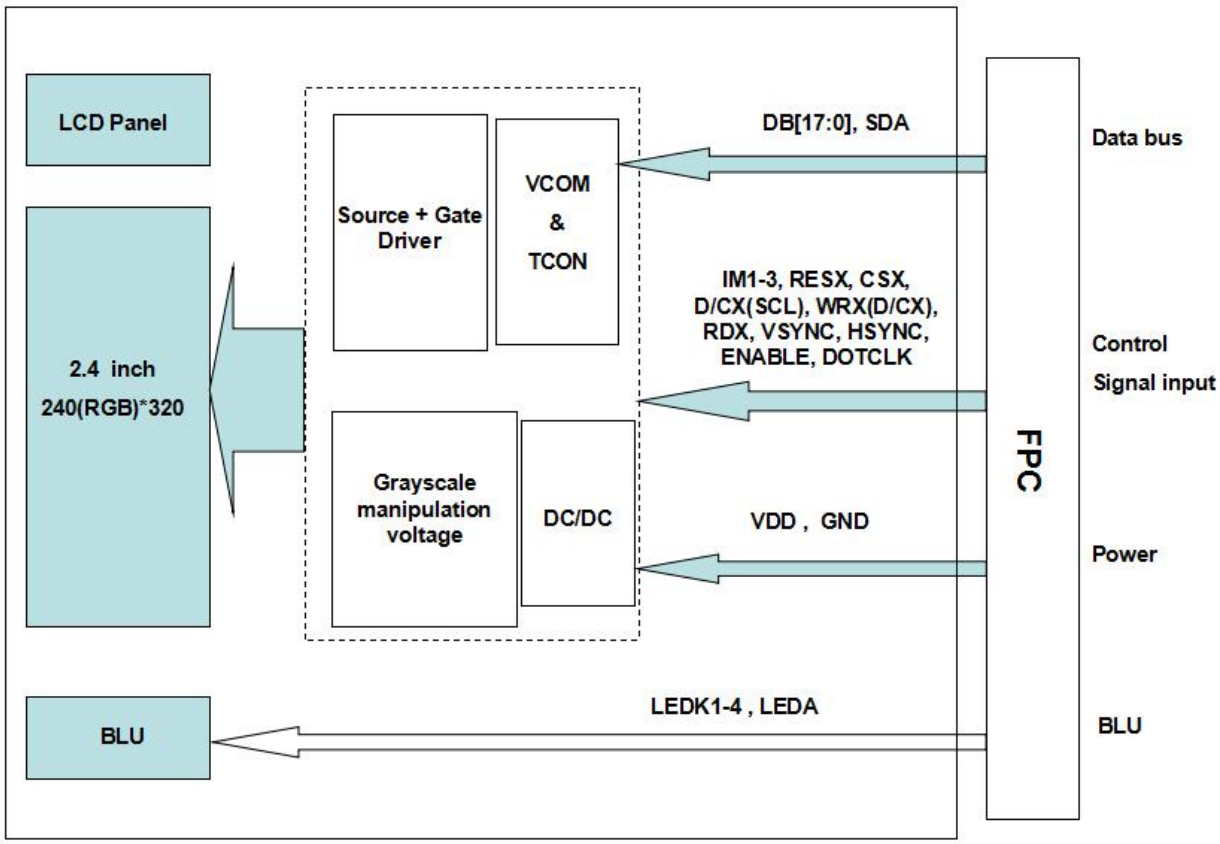
6.6.2. Uniformity = Minimal (L_{P1}:L_{P9}) / Maximal (L_{P1}:L_{P9}) * 100%

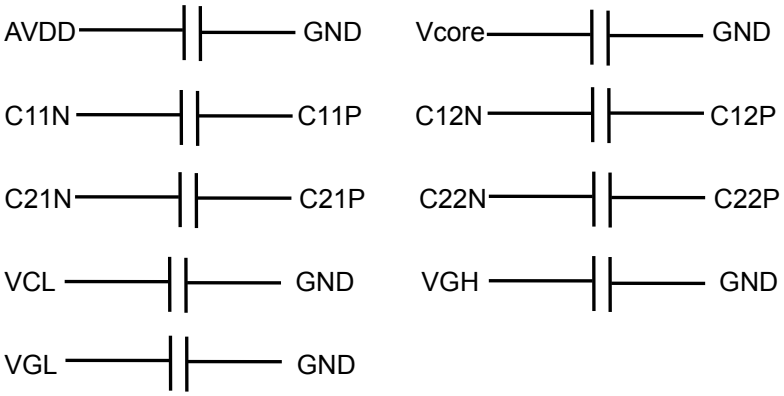
6.6.3. Transmittance = L_V on LCD / L_V on Backlight * 100%

Note: Measuring machine: BM-7



7. Block Diagram and Power Supply





8. Interface Pins Definition

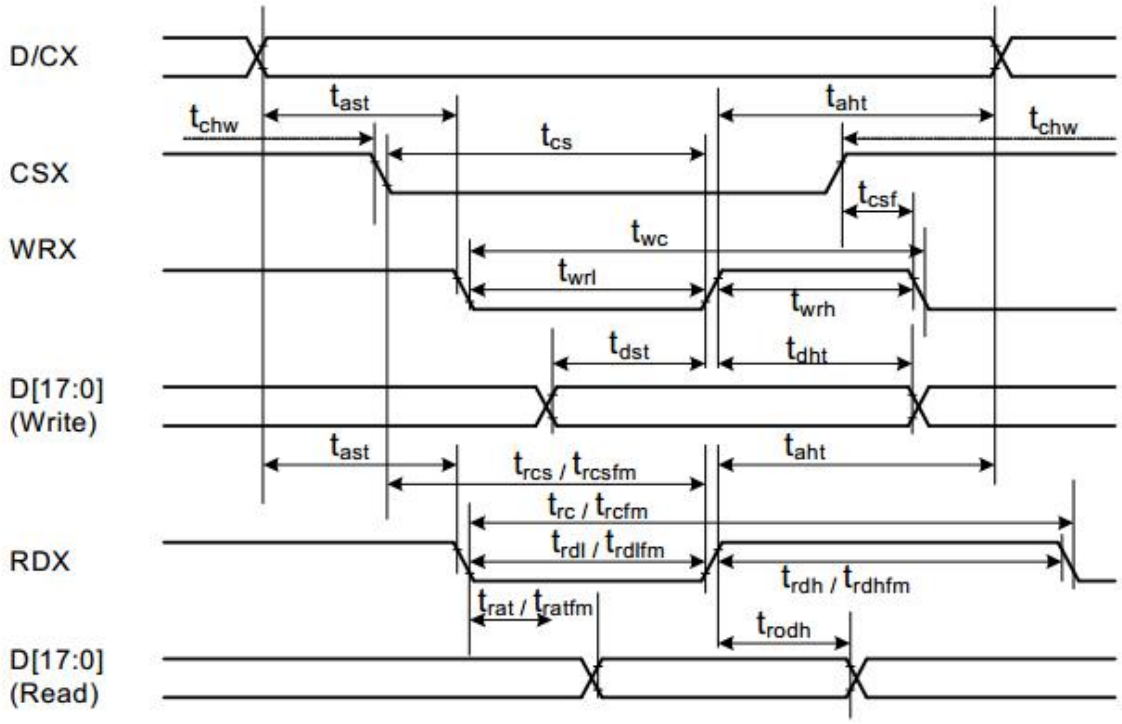
Connector: FH23-61S-0.3SHW

No.	Symbol	Function	Remark
1	GND	Ground	
2	GND	Ground	
3	LEDK4	Led cathode	
4	LEDK3	Led cathode	
5	LEDK2	Led cathode	
6	LEDK1	Led cathode	
7	LEDA	Led anode	
8	C22P	Connect the charge-pumping capacitor for generating VGH, VGL level	
9	C22N	Connect the charge-pumping capacitor for generating VGH, VGL level	
10	C21P	Connect the charge-pumping capacitor for generating VGH, VGL level	
11	C21N	Connect the charge-pumping capacitor for generating VGH, VGL level	
12	VGH	Power setting capacitor connect pin.	
13	VGL	Power setting capacitor connect pin.	
14	AVDD	Analog Power supply	
15	C12P	Connect the charge-pumping capacitor for generating AVDD level	
16	C12N	Connect the charge-pumping capacitor for generating AVDD level	
17	C11P	Connect the charge-pumping capacitor for generating AVDD level	
18	C11N	Connect the charge-pumping capacitor for generating AVDD level	
19	GND	Ground	
20	GND	Ground	
21	GND	Ground	
22 23 24 25	IM3 IM2 IM1 IM0	**IM3 / IM2 / IM1 / IM0 / Interface mode** 0 0 0 0 80 MCU 8-bit bus interface Ⅰ 0 0 0 1 80 MCU 16-bit bus interface Ⅰ 0 0 1 0 80 MCU 9-bit bus interface Ⅰ 0 0 1 1 80 MCU 18-bit bus interface Ⅰ 0 1 0 1 3-wire 9-bit data serial interface Ⅰ 0 1 1 0 4-wire 8-bit data serial interface Ⅰ 1 0 0 0 80 MCU 16-bit bus interface Ⅱ 1 0 0 1 80 MCU 8-bit bus interface Ⅱ 1 0 1 0 80 MCU 18-bit bus interface Ⅱ 1 0 1 1 80 MCU 9-bit bus interface Ⅱ 1 1 0 1 3-wire 9-bit data serial interface Ⅱ 1 1 1 0 4-wire 8-bit data serial interface Ⅱ	
26	RESX	Reset signal	
27	CSX	Chip select signal	
28	D/CX(SCL)	(D/CX): This pin is used to select “Data or Command” in the parallel	

		interface. When DCX = 1, data is selected. When DCX = 0, command is selected. (SCL): This pin is used as the serial interface clock in 3-wire 9-bit/4-wire 8-bit serial data interface.	
29	WRX(D/CX)	(WRX) - 8080- /8080 Ⅰ -Ⅱ system: Serves as a write signal and writes data at the rising edge. (D/CX) - 4-line system: Serves as the selector of command or parameter.	
30	RDX	Read signal	
31	VSYNC	Vertical Sync input.	
32	HSYNC	Horizontal Sync input.	
33	ENABLE	Data Enable signal.	
34	DOTCLK	Clock signal.	
35	SDA	Serial data.	
36	DB0	Data bus	
37	DB1	Data bus	
38	DB2	Data bus	
39	DB3	Data bus	
40	DB4	Data bus	
41	DB5	Data bus	
42	DB6	Data bus	
43	DB7	Data bus	
44	DB8	Data bus	
45	DB9	Data bus	
46	DB10	Data bus	
47	DB11	Data bus	
48	DB12	Data bus	
49	DB13	Data bus	
50	DB14	Data bus	
51	DB15	Data bus	
52	DB16	Data bus	
53	DB17	Data bus	
54	TE	Tearing effect output pin	
55	VDD	Power supply	
56	VDD	Power supply	
57	VDD	Power supply	
58	Vcore	Regulated Low voltage level for interface circuits	
59	VCL	VCL pad. Place a 1uF/10V capacitor to GND.	
60	GND	Ground	
61	GND	Ground	

9. AC Characteristics

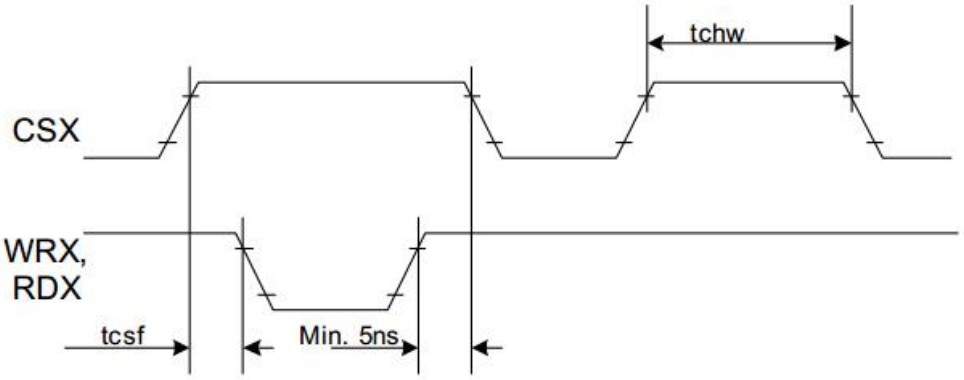
1）Display Parallel 18/16/9/8-bit Interface Timing Characteristics (8080- Ⅰ system)



Signal	Symbol	Parameter	min	max	Unit	Description
DCX	tast	Address setup time	0	-	ns	
	taht	Address hold time (Write/Read)	0	-	ns	
CSX	tchw	CSX "H" pulse width	0	-	ns	
	tcs	Chip Select setup time (Write)	15	-	ns	
	trcs	Chip Select setup time (Read ID)	45	-	ns	
	trcsfm	Chip Select setup time (Read FM)	355	-	ns	
	tcsf	Chip Select Wait time (Write/Read)	10	-	ns	
WRX	twc	Write cycle	66	-	ns	
	twrh	Write Control pulse H duration	15	-	ns	
	twrl	Write Control pulse L duration	15	-	ns	
RDX (FM)	trcfm	Read Cycle (FM)	450	-	ns	
	trdhfm	Read Control H duration (FM)	90	-	ns	
	trdlfm	Read Control L duration (FM)	355	-	ns	
RDX (ID)	trc	Read cycle (ID)	160	-	ns	
	trdh	Read Control pulse H duration	90	-	ns	
	trdl	Read Control pulse L duration	45	-	ns	
D[17:0], D[15:0], D[8:0], D[7:0]	tdst	Write data setup time	10	-	ns	For maximum CL=30pF For minimum CL=8pF
	tdht	Write data hold time	10	-	ns	
	trat	Read access time	-	40	ns	
	tratfm	Read access time	-	340	ns	
	trod	Read output disable time	20	80	ns	

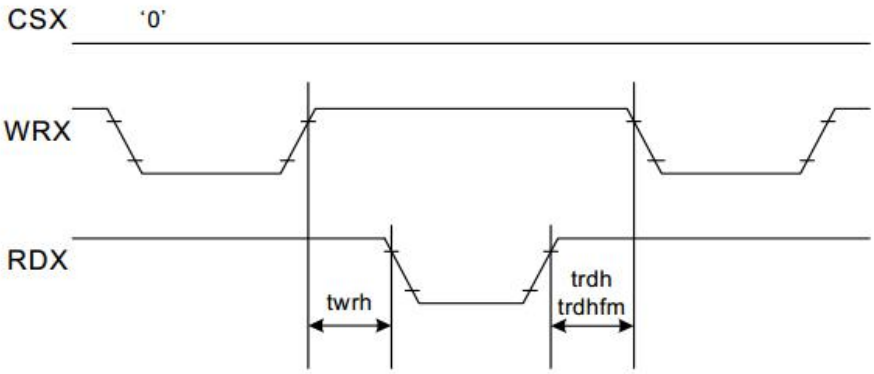
Note: Ta = -30 to 70 °C, VDDI=1.65V to 3.3V, VCI=2.5V to 3.3V, VSS=0V

CSX timings :



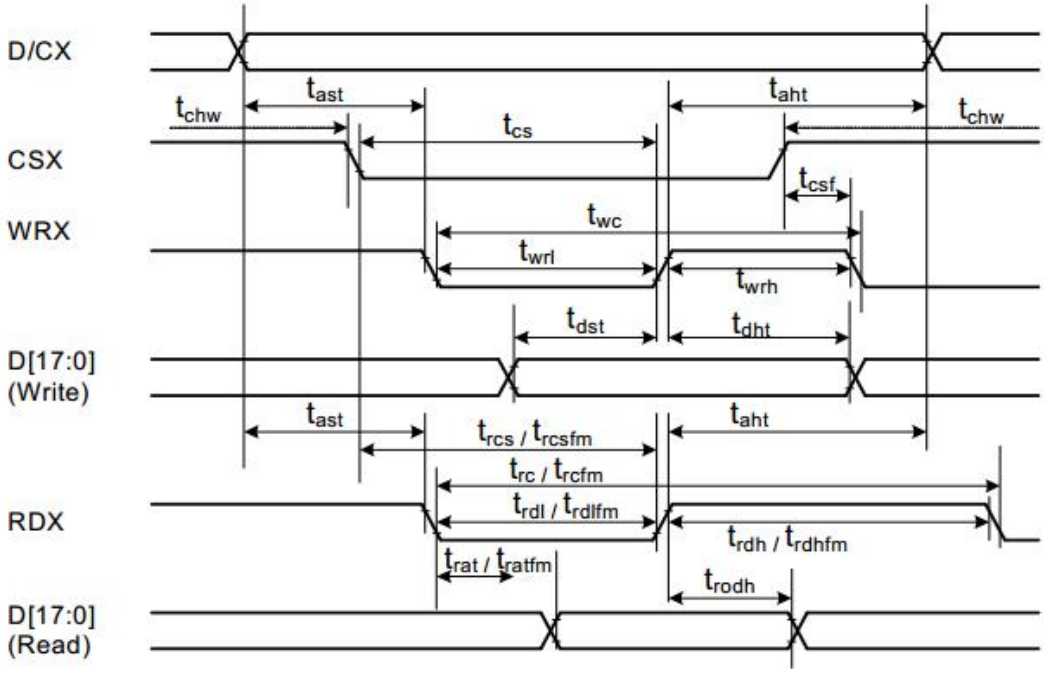
Note: Logic high and low levels are specified as 30% and 70% of VDDI for Input signals.

Write to read or read to write timings:



Note: Logic high and low levels are specified as 30% and 70% of VDDI for Input signals.

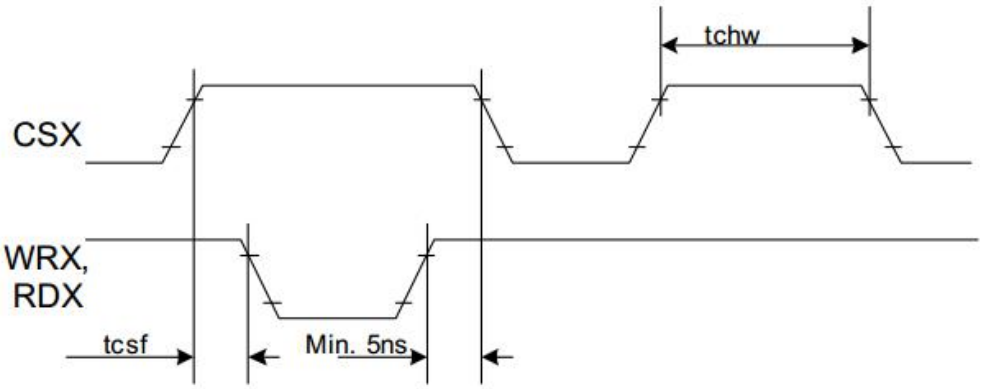
2）Display Parallel 18/16/9/8-bit Interface Timing Characteristics(8080-Ⅱsystem)



Signal	Symbol	Parameter	min	max	Unit	Description
DCX	tast	Address setup time	0	-	ns	
	taht	Address hold time (Write/Read)	0	-	ns	
CSX	tchw	CSX "H" pulse width	0	-	ns	
	tcs	Chip Select setup time (Write)	15	-	ns	
	trcs	Chip Select setup time (Read ID)	45	-	ns	
	trcsfm	Chip Select setup time (Read FM)	355	-	ns	
	tcsf	Chip Select Wait time (Write/Read)	10	-	ns	
WRX	twc	Write cycle	66	-	ns	
	twrh	Write Control pulse H duration	15	-	ns	
	twrl	Write Control pulse L duration	15	-	ns	
RDX (FM)	trcfm	Read Cycle (FM)	450	-	ns	
	trdhfm	Read Control H duration (FM)	90	-	ns	
	trdlfm	Read Control L duration (FM)	355	-	ns	
RDX (ID)	trc	Read cycle (ID)	160	-	ns	
	trdh	Read Control pulse H duration	90	-	ns	
	trdl	Read Control pulse L duration	45	-	ns	
D[17:0], D[17:10]&D[8:1], D[17:10], D[17:9]	tdst	Write data setup time	10	-	ns	For maximum CL=30pF For minimum CL=8pF
	tdht	Write data hold time	10	-	ns	
	trat	Read access time	-	40	ns	
	tratfm	Read access time	-	340	ns	
	trod	Read output disable time	20	80	ns	

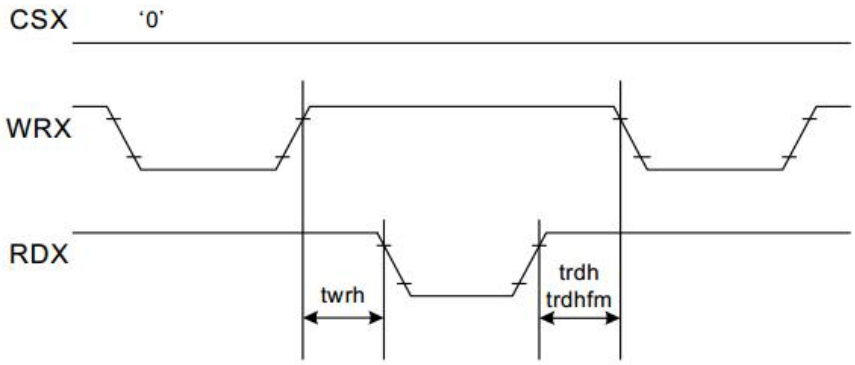
Note: Ta = -30 to 70 °C, VDDI=1.65V to 3.3V, VCI=2.5V to 3.3V, VSS=0V.

CSX timings :



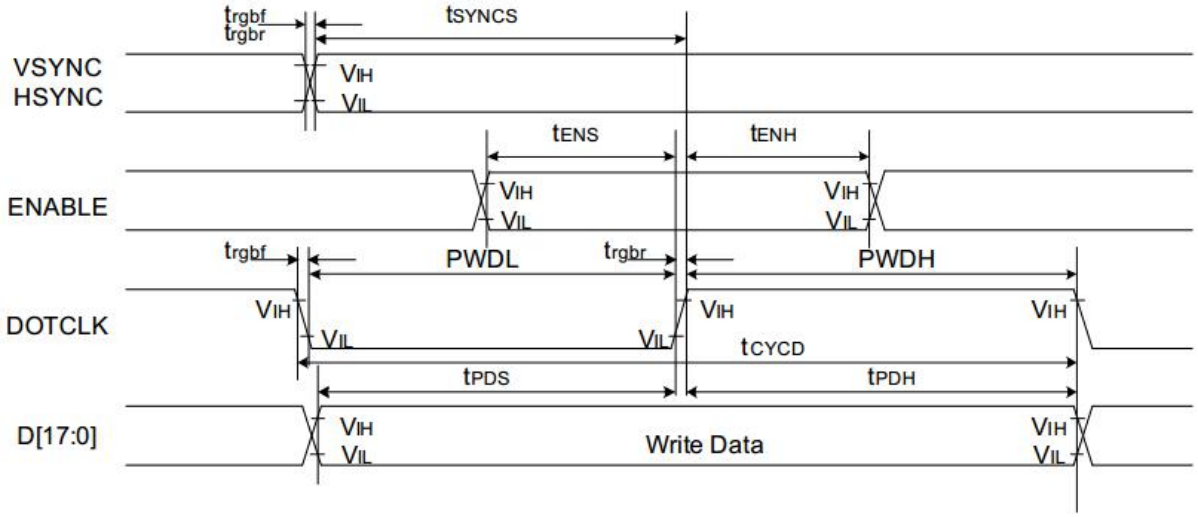
Note: Logic high and low levels are specified as 30% and 70% of VDDI for Input signals.

Write to read or read to write timings:



Note: Logic high and low levels are specified as 30% and 70% of VDDI for Input signals.

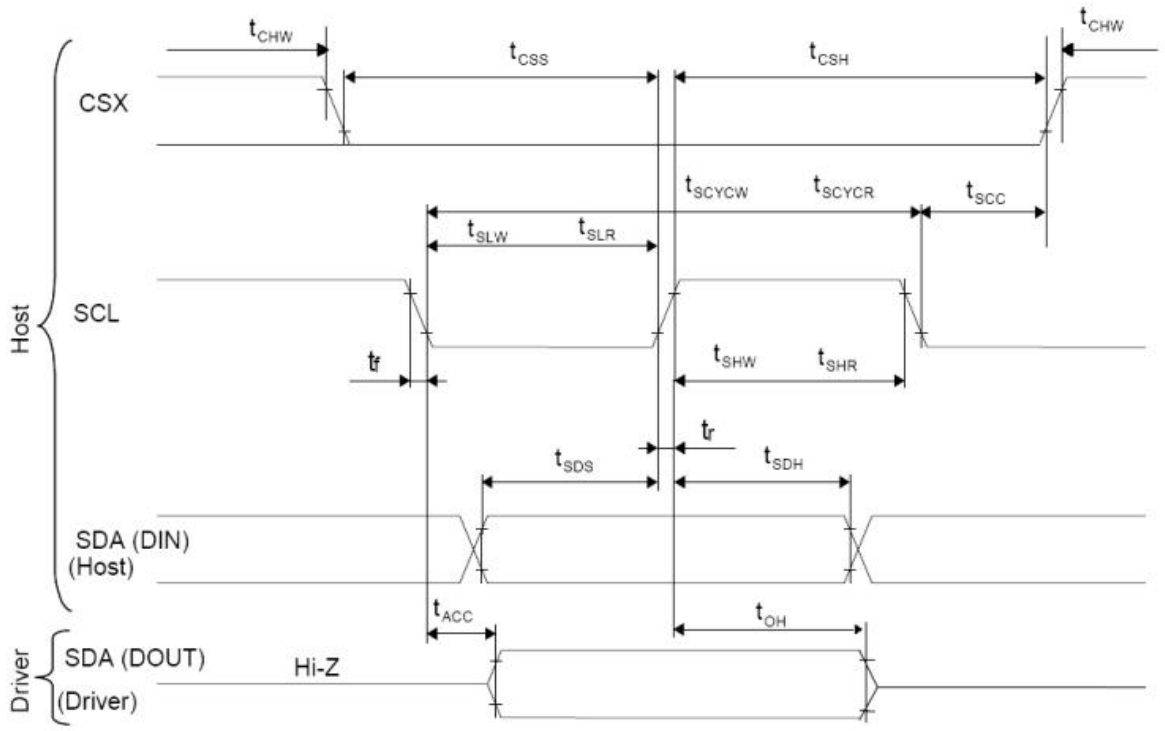
3）Parallel 18/16/6-bit RGB Interface Timing Characteristics



Signal	Symbol	Parameter	min	max	Unit	Description
VSYNC / HSYNC	t_{SYNCS}	VSYNC/HSYNC setup time	15	-	ns	18/16-bit bus RGB interface mode
	t_{SYNCH}	VSYNC/HSYNC hold time	15	-	ns	
DE	t_{ENS}	DE setup time	15	-	ns	
	t_{ENH}	DE hold time	15	-	ns	
D[17:0]	t_{POS}	Data setup time	15	-	ns	
	t_{PDH}	Data hold time	15	-	ns	
DOTCLK	PWDH	DOTCLK high-level period	15	-	ns	
	PWDL	DOTCLK low-level period	15	-	ns	
	t_{CYCD}	DOTCLK cycle time	100	-	ns	
	t_{rgbr} , t_{rgbf}	DOTCLK,HSYNC,VSYNC rise/fall time	-	15	ns	
VSYNC / HSYNC	t_{SYNCS}	VSYNC/HSYNC setup time	15	-	ns	6-bit bus RGB interface mode
	t_{SYNCH}	VSYNC/HSYNC hold time	15	-	ns	
DE	t_{ENS}	DE setup time	15	-	ns	
	t_{ENH}	DE hold time	15	-	ns	
D[17:0]	t_{POS}	Data setup time	15	-	ns	
	t_{PDH}	Data hold time	15	-	ns	
DOTCLK	PWDH	DOTCLK high-level pulse period	15	-	ns	
	PWDL	DOTCLK low-level pulse period	15	-	ns	
	t_{CYCD}	DOTCLK cycle time	50	-	ns	
	t_{rgbr} , t_{rgbf}	DOTCLK,HSYNC,VSYNC rise/fall time	-	15	ns	

Note: Ta = -30 to 70 °C, VDDI=1.65V to 3.3V, VCI=2.5V to 3.3V, AGND=VSS=0V

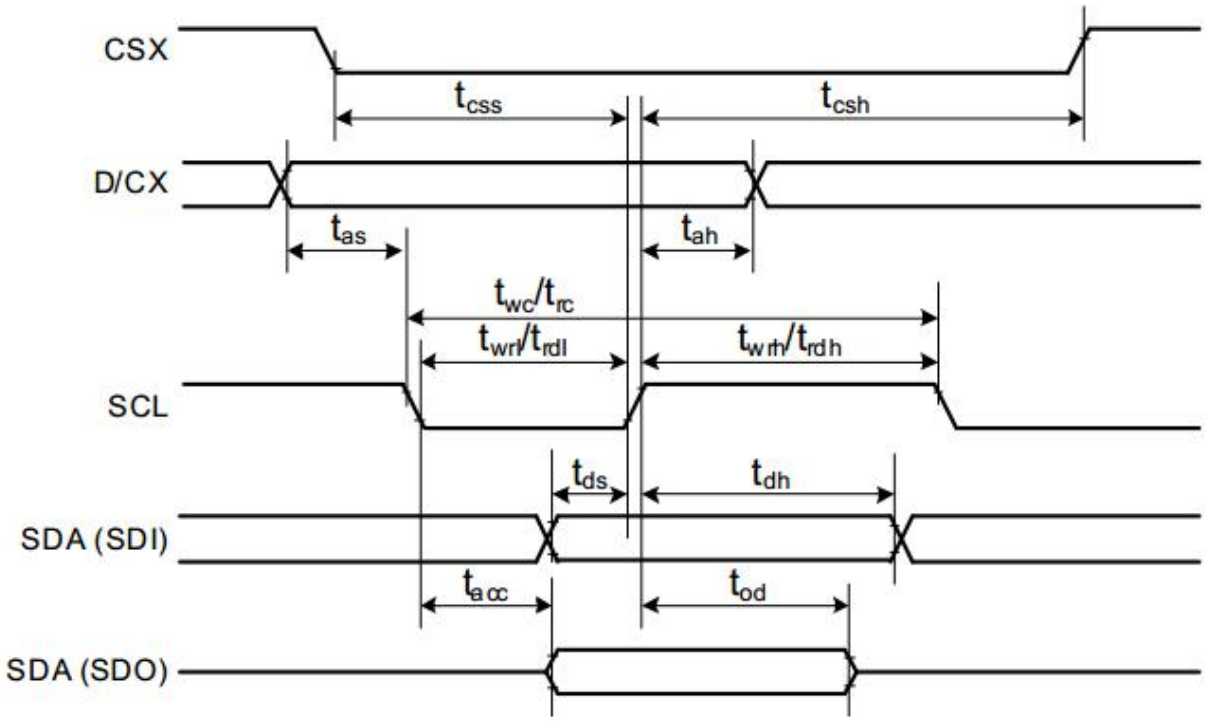
4）Display Serial Interface Timing Characteristics (3-line SPI system)



Signal	Symbol	Parameter	min	max	Unit	Description
SCL	tscycw	Serial Clock Cycle (Write)	100	-	ns	
	tshw	SCL “H” Pulse Width (Write)	40	-	ns	
	tslw	SCL “L” Pulse Width (Write)	40	-	ns	
	tscycr	Serial Clock Cycle (Read)	150	-	ns	
	tshr	SCL “H” Pulse Width (Read)	60	-	ns	
	tslr	SCL “L” Pulse Width (Read)	60	-	ns	
SDA / SDI (Input)	tsds	Data setup time (Write)	30	-	ns	
	tsdh	Data hold time (Write)	30	-	ns	
SDA / SDO (Output)	tacc	Access time (Read)	10	-	ns	
	toh	Output disable time (Read)	10	50	ns	
CSX	tscc	SCL-CSX	20	-	ns	
	tchw	CSX “H” Pulse Width	40	-	ns	
	tcss	CSX-SCL Time	60	-	ns	
	tcsh		65	-	ns	

Note: Ta = 25 °C, VDDI=1.65V to 3.3V, VCI=2.5V to 3.3V, AGND=VSS=0V

5）Display Serial Interface Timing Characteristics (4-line SPI system)



Signal	Symbol	Parameter	min	max	Unit	Description
CSX	tcss	Chip select time (Write)	40	-	ns	
	tcsh	Chip select hold time (Read)	40	-	ns	
SCL	twc	Serial clock cycle (Write)	100	-	ns	
	twrh	SCL “H” pulse width (Write)	40	-	ns	
	twrl	SCL “L” pulse width (Write)	40	-	ns	
	trc	Serial clock cycle (Read)	150	-	ns	
	trdh	SCL “H” pulse width (Read)	60	-	ns	
	trdl	SCL “L” pulse width (Read)	60	-	ns	
D/CX	tas	D/CX setup time	10	-		
	tah	D/CX hold time (Write / Read)	10	-		
SDA / SDI (Input)	tds	Data setup time (Write)	30	-	ns	
	tdh	Data hold time (Write)	30	-	ns	
SDA / SDO (Output)	tacc	Access time (Read)	10	-	ns	For maximum CL=30pF
	tod	Output disable time (Read)	10	50	ns	For minimum CL=8pF

Note: Ta = 25 °C, VDDI=1.65V to 3.3V, VCI=2.5V to 3.3V, AGND=VSS=0V

10. Quality Assurance

10.1. Purpose

This standard for Quality Assurance assures the quality of LCD module products supplied to customer.

10.2. Standard for Quality Test

10.2.1. Sampling Plan:

GB2828.1-2012

Single sampling, general inspection level II

10.2.2. Sampling Criteria:

Visual inspection: AQL 1.5%

Electrical functional: AQL 0.65%.

10.2.3. Reliability Test:

Detailed requirement refer to Reliability Test Specification.

10.3. Nonconforming Analysis & Disposition

10.3.1. Nonconforming analysis:

10.3.1.1. Customer should provide overall information of non-conforming sample for their complaints.

10.3.1.2. After receipt of detailed information from customer, the analysis of nonconforming parts usually should be finished in one week.

10.3.1.3. If cannot finish the analysis on time, customer will be notified with the progress status.

10.3.2. Disposition of nonconforming:

10.3.2.1. Non-conforming product over PPM level will be replaced.

10.3.2.2. The cause of non-conformance will be analyzed. Corrective action will be discussed and implemented.

10.4. Agreement Items

Shall negotiate with customer if the following situation occurs:

10.4.1. There is any discrepancy in standard of quality assurance.

10.4.2. Additional requirement to be added in product specification.

10.4.3. Any other special problem.

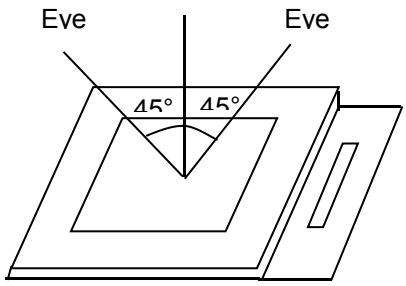
10.5. Standard of the Product Visual Inspection

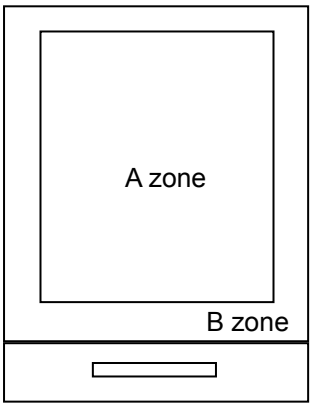
10.5.1. Appearance inspection:

10.5.1.1. The inspection must be under illumination about 1000 – 1500 lx, and the distance of view must be at 30cm ± 2cm.

10.5.1.2. The viewing angle should be 45° from the vertical line without reflection light or follows customer's viewing angle specifications.

10.5.1.3. Definition of area: A Zone: Active Area, B Zone: Viewing Area,



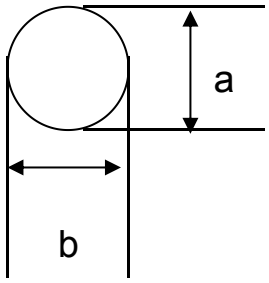


10.5.2. Basic principle:

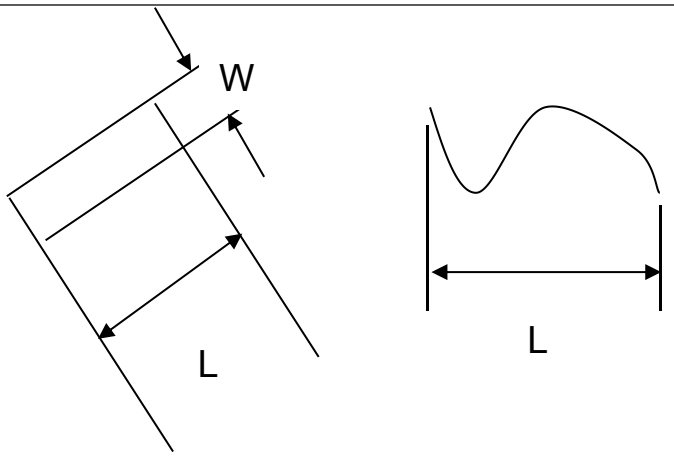
10.5.2.1. A set of sample to indicate the limit of acceptable quality level must be discussed by both us and customer when there is any dispute happened.

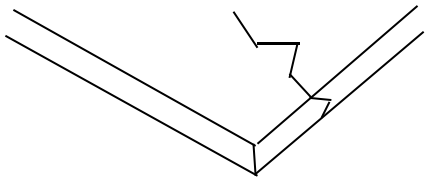
10.5.2.2. New item must be added on time when it is necessary.

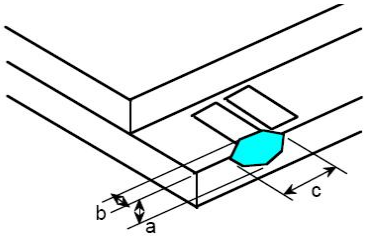
10.6. Inspection Specification

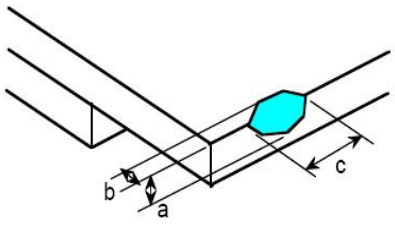
<table>
<tr><th>No.</th><th>Item</th><th>Criteria (Unit: mm)</th></tr>
<tr><td>01</td><td>Black / White spot
Foreign material
(Round type)
Pinholes
Stain
Particles inside cell.
(Minor defect)</td><td>


φ= (a + b) /2
<table>
<tr><th>Size \ Area</th><th>Acc. Qty</th></tr>
<tr><td>φ≤0.10</td><td>Ignore</td></tr>
<tr><td>0.10<φ≤0.15</td><td>2</td></tr>
<tr><td>0.15<φ≤0.25</td><td>1</td></tr>
<tr><td>0.25<φ</td><td>0</td></tr>
<tr><td>Total</td><td>2 no include φ≤ 0.10</td></tr>
</table>
Distance between 2 defects should more than 3mm apart.
</td></tr>
<tr><td>02</td><td>Electrical Defect
(Minor defect)</td><td>
<table>
<tr><td></td><td>Display Area</td><td>Total</td><td rowspan="4">Note1</td></tr>
<tr><td>Bright dot</td><td>0</td><td>0</td></tr>
<tr><td>Dark dot</td><td>N≤2</td><td>N≤2</td></tr>
<tr><td>Total dot</td><td>N≤2</td><td>N≤2</td></tr>
<tr><td>Mura</td><td colspan="2">Not visible through 5% ND filters.</td><td>Note2</td></tr>
</table>
Remark:
1. Bright dot caused by scratch and foreign object accords to item 1.
</td></tr>
</table>

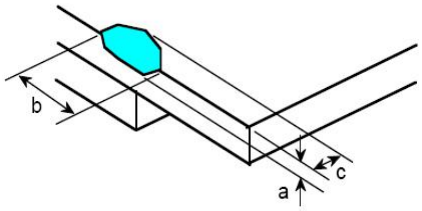
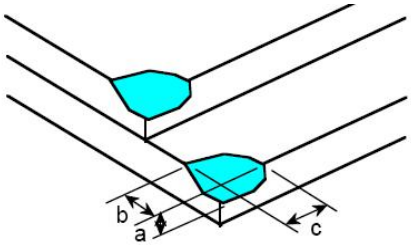
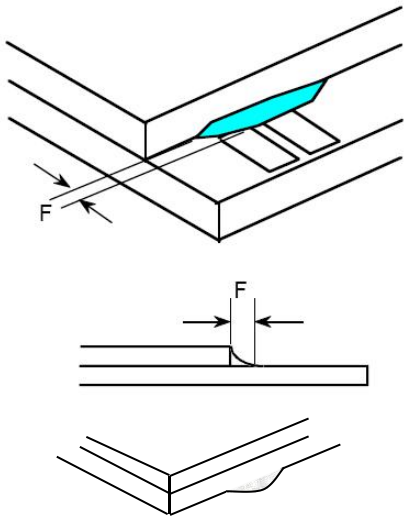
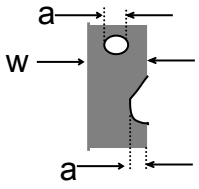
<table>
<tr>
<td>03</td>
<td>Black and White line
Scratch
Foreign material
(Line type)
(Minor defect)</td>
<td>


<table>
<tr><th>Length</th><th>Width</th><th>Acc. Qty</th></tr>
<tr><td>/</td><td>W ≦ 0.03</td><td>Ignore</td></tr>
<tr><td>L ≦ 2.5</td><td>0.03 ＜ W ≦ 0.05</td><td>3</td></tr>
<tr><td>L ≦ 2.5</td><td>0.05 ＜ W ≦ 0.10</td><td>2</td></tr>
<tr><td>/</td><td>0.1 ＜ W</td><td></td></tr>
<tr><td colspan="2">Total</td><td>3</td></tr>
</table>
Distance between 2 defects should more than 3mm apart. Scratches not viewable through the back of the display are acceptable.
</td>
</tr>
<tr>
<td>04</td>
<td>Glass Crack
(Minor defect)</td>
<td>

Crack is potential to enlarge, any type is not allowed.
</td>
</tr>
</table>

<table>
<tr>
<td>05</td>
<td>Glass Chipping Pad Area:
(Minor defect)


</td>
<td>
<table>
<tr><th>Length and Width</th><th>Acc. Qty</th></tr>
<tr><td>c > 3.0, b< 1.0</td><td>1</td></tr>
<tr><td>c< 3.0, b< 1.0</td><td>3</td></tr>
<tr><td colspan="2">a<Glass Thickness</td></tr>
</table>
</td>
</tr>
<tr>
<td>06</td>
<td>Glass Chipping Rear of Pad Area:
(Minor defect)


</td>
<td>
<table>
<tr><th>Length and Width</th><th>Acc. Qty</th></tr>
<tr><td>c > 3.0, b< 1.0</td><td>1</td></tr>
<tr><td>c< 3.0, b< 1.0</td><td>2</td></tr>
<tr><td>c< 3.0, b< 0.5</td><td>4</td></tr>
<tr><td colspan="2">a<Glass Thickness</td></tr>
</table>
</td>
</tr>
</table>

<table>
<tr>
<td>07</td>
<td>Glass Chipping Except Pad Area:
(Minor defect)
 
</td>
<td><table>
<tr><th>Length and Width</th><th>Acc. Qty</th></tr>
<tr><td>c > 3.0, b< 1.0</td><td>1</td></tr>
<tr><td>c< 3.0, b< 1.0</td><td>2</td></tr>
<tr><td>c< 3.0, b< 0.5</td><td>4</td></tr>
<tr><td colspan="2">a<Glass Thickness</td></tr>
</table></td>
</tr>
<tr>
<td>08</td>
<td>Glass Corner Chipping:
(Minor defect)
 
</td>
<td><table>
<tr><th>Length and Width</th><th>Acc. Qty</th></tr>
<tr><td>c < 3.0, b< 3.0</td><td>Ignore</td></tr>
<tr><td colspan="2">a<Glass Thickness</td></tr>
</table></td>
</tr>
<tr>
<td>09</td>
<td>Glass Burr:
(Minor defect)
 
</td>
<td><table>
<tr><th>Length</th><th>Acc. Qty</th></tr>
<tr><td>F < 1.0</td><td>Ignore</td></tr>
</table>
Glass burr don’t affect assemble and module dimension.</td>
</tr>
<tr>
<td>10</td>
<td>FPC Defect:
(Minor defect)
 
</td>
<td>10.1 Dent, pinhole width a<w/3.
(w: circuitry width.)
10.2 Open circuit is unacceptable.
10.3 No oxidation, contamination and distortion.</td>
</tr>
</table>

<table>
<tr><td>11</td><td>Bubble on Polarizer
(Minor defect)</td><td><table><tr><td>Diameter</td><td>Acc. Qty</td></tr><tr><td>φ≤0.20</td><td>Ignore</td></tr><tr><td>0.20 <φ≤0.30</td><td>4</td></tr><tr><td>0.30 <φ≤0.50</td><td>1</td></tr><tr><td>0.50 < φ</td><td>None</td></tr></table></td></tr>
<tr><td>12</td><td>Dent on Polarizer
(Minor defect)</td><td><table><tr><td>Diameter</td><td>Acc. Qty</td></tr><tr><td>φ≤0.20</td><td>Ignore</td></tr><tr><td>0.20 <φ≤0.30</td><td>4</td></tr><tr><td>0.30 <φ≤0.50</td><td>1</td></tr><tr><td>0.50 < φ</td><td>None</td></tr></table></td></tr>
<tr><td>13</td><td>Bezel</td><td>13.1 No rust, distortion on the Bezel.
13.2 No visible fingerprints, stains or other contamination.</td></tr>
<tr><td>14</td><td>Touch Panel</td><td>D: Diameter W: width L: length
14.1 Spot: D<0.25 is acceptable
0.25≤D≤0.4
2dots are acceptable and the distance between defects should more than 10 mm.
D>0.4 is unacceptable
14.2 Dent: D>0.40 is unacceptable
14.3 Scratch: W≤0.03, L≤10 is acceptable,
0.03<W≤0.10, L≤10 is acceptable
Distance between 2 defects should more than 10 mm.
W>0.10 is unacceptable.</td></tr>
<tr><td>15</td><td>PCB</td><td>15.1 No distortion or contamination on PCB terminals.
15.2 All components on PCB must same as documented on the BOM/component layout.
15.3 Follow IPC-A-600F.</td></tr>
<tr><td>16</td><td>Soldering</td><td>Follow IPC-A-610C standard</td></tr>
<tr><td>17</td><td>Electrical Defect
(Major defect)</td><td>The below defects must be rejected.
17.1 Missing vertical / horizontal segment,
17.2 Abnormal Display.
17.3 No function or no display.
17.4 Current exceeds product specifications.
17.5 LCD viewing angle defect.
17.6 No Backlight.
17.7 Dark Backlight.
17.8 Touch Panel no function.</td></tr>
</table>

Remark: LCD Panel Broken shall be rejected. Defect out of LCD viewing area is acceptable.

10.7. Classification of Defects

10.7.1. Visual defects (Except no / wrong label) are treated as minor defect and electrical defect is major.

10.7.2. Two minor defects are equal to one major in lot sampling inspection.

10.8. Identification/marking criteria

Any unit with illegible / wrong /double or no marking/ label shall be rejected.

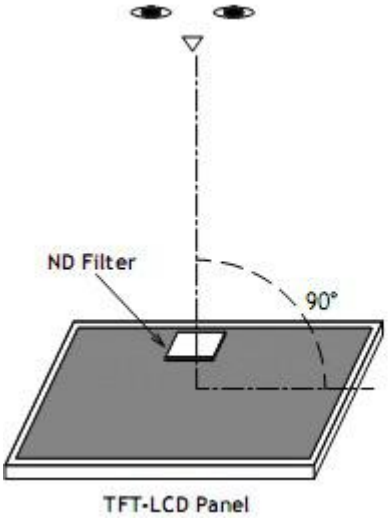
10.9. Packaging

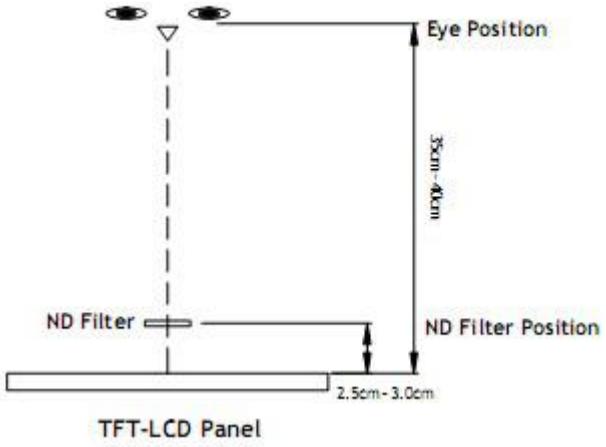
10.9.1. There should be no damage of the outside carton box, each packaging box should have one identical label.

10.9.2. Modules inside package box should have compliant mark.

10.9.3. All direct package materials shall offer ESD protection

Note1: Bright dot is defined as the defective area of the dot is larger than 50% of one sub-pixel area.





Bright dot: The bright dot size defect at black display pattern. It can be recognized by 2% transparency of filter when the distance between eyes and panel is 350mm±50mm.

Dark dot: Cyan, Magenta or Yellow dot size defect at white display pattern. It can be recognized by 5% transparency of filter when the distance between eyes and panel is 350mm±50mm.

Note2: Mura on display which appears darker / brighter against background brightness on parts of display area.

11. Reliability Specification

No	Item	Condition	Quantity	Criteria
1	High Temperature Operating	**70℃, 96Hrs**	5	GB/T2423.2 -2008
2	Low Temperature Operating	**-20℃, 96Hrs**	5	GB/T2423.1 -2008
3	High Humidity	**60℃, 90%RH, 96Hrs**	3	GB/T2423.3 -2006
4	High Temperature Storage	**80℃, 96Hrs**	3	GB/T2423.2 -2008
5	Low Temperature Storage	**-30℃, 96Hrs**	3	GB/T2423.1 -2008
6	Thermal Cycling Test	**-30℃, 30min~80℃, 30min, 10 cycles.**	3	GB/T2423.22 -2012
7	Packing vibration	Frequency range:10Hz~50Hz Acceleration of gravity:5G X, Y, Z 120 min for each direction.	2	GB/T5170.14 -2009
8	Electrical Static Discharge	Air:±2KV 150pF/330Ω 5 times Contact:±300V 150pF/330Ω 5 times	3	GB/T17626.2 -2006
9	Drop Test (Packaged)	Height:80 cm,1 corner, 3 edges, 6 surfaces.	2	GB/T2423.8 -1995

Note1. No defection cosmetic and operational function allowable.

Note2. Total current Consumption should be below double of initial value

12. Precautions and Warranty

12.1. Safety

12.1.1. The liquid crystal in the LCD is poisonous. Do not put it in your mouth. If the liquid crystal touches your skin or clothes, wash it off immediately using soap and water.

12.1.2. Since the liquid crystal cells are made of glass, do not apply strong impact on them. Handle with care.

12.2. Handling

12.2.1. Reverse and use within ratings in order to keep performance and prevent damage.

12.2.2. Do not wipe the polarizer with dry cloth, as it might cause scratch. If the surface of the LCD needs to be cleaned, wipe it swiftly with cotton or other soft cloth soaked with petroleum IPA, do not use other chemicals.

12.3. Storage

12.3.1. Do not store the LCD module beyond the specified temperature ranges.

12.3.2. Strong light exposure causes degradation of polarizer and color filter.

12.4. Metal Pin (Apply to Products with Metal Pins)

12.4.1. Pins of LCD and Backlight

12.4.1.1. Solder tip can touch and press on the tip of Pin LEAD during the soldering

12.4.1.2. Recommended Soldering Conditions

Solder Type: Sn96.3~94-Ag3.3~4.3-Cu0.4~1.1

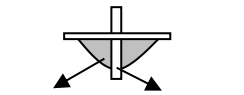
Maximum Solder Temperature: 370℃

Maximum Solder Time: 3s at the maximum temperature

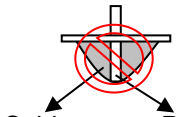
Recommended Soldering Temp: 350±20℃

Typical Soldering Time: ≤3s

12.4.1.3. Solder Wetting



Recommended



Not Recommended

12.4.2. Pins of EL

12.4.2.1. Solder tip can touch and press on the tip of EL leads during soldering.

12.4.2.2. No Solder Paste on the soldering pad on the motherboard is recommended.

12.4.2.3. Recommended Soldering Conditions

Solder type: Nippon Alimit Leadfree SR-34, size 0.5mm

Recommended Solder Temperature: 270～290℃

Typical Soldering Time: ≤2s

Minimum solder distance from EL lamp (body):2.0mm

12.4.2.4. No horizontal press on the EL leads during soldering.

12.4.2.5. 180° bend EL leads three times is not allowed.

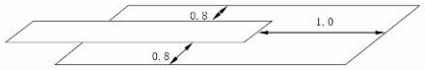
12.4.2.6. Solder Wetting

Recommended Not Recommended

12.4.2.7. The type of the solder iron:

Recommended Not Recommended

12.4.2.8. Solder Pad



12.5. Operation

12.5.1. Do not drive LCD with DC voltage

12.5.2. Response time will increase below lower temperature

12.5.3. Display may change color with different temperature

12.5.4. Mechanical disturbance during operation, such as pressing on the display area, may cause the segments to appear “fractured”.

12.5.5. Do not connect or disconnect the LCM to or from the system when power is on.

12.5.6. Never use the LCM under abnormal condition of high temperature and high humidity.

12.5.7. Module has high frequency circuits. Sufficient suppression to the electromagnetic interface shall be done by system manufacturers. Grounding and shielding methods may be important to minimize the interference.

12.5.8. Do not display the fixed pattern for long time（we suggest the time not longer than one hour） because it may develop image sticking due to the TFT structure.

12.6. Static Electricity

12.6.1. CMOS LSIs are equipped in this unit, so care must be taken to avoid the electro-static charge, by ground human body, etc.

12.6.2. The normal static prevention measures should be observed for work clothes and benches.

12.6.3. The module should be kept into anti-static bags or other containers resistant to static for storage.

12.7. Limited Warranty

12.7.1. Our warranty liability is limited to repair and/or replacement. We will not be responsible for any consequential loss.

12.7.2. If possible, we suggest customer to use up all modules in six months. If the module storage time over twelve months, we suggest that recheck it before the module be used.

12.7.3. After the product shipped, any product quality issues must be feedback within three months, otherwise, we will not be responsible for the subsequent or consequential events.

13. Packaging

TBD

14. Outline Drawing