

OLED PRODUCT SPECIFICATION

Manufactured by:



PART NUMBER:	USMP-P23201
DESCRIPTION:	1.0", 128x64, White, SEPS200A, TAB

ISSUE DATE	APPROVED BY	CHECKED BY	PREPARED BY
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REVISION RECORD

REV.	REVISION DESCRIPTION	REV. DATE	REMARK
X01	■ INITIAL RELEASE	2008. 11. 11	
X02	 Add lifetime specifications Add luminance specifications Add driver IC data Add power on/off sequence Add application circuit 	2009. 01. 07	Page 6, 8, 10, 11, 13 & 14
X03	 Add the information of module weight Add the operating conditions for different luminance Add the panel electrical specifications Modify power on/off sequence 	2009. 02. 27	Page 5, 6, 7, 8 & 13
A01	 Transfer from X version Modify definition of panel thickness Add the packing specification 	2009. 05. 05	Page 5 & 17
A02	Modify interface timing chartModify power on sequence	2010. 01. 28	Page 12 & 13

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1. SCOPE

The purpose of this specification is to define the general provisions and quality requirements that apply to the supply of display cells manufactured by RiTdisplay. This document, together with the Module Assembly Drawing, is the highest-level specification for this product. It describes the product, identifies supporting documents and contains specifications.

2. WARRANTY

RiTdisplay warrants that the products delivered pursuant to this specification (or order) will conform to the agreed specifications for twelve (12) months from the shipping date ("Warranty Period"). RiTdisplay is obligated to repair or replace the products which are found to be defective or inconsistent with the specifications during the Warranty Period without charge, on condition that the products are stored or used as the conditions specified in the specifications. Nevertheless, RiTdisplay is not obligated to repair or replace the products without charge if the defects or inconsistency are caused by the force majeure or the reckless behaviors of the customer.

After the Warranty Period, all repairs or replacements of the products are subject to charge.

3. FEATURES

- Small molecular organic light emitting diode.
- Color: White
- Panel resolution: 128*64
- Driver IC: SEPS200A
- Excellent Quick response time: 10µs
- Extremely thin thickness for best mechanism design: 1.26 mm
- High contrast: 2000:1
- Wide viewing angle: 160°
- Strong environmental resistance.
- 8-bits 6800-series parallel Interface, 8-bits 8080-series parallel Interface,
 SPI (serial Peripheral Interface), I²C Interface.
- Wide range of operating temperature : -40 to 70°C
- Anti-glare polarizer.

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4. MECHANICAL DATA

			1
NO	ITEM	SPECIFICATION	UNIT
1	Dot Matrix	128 x 64	dot
2	Dot Size	0.15 (W) x 0.15 (H)	mm ²
3	Dot Pitch	0.17 (W) x 0.17 (H)	mm ²
4	Aperture Rate	78	%
5	Active Area	21.74 (W) x 10.86 (H)	mm ²
6	Panel Size	26.4 (W) x 19.7 (H)	mm ²
7*	Panel Thickness	1.07 ± 0.1	mm
8	Module Size	26.4 (W) x 28.5 (H) x 1.26 (T)	mm ³
9	Diagonal A/A size	0.96	inch
10	Module Weight	1.29 ± 10%	gram

^{*} Panel thickness includes substrate glass, cover glass and UV glue thickness.

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5. MAXIMUM RATINGS

ITEM	MIN	MAX	UNIT	Condition	Remark
Supply Voltage (VDD)	-0.3	4.0	V	Ta = 25°C	IC maximum rating
Supply Voltage (VCC)	8	18	>	Ta = 25°C	IC maximum rating
Operating Temp.	-40	70	°C		
Storage Temp	-40	85	°C		
Humidity		85	%		
Life Time	13,000	-	Hrs	120 cd/m², 50% checkerboard	Note (1)
Life Time	16,000	-	Hrs	100 cd/m², 50% checkerboard	Note (2)
Life Time	20,000	-	Hrs	80 cd/m ² , 50% checkerboard	Note (3)

Note:

- (A) Under VCC = 12V, Ta = 25°C, 50% RH.
- (B) Life time is defined the amount of time when the luminance has decayed to less than 50% of the initial measured luminance.
- (1) Setting of 120 cd/m²:

Contrast setting: 0xae

- Frame rate : 105Hz

- Duty setting: 1/64

(2) Setting of 100 cd/m²:

Contrast setting: 0x93

- Frame rate: 105Hz

- Duty setting: 1/64

(3) Setting of 80 cd/m²:

Contrast setting: 0x74

- Frame rate: 105Hz

- Duty setting: 1/64

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6. ELECTRICAL CHARACTERISTICS

6.1 D.C ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
VDD	Logic operating voltage	-	1.6	2.8	3.6	V
vcc	OLED operating voltage	-	11.5	12	12.5	V
VIH	High level input voltage	-	0.8*VDD	ı	VDD	V
VIL	Low level input voltage	-	0	ı	0.2*VDD	>
VOH	High level output voltage	IOH = -0.1mA	0.8*VDD	ı	-	>
VOL	Low level output voltage	IOL = -0.1mA	0	ı	0.2*VDD	>
ILI	Input leakage current	VI = VSS or VDD	-1	-	1	μA
ILO	Output leakage current	VI = VSS or VDD	-1	-	1	μA

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6.2 ELECTRO-OPTICAL CHARACTERISTICS

PANEL ELECTRICAL SPECIFICATIONS

PARAMETER	MIN	TYP.	MAX	UNITS	COMMENTS
Normal mode current consumption	ı	9	11	mA	All pixels on
Standby mode current consumption	ı	1	2	mA	Standby mode 10% pixels on
Normal mode power consumption	-	108	132	mW	All pixels on
Standby mode power consumption	-	12	24	mW	Standby mode 10% pixels on
Pixel Luminance	80	100		cd/m ²	Display Average
Standby Luminance		20		cd/m ²	
CIEx (White)	0.24	0.28	0.32		CIE1931
CIEy (White)	0.28	0.32	0.36		CIE1931
Dark Room Contrast	2000:1				
Viewing Angle	160			degree	
Response Time		10		μs	

Normal mode condition:

Driving Voltage: 12V
Contrast setting: 0x93
Frame rate: 105Hz
Duty setting: 1/64
Standby mode condition:
Driving Voltage: 12V

- Contrast setting : 0x26 - Frame rate : 105Hz

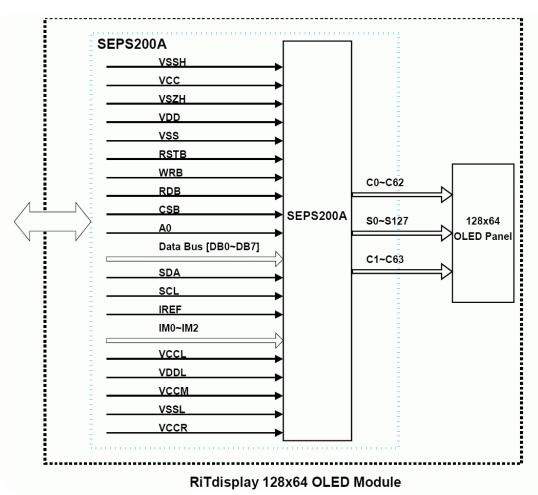
Duty setting: 1/64



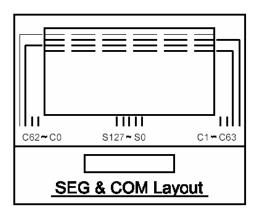


7. INTERFACE

7.1 FUNCTION BLOCK DIAGRAM



7.2 PANEL LAYOUT DIAGRAM



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7.3 PIN ASSIGNMENTS

PIN NO	PIN NAME	DESCRIPTION
1	VSSH	Ground.
2	VCC	Data driver power supply.
3	VSZH	Tie zener diode.
4	VDD	Logic power supply.
5	VSS	Ground.
6	RSTB	Reset control.
7	WRB	For an 80-series bus interface, serves as a write strobe signal, and writes data at the low level. For a 68-series bus interface, serves as a signal to select data read/ write operation. Low: write, High: read When using SPI, fix it to VDD or VSS level.
8	RDB	For an 80-series bus interface, serves as a read strobe signal, and reads data at the low level. For a 68-series bus interface, serves as an enable signal to activate data read/write operation. When using SPI, fix it to VDD or VSS level.
9	CSB	Selects the SEPS200A. Low: SEPS200A is selected and can be accessed High: SEPS200A is not selected and cannot be accessed
10	A0	Selects the data / command. Low: command High: parameter / data
11	DB0	Serves as an 8-bit bi-directional data bus.
12	DB1	8-bit bus interface: DB [7:0]
13	DB2	For a clock-synchronous serial interface, serves as the serial
14	DB3	data input pin (SDI). The input data is Latched on the rising
15	DB4	edge of the SCL signal.
16	DB5	DB[3]/R/W. DB[2]/SDO: serial data output (floating @ serial mode).
17	DB6	DB[2]/SDO: serial data output (noating @ serial mode). DB[1]/SDI: serial data input.
18	DB7	DB[0]/SCLK: serial clock.
19		-
+	SDA	l ² C serial data input.
20	SCL	l ² C serial clock input.
21	IREF	Current reference pin.
22	IM2	
23	IM1	MCU bus interface selection pin.
24	IM0	
25	VCCL	Generated power for analog circuit.
26	VDDL	Generated power for logic.
27	VCCM	Generated power for logic.
28	VSSL	Ground.
29	VCCR	Generated power for scan off.
30	VCC	Data driver power supply.
31	VSSH	Ground.

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7.4 GRAPHIC DISPLAY DATA RAM ADDRESS MAP

The GRAM is a bit mapped static RAM holding the bit pattern to be displayed. The size of the GRAM is 128 x 64 bits

GRAM structure of 200A GS Graphics RAM (128x64) 0 АХ DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 R0 000 R2 R6: 0 0 0 0 0 0 61 62 R1 000 R63 R0 63 121 122 124 120 15 0 C118 C119 C120 C122 C123 C124 C125 C126 C127 22 8 9 65 90 C121 C7 80 C119 C125 C118 C123 C126 C124 C122 C121 C120 C127 8 60 89 C7 90 65 g 2 22 5

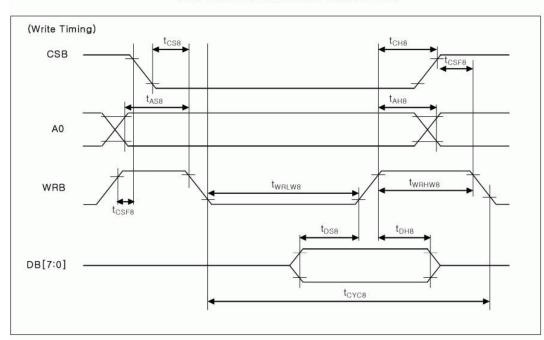




7.5 INTERFACE TIMING CHART

Write Cycle

8080-Series Parallel Interface Characteristics



8080-Series MCU Parallel Interface Timing Characteristics

ITEM	SYMBOL	CONDITION	MIN	MAX	UNIT	PORT
Chip select hold time Chip select setup time Chip select disable hold time	t _{CH8} t _{CS8} t _{CSF8}	_	5 5 20	- <u></u> 1	ns ns	CSB
Address hold time Address setup time	t _{AH8} t _{AS8}		5 25	:=:	ns ns	A0
System cycle time Write "L" pulse width Write "H" pulse width	t _{CYC8} t _{WRLW8} t _{WRHW8}	1.7	100 45 45	STI	ns ns ns	WRB
Data setup time Data hold time	t _{DS8} t _{DH8}	9.7	30 10	(71)	ns ns	DB[7:0]

(VDD = 2.8V, Ta = 25°C)

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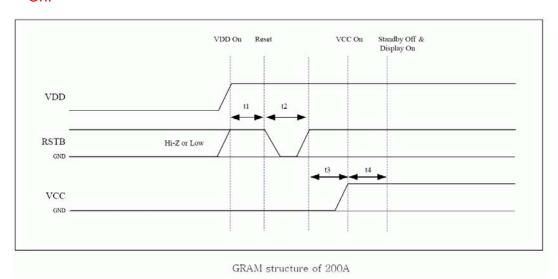


8. POWER ON / OFF SEQUENCE & APPLICATION CIRCUIT

8.1 POWER ON / OFF SEQUENCE

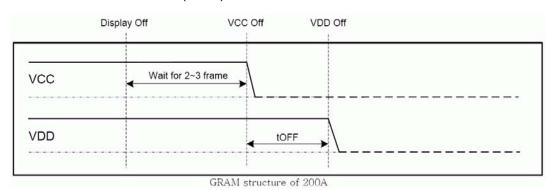
Power On sequence

- 1. VDD Power On.
- 2. After VDD becomes stable, wait for 10ms(t1), and then set RSTB pin LOW (logic low) for at least 1us (t2), and then HIGH(logic high).
- 3. After RSTB pin HIGH, wait for at least 10ms (t3). Then VCC Power on.
- After VCC Power on, wait for at least 10ms(t4). Then standby off and Display On.



Power OFF sequence

- 1. Display Off.
- 2. VCC Power Off.
- 3. Wait for at least 100ms(tOFF). Then VDD Power Off.



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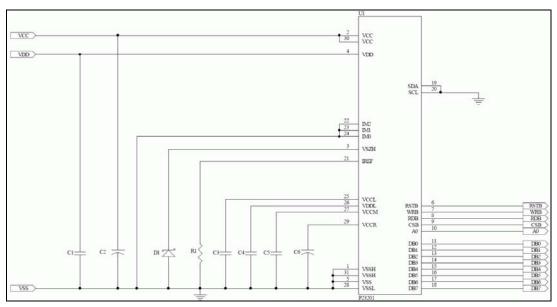
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8.2 APPLICATION CIRCUIT



Recommend components:

C1, C3, C4, C5: 1uF/16V(0603)

C2, C6: 4.7uF/25V (Tantalum type) or VISHAY (572D475X0025A2T)

R1: 68K ohm (0603) 1%

D1: UDZSTE-172.7B or PDZ2.7B (zener diode)

This circuit is for 8080 8bits interface.

8.3 COMMAND TABLE

Refer to IC Spec.: SEPS200A

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9. RELIABILITY TEST CONDITIONS

No.	Items	Specification	Quantity
1	High temp. (Non-operation)	85°C, 240hrs	5
2	High temp. (Operation)	70°C, 120hrs	5
3	Low temp. (Operation)	-40°C, 120hrs	5
4	High temp. / High humidity (Operation)	65°C, 90%RH, 120hrs	5
5	Thermal shock (Non-operation)	-40°C ~85°C (-40°C /30min; transit /3min; 85°C /30min; transit /3min) 1cycle: 66min, 100 cycles	5
6	Vibration	Frequency: 5~50HZ, 0.5G Scan rate: 1 oct/min Time: 2 hrs/axis Test axis: X, Y, Z	1 Carton
7	Drop	Height: 120cm Sequence : 1 angle \ 3 edges and 6 faces Cycles: 1	1 Carton
8	ESD (Non-operation)	Air discharge model, ±8kV, 10 times	5

Test and measurement conditions

- 1. All measurements shall not be started until the specimens attain to temperature stability.
- 2. All-pixels-on is used as operation test pattern.
- 3. The degradation of Polarizer are ignored for item 1, 4 & 5.

Evaluation criteria

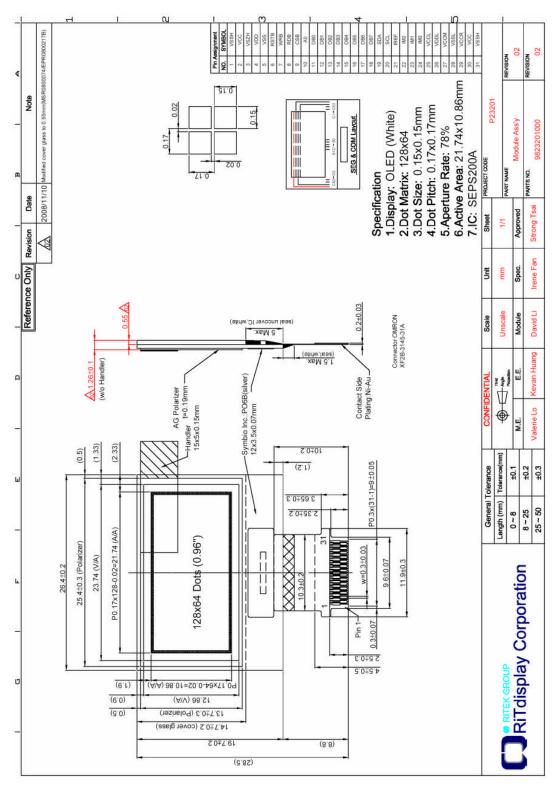
- 1. The function test is OK.
- 2. No observable defects.
- 3. Luminance: > 50% of initial value.
- 4. Current consumption: within \pm 50% of initial value.

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10. EXTERNAL DIMENSION

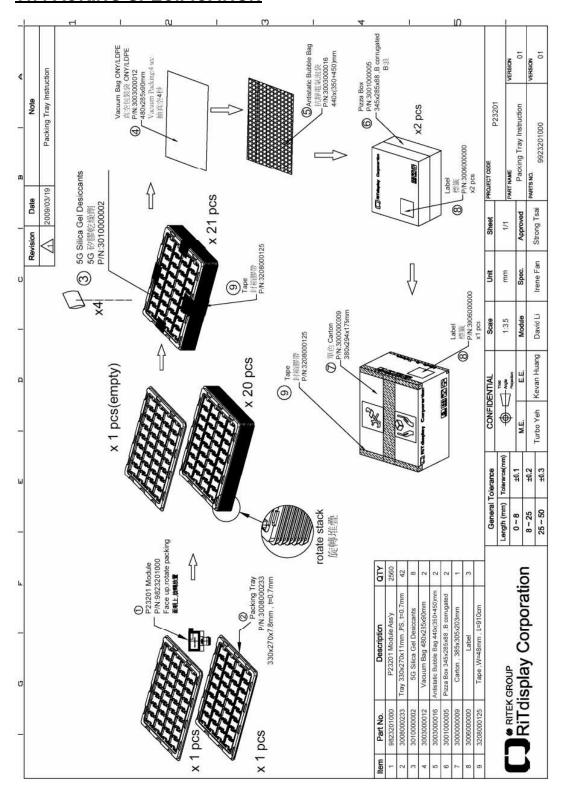


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11. PACKING SPECIFICATION



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12. APPENDIXES

APPENDIX 1: DEFINITIONS

A. DEFINITION OF CHROMATICITY COORDINATE

The chromaticity coordinate is defined as the coordinate value on the CIE 1931 color chart for R, G, B, W.

B. DEFINITION OF CONTRAST RATIO

The contrast ratio is defined as the following formula:

C. DEFINITION OF RESPONSE TIME

The definition of turn-on response time Tr is the time interval between a pixel reaching 10% of steady state luminance and 90% of steady state luminance. The definition of turn-off response time Tf is the time interval between a pixel reaching 90% of steady state luminance and 10% of steady state luminance. It is shown in Figure 2.

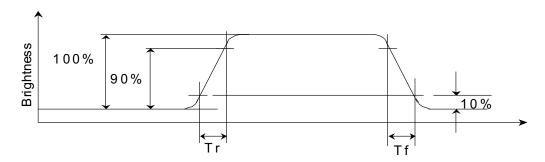


Figure 2 Response time

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D. DEFINITION OF VIEWING ANGLE

The viewing angle is defined as Figure 3. Horizontal and vertical (H & V) angles are determined for viewing directions where luminance varies by 50% of the perpendicular value.

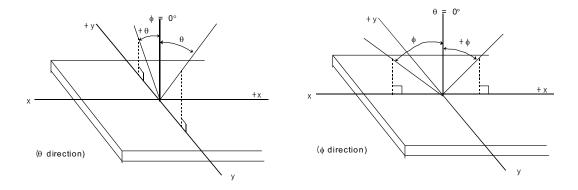


Figure 3 Viewing angle

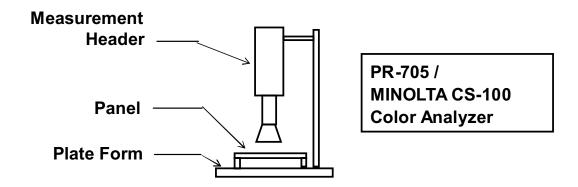




APPENDIX 2: MEASUREMENT APPARATUS

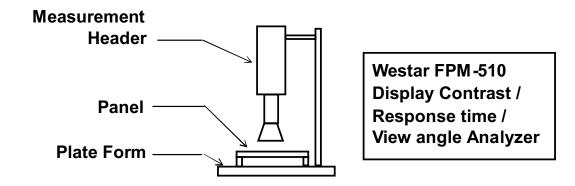
A. LUMINANCE/COLOR COORDINATE

PHOTO RESEARCH PR-705, MINOLTA CS-100



B. CONTRAST / RESPONSE TIME / VIEWING ANGLE

WESTAR CORPORATION FPM-510



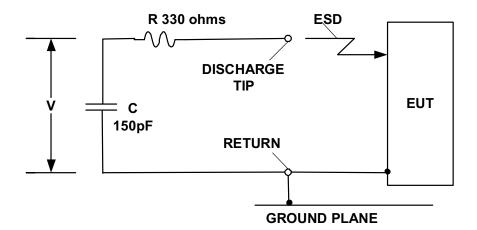
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APPENDIX 3: PRECAUTIONS

A. RESIDUE IMAGE

Because the pixels are lighted in different time, the luminance of active pixels may reduce or differ from inactive pixels. Therefore, the residue image will occur. To avoid the residue image, every pixel needs to be lighted up uniformly.

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