US Micro Products
Electronic Products for the OEM

OLED PRODUCT SPECIFICATION

Manufactured by:

RITEK GROUP
RiTdisplay Corporation

PART NUMBER:	**USMP-P21301**
DESCRIPTION:	3.2”, 256 x 64, Monochrome White, COF, SSD1322 IC

ISSUE DATE	APPROVED BY (Customer Use Only)	CHECKED BY	PREPARED BY
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REVISION RECORD

REV.	REVISION DESCRIPTION	REV. DATE	REMARK
X01	INITIAL RELEASE	2008. 04. 07	
X02	■ Add IC specifications ■ Add lifetime specifications ■ Add panel electrical specifications	2008. 06. 19	Page 4 & 6~16

CONTENTS

1. SCOPE

The purpose of this specification is to define the general provisions and quality requirements that apply to the supply of display cells manufactured by RiTdisplay. This document, together with the Module Ass'y Drawing, is the highest-level specification for this product. It describes the product, identifies supporting documents and contains specifications.

2. WARRANTY

RiTdisplay warrants that the products delivered pursuant to this specification (or order) will conform to the agreed specifications for twelve (12) months from the shipping date ("Warranty Period"). RiTdisplay is obligated to repair or replace the products which are found to be defective or inconsistent with the specifications during the Warranty Period without charge, on condition that the products are stored or used as the conditions specified in the specifications. Nevertheless, RiTdisplay is not obligated to repair or replace the products without charge if the defects or inconsistency are caused by the force majeure or the reckless behaviors of the customer.
After the Warranty Period, all repairs or replacements of the products are subject to charge.

3. FEATURES

Small molecular organic light emitting diode.

- Color : White.
- Panel matrix : 256x64.
- Driver IC : SSD1322.
- Excellent Quick response time : 10μs.
- Extremely thin thickness for best mechanism design : 2.01mm.
  High contrast : 2000:1.
- Wide viewing angle : 160°.
  8-bit 6800/8080-series parallel interface, 3/4-wire Serial Peripheral Interface.
- Wide range of operating temperature : -40 to 70 °C.
- Anti-glare polarizer.

4. MECHANICAL DATA

NO	ITEM	SPECIFICATION	UNIT
1	Dot Matrix	256 (W) x 64 (H)	dot
2	Dot Size	0.289 (W) x 0.289 (H)	mm^2
3	Dot Pitch	0.309 (W) x 0.309 (H)	mm^2
4	Aperture Rate	88	%
5	Active Area	79.084 (W) x 19.756 (H)	mm^2
6	Panel Size	87.4 (W) x 28.5 (H)	mm^2
7	Panel Thickness	2.01	mm
8	Module Size	87.4 (W) x 51.3 (H) x 2.01 (T)	mm^3
9	Diagonal A/A size	3.2	inch
10	Module Weight	TBD	gram

5. MAXIMUM RATINGS

ITEM	MIN	MAX	UNIT	Condition	Remark
Supply Voltage (V_{CI})	2.4	3.5	V	Ta = 25°C	IC maximum rating
Supply Voltage (V_{CC})	10	20	V	Ta = 25°C	IC maximum rating
Operating Temp.	-40	70	°C		
Storage Temp	-40	85	°C		
Humidity		85	%		
Life Time	13,000	-	Hrs	80 cd/m^2, 50% checkerboard	Note (1)
Life Time	16,000	-	Hrs	70 cd/m^2, 50% checkerboard	Note (2)
Life Time	19,000	-	Hrs	60 cd/m^2, 50% checkerboard	Note (3)

(A) Under VCC = 14V, Ta = 25°C, 50% RH.

(B) Life time is defined the amount of time when the luminance has decayed to less than 50% of the initial measured luminance.

(1) Setting of 80 cd/m^2 :
- Contrast setting : 0XA0
- Frame rate : 105Hz
- Duty setting : 1/64

(2) Setting of 70 cd/m^2 :
- Contrast setting : 0x78
- Frame rate : 105Hz
- Duty setting : 1/64

(3) Setting of 60 cd/m^2 :
- Contrast setting : 0x4A
- Frame rate : 105Hz
- Duty setting : 1/64

6. ELECTRICAL CHARACTERISTICS

6.1 D.C ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETERS	TEST CONDITION	MIN	TYP	MAX	UNIT
V_{CC}	Operating Voltage	-	13.5	14	14.5	V
V_{CI}	Low voltage power supply	-	2.4	2.8	3.5	V
V_{DDIO}	Power Supply for I/O pins	-	1.65	1.8	V_{CI}	V
V_{IH}	High Logic Input Level	-	0.8* V_{DDIO}	-	V_{DDIO}	V
V_{IL}	Low Logic Input Level	-	0	-	0.2* V_{DDIO}	V
V_{OH}	High Logic Output Level	I_{OUT} = 100uA	0.9* V_{DDIO}	-	V_{DDIO}	V
V_{OL}	Low Logic Output Level	I_{OUT} = 100uA	0	-	0.1* V_{DDIO}	V
I_{CC}	VCC Supply Current	VCI = 3.3V, VCC = 18V, VDDIO = 2.5V,Display ON,No panel attached, contrast = FF		TBD	TBD	mA
I_{CI}	VCI Supply Current	VCI = 3.3V, VCC = 18V, VDDIO = 2.5V, Display ON, No panel attached, contrast = FF		TBD	TBD	mA
I_{DDIO}	VDDIO Supply Current	VCI = 3.3V, VCC = 18V, VDDIO = 2.5V, Display ON, No panel attached, contrast = FF		TBD	TBD	mA
ISEG	Segment Output Current Setting V_{CC}=18V, I_{REF}=10uA	Contrast = FF	-	TBD	TBD	uA
		Contrast = 7F	-	TBD	TBD	uA
		Contrast = 3F	-	TBD	TBD	uA

Note 1: V_{CI}= 2.8 V；V_{CC}=14V；Frame rate= 105Hz；No panel attached.

Note 2: The Vcc input must keep in a stable value; ripple and noise are not allowed.

6.2 ELECTRO-OPTICAL CHARACTERISTICS

PANEL ELECTRICAL SPECIFICATIONS

PARAMETER	MIN	TYP.	MAX	UNITS	COMMENTS
Normal mode current		39	41	mA	All pixels on (1)
Standby mode current		4	6	mA	Standby mode 10% pixels on (2)
Normal mode power consumption		546	574	mW	All pixels on (1)
Standby mode power consumption		56	84	mW	Standby mode 10% pixels on (2)
Normal mode Luminance	60	70		cd/m^2	Display Average
Standby mode Luminance		30		cd/m^2	Display Average
CIEx (White)	0.24	0.28	0.32		x, y (CIE 1931)
CIEy (White)	0.28	0.32	0.36		
Dark Room Contrast	2000:1				
Viewing Angle	160			degree	
Response Time		10		μs	

(1) Normal mode condition :

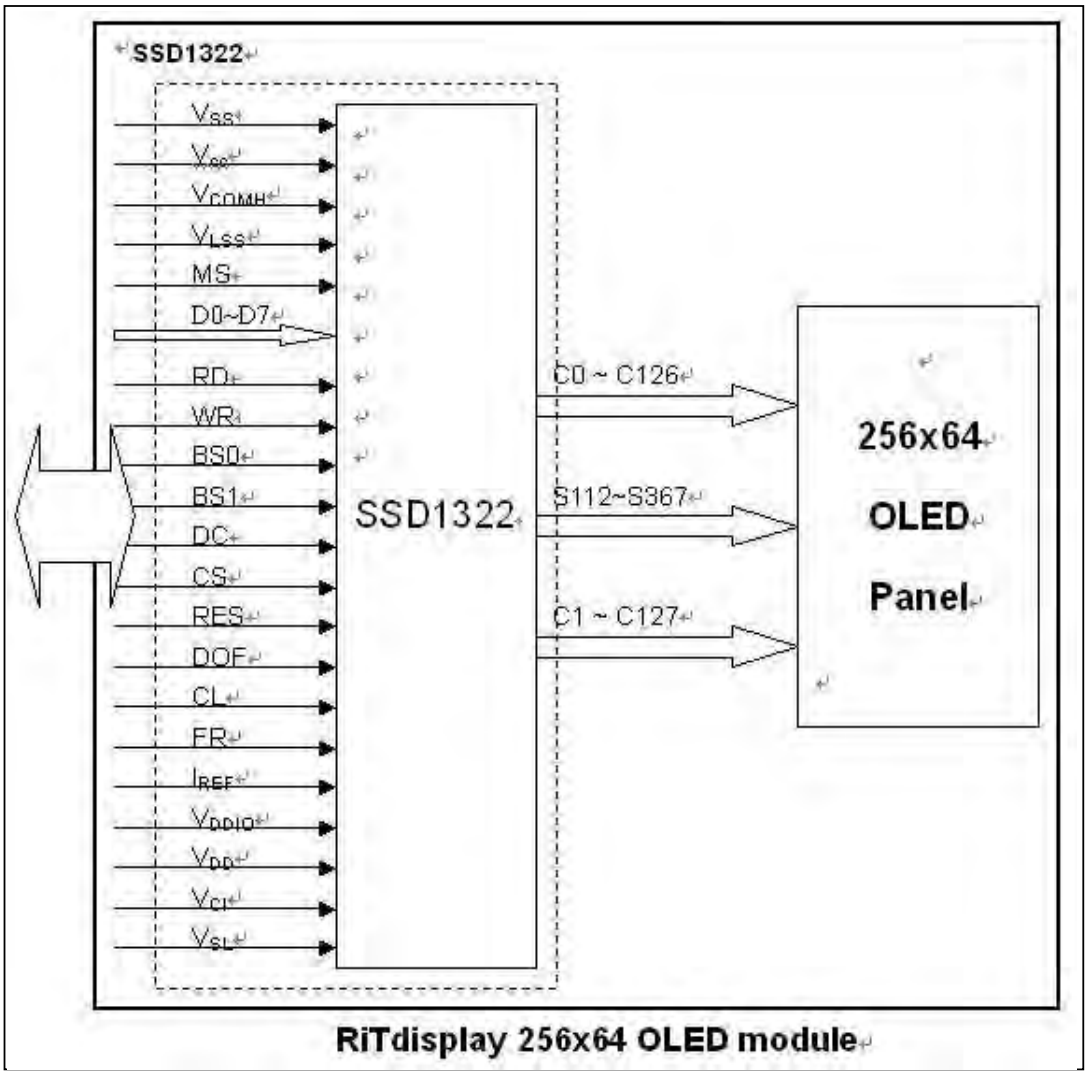
- Driving Voltage : 14V
- Contrast setting : 0x78
- Frame rate : 105Hz
- Duty setting : 1/64

(2) Standby mode condition :

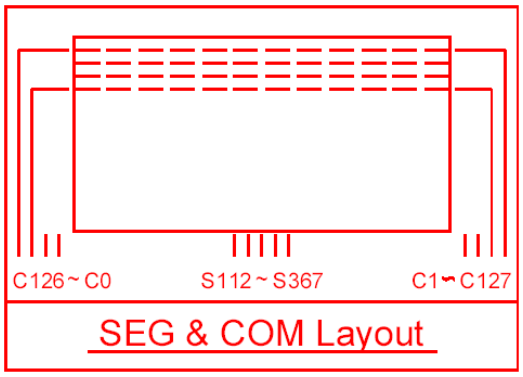
- Driving Voltage : 14V
- Contrast setting : 0x20
- Frame rate : 105Hz
- Duty setting : 1/64

7. INTERFACE

7.1 FUNCTION BLOCK DIAGRAM



7.2 PANEL LAYOUT DIAGRAM



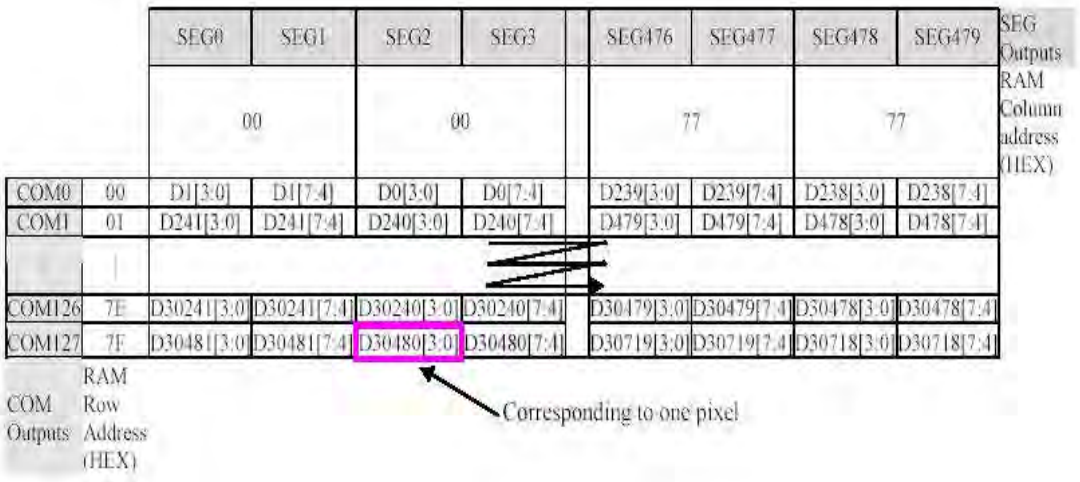
7.3 PIN ASSIGNMENTS

PIN NAME	PIN NO.	DESCRIPTION
NC	1	Not Connected.
V_{SS}	2	Ground pin.
NC	3	Not Connected.
V_{CC}	4	Power supply for panel driving voltage.
V_{COMH}	5	A capacitor should be connected between this pin and V_{SS}.
V_{LSS}	6	Analog system ground pin.
MS	7	This pin must be connected to V_{DDIO} to enable the chip.
D7	8	Bi-direction data singal.
D6	9	
D5	10	
D4	11	
D3	12	
D2	13	
D1	14	
D0	15	
RD	16	When connecting to an 8080-microprocessor, this pin receives the Read (RD#) signal. Read operation is initiated when this pin is pulled LOW and the chip is selected.
WR	17	When 8080 interface mode is selected, this pin will be the Write (WR#) input. Data write operation is initiated when this pin is pulled LOW and the chip is selected.
BS0	18	MCU bus interface selection pins.
BS1	19	
DC	20	This pin is Data/Command control pin connecting to the MCU.
CS	21	This pin is the chip select input connecting to the MCU. The chip is enabled for MCU communication only when CS# is pulled LOW.
RES	22	This pin is reset signal input. When the pin is pulled LOW, initialization of the chip is executed.
DOF	23	This pin is No Connection pins.
CL	24	External clock input pin.
FR	25	This pin is No Connection pins.
I_{REF}	26	A resistor should be connected between this pin and V_{SS}.
V_{DDIO}	27	Power supply for interface logic level. It should be matched with the MCU interface voltage level.
V_{DD}	28	Power supply pin for core logic operation. A capacitor is required to connect between this pin and V_{SS}.
V_{CI}	29	Low voltage power supply. VCI must always be equal to or higher than VDD and VDDIO.
V_{SL}	30	This is segment voltage reference pin.When external V_{SL} is used, connect with resistor and diode to ground.
V_{LSS}	31	Analog system ground pin.
NC	32	Not Connected.
V_{CC}	33	Power supply for panel driving voltage.
NC	34	Not Connected.

7.4 GRAPHIC DISPLAY DATA RAM ADDRESS MAP

The GDDRAM address map shows the GDDRAM in Gray Scale mode. Since in Gray Scale mode, there are 16 gray levels. Therefore four bits (one nibble) are allocated for each pixel.

For example D30480[3:0] corresponds to the pixel located in (COM127, SEG2). So the lower nibble and higher nibble of D0, D1, D2, …, D30717, D30718, D30719 represent the 480x128 data nibbles in the GDDRAM.



		SEG0	SEG1	SEG2	SEG3		SEG476	SEG477	SEG478	SEG479	SEG Outputs
		00		00			77		77		RAM Column address (HEX)
COM0	00	D1[3:0]	D1[7:4]	D0[3:0]	D0[7:4]		D239[3:0]	D239[7:4]	D238[3:0]	D238[7:4]	
COM1	01	D241[3:0]	D241[7:4]	D240[3:0]	D240[7:4]		D479[3:0]	D479[7:4]	D478[3:0]	D478[7:4]	
COM126	7E	D30241[3:0]	D30241[7:4]	D30240[3:0]	D30240[7:4]		D30479[3:0]	D30479[7:4]	D30478[3:0]	D30478[7:4]	
COM127	7F	D30481[3:0]	D30481[7:4]	D30480[3:0]	D30480[7:4]		D30719[3:0]	D30719[7:4]	D30718[3:0]	D30718[7:4]	
COM Outputs	RAM Row Address (HEX)										

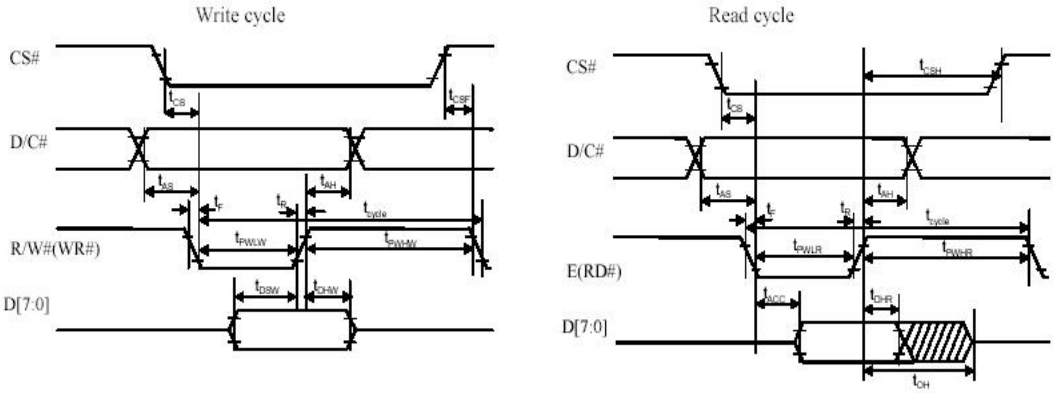
Corresponding to one pixel

7.5 INTERFACE TIMING CHART

(V_{DD} - V_{SS} = 2.4 to 2.6V, V_{DDIO}=1.6V, V_{CI} = 3.3V, T_A = 25°C)

Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time	300	-	-	ns
t_{AS}	Address Setup Time	10	-	-	ns
t_{AH}	Address Hold Time	0	-	-	ns
t_{DSW}	Write Data Setup Time	40	-	-	ns
t_{DHW}	Write Data Hold Time	7	-	-	ns
t_{DHR}	Read Data Hold Time	20	-	-	ns
t_{OH}	Output Disable Time	-	-	70	ns
t_{ACC}	Access Time	-	-	140	ns
t_{PWLR}	Read Low Time	150	-	-	ns
t_{PWLW}	Write Low Time	60	-	-	ns
t_{PWHR}	Read High Time	60	-	-	ns
t_{PWHW}	Write High Time	60	-	-	ns
t_R	Rise Time	-	-	15	ns
t_F	Fall Time	-	-	15	ns
t_{CS}	Chip select setup time	0	-	-	ns
t_{CSH}	Chip select hold time to read signal	0	-	-	ns
t_{CSF}	Chip select hold time	20	-	-	ns

8080-Series MCU Parallel Interface Timing Characteristics



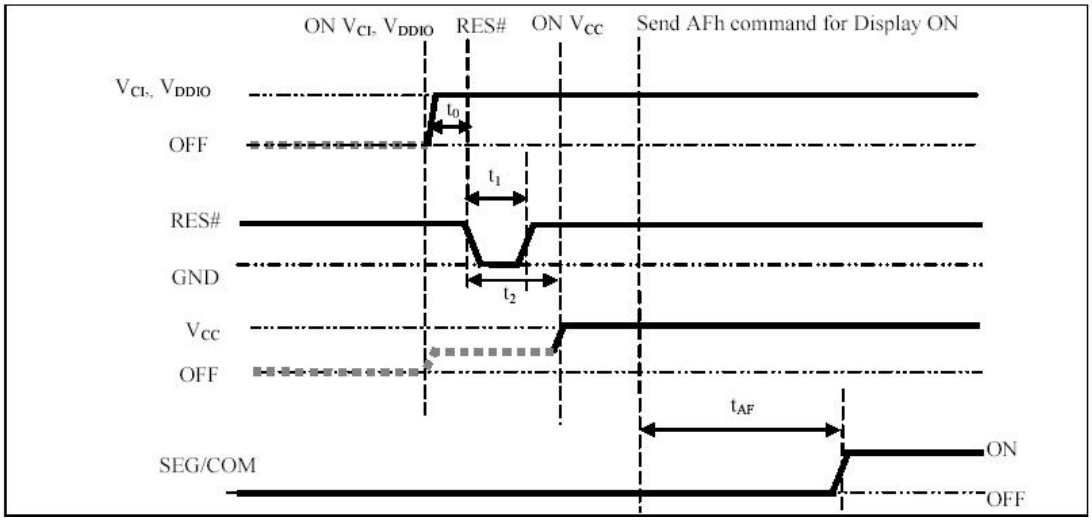
8080-series MCU parallel interface characteristics

8. POWER ON / OFF SEQUENCE & APPLICATION CIRCUIT

8.1 POWER ON / OFF SEQUENCE

***Power ON sequence*:**

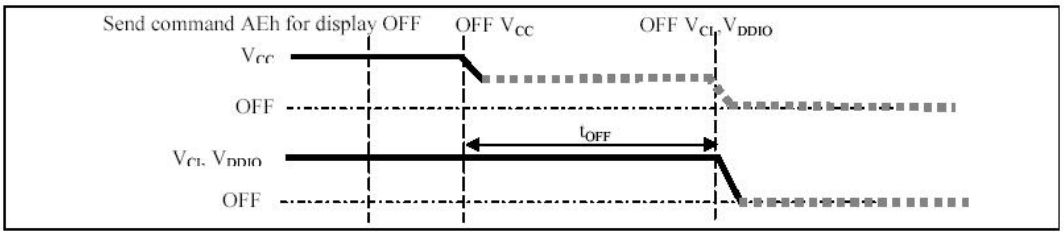
1. Power ON V_{CI}, V_{DDIO}.
2. After V_{CI}, V_{DDIO} become stable, set wait time at least 1ms (t_0) for internal V_{DD} become stable. Then set RES# pin LOW (logic low) for at least 100us (t_1) (4) and then HIGH (logic high).
3. After set RES# pin LOW (logic low), wait for at least 100us (t_2). Then Power ON V_{CC}. (1)
4. After V_{CC} become stable, send command AFh for display ON. SEG/COM will be ON after 200ms(t_{AF}).



The Power ON sequence.

***Power OFF sequence*:**

1. Send command AEh for display OFF.
2. Power OFF VCC.(1), (2)
3. Wait for t_{OFF}. Power OFF V_{CI}, V_{DDIO}.
   (where Minimum t_{OFF}=80ms (3), Typical t_{OFF}=100ms)



The Power OFF sequence

Note:

(1) Since an ESD protection circuit is connected between V_{CI}, V_{DDIO} and V_{CC}, V_{CC} becomes lower than V_{CI} whenever V_{CI},V_{DDIO} is ON and V_{CC} is OFF as shown in the dotted line of V_{CC}.

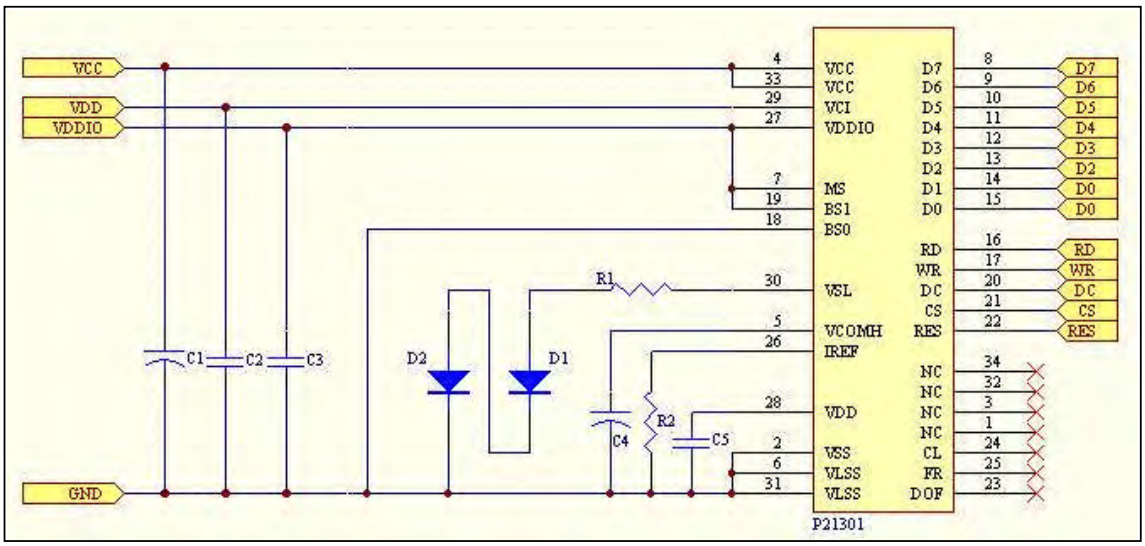
(2) V_{CC} should be kept float (disable) when it is OFF.

(3) V_{CI}, V_{DDIO} should not be Power OFF before V_{CC} Power OFF.

(4) The register values are reset after t_1.

(5) Power pins (V_{CI}, V_{CC}) can never be pulled to ground under any circumstance.

8.2 APPLICATION CIRCUIT



Recommend components:

C1&C4: 4.7uF(Tantalum Type) / 25V, or Solid Tantalum 4.7uF/ 25V/ A Case (Vishay 572D).

C2&C3&C5: 1uF(0805) / 16V.

R1 : 50 ohm 1/4W.

R2 : 430K ohm ,1%.

D1&D2 : RB480K (ROHM).

This circuit is designed for 8080 8-bits interface.

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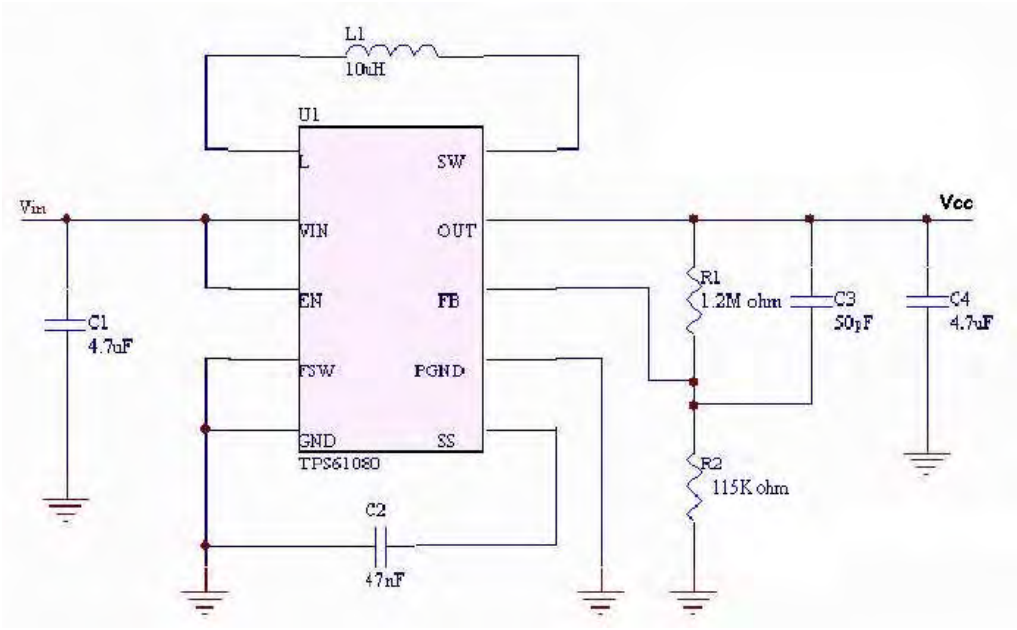
External DC-DC CIRCUIT



The R1 & R2 resistor value should be fine tune by DC-DC vendor.

8.3 COMMAND TABLE

Refer to SSD1322 IC Spec.

9. RELIABILITY TEST CONDITIONS

No.	Items	Specification	Quantity
1	High temp. (Non-operation)	85°C, 240hrs	5
2	High temp. (Operation)	70°C, 120hrs	5
3	Low temp. (Operation)	-40°C, 120hrs	5
4	High temp. / High humidity (Operation)	65°C, 90%RH, 120hrs	5
5	Thermal shock (Non-operation)	-40°C ~85°C (-40°C /30min; transit /3min; 85°C /30min; transit /3min) 1cycle: 66min, 100 cycles	5
6	Vibration	Frequency : 5~50HZ, 0.5G Scan rate : 1 oct/min Time : 2 hrs/axis Test axis : X, Y, Z	1 Carton
7	Drop	Height: 120cm Sequence : 1 angle、3 edges and 6 faces Cycles: 1	1 Carton
8	ESD (Non-operation)	Air discharge model, ±8kV, 10 times	5

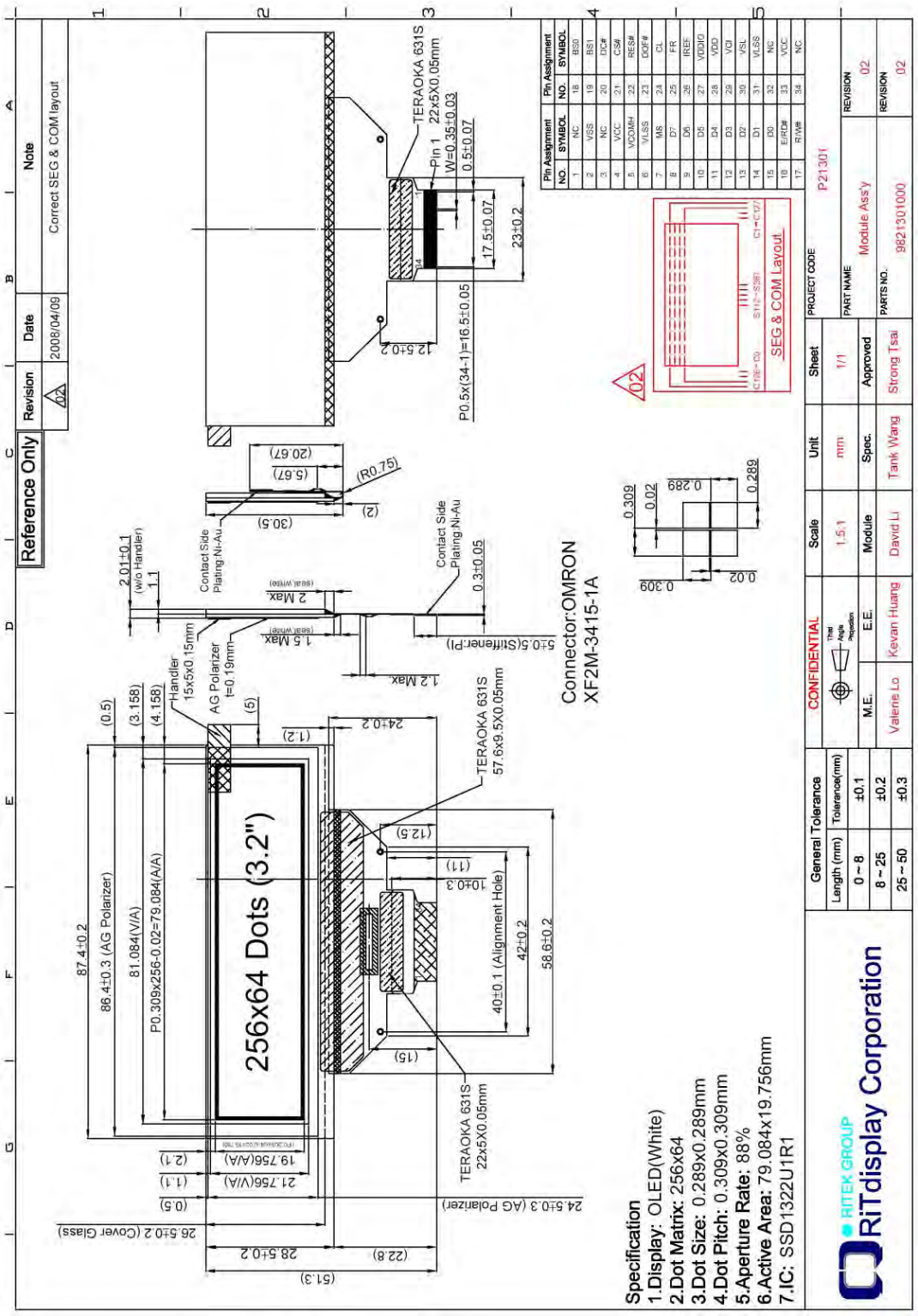
Test and measurement conditions

1. All measurements shall not be started until the specimens attain to temperature stability.
2. All-pixels-on is used as operation test pattern.
3. The degradation of Polarizer are ignored for item 1, 4 & 5.

Evaluation criteria

1. The function test is OK.
2. No observable defects.
3. Luminance: > 50% of initial value.
4. Current consumption: within ± 50% of initial value.

10. EXTERNAL DIMENSION



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11. PACKING SPECIFICATION

TBD

12. APPENDIXES

APPENDIX 1: DEFINITIONS

A. DEFINITION OF CHROMATICITY COORDINATE

The chromaticity coordinate is defined as the coordinate value on the CIE 1931 color chart for R, G, B, W.

B. DEFINITION OF CONTRAST RATIO

The contrast ratio is defined as the following formula:

$$\text{Contrast Ratio} = \frac{\text{Luminance of all pixels on measurement}}{\text{Luminance of all pixels off measurement}}$$

C. DEFINITION OF RESPONSE TIME

The definition of turn-on response time Tr is the time interval between a pixel reaching 10% of steady state luminance and 90% of steady state luminance. The definition of turn-off response time Tf is the time interval between a pixel reaching 90% of steady state luminance and 10% of steady state luminance. It is shown in Figure 2.

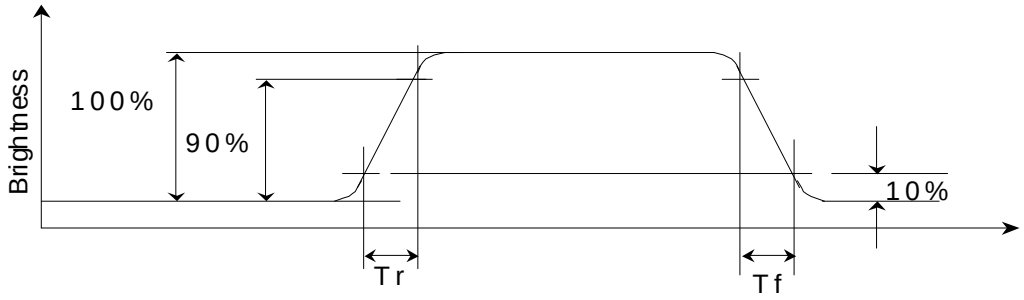


Figure 2 Response time

D. DEFINITION OF VIEWING ANGLE

The viewing angle is defined as Figure 3. Horizontal and vertical (H & V) angles are determined for viewing directions where luminance varies by 50% of the perpendicular value.

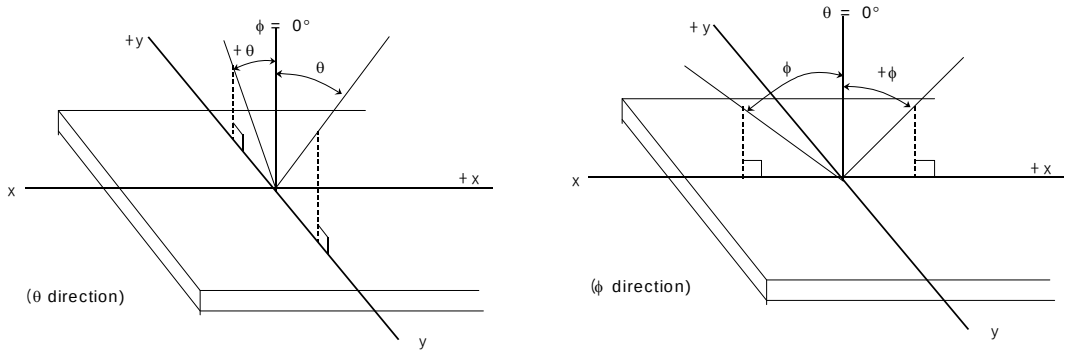
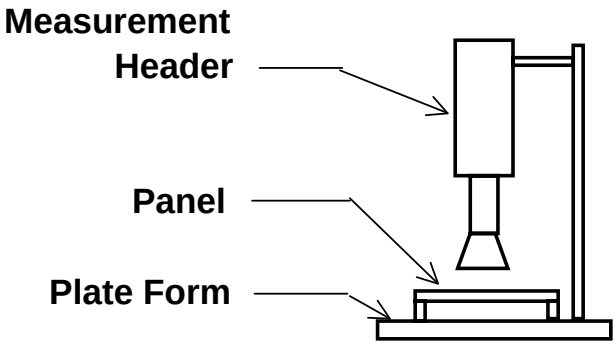


Figure 3 Viewing angle

APPENDIX 2: MEASUREMENT APPARATUS

A. LUMINANCE/COLOR COORDINATE

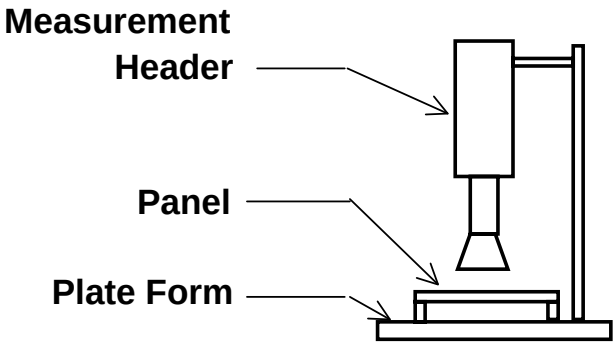
PHOTO RESEARCH PR-705, MINOLTA CS-100



**PR-705 /
MINOLTA CS-100
Color Analyzer**

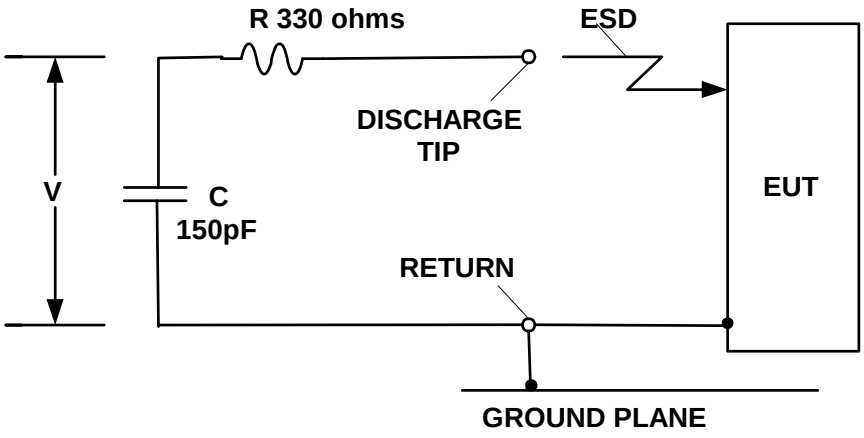
B. CONTRAST / RESPONSE TIME / VIEW ANGLE

WESTAR CORPORATION FPM-510



**Westar FPM-510
Display Contrast /
Response time /
View angle Analyzer**

C. ESD ON AIR DISCHARGE MODE



APPENDIX 3: PRECAUTIONS

A. RESIDUE IMAGE

Because the pixels are lighted in different time, the luminance of active pixels may reduce or differ from inactive pixels. Therefore, the residue image will occur. To avoid the residue image, every pixel needs to be lighted up uniformly.

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