

OLED PRODUCT SPECIFICATION

Manufactured by:



PART NUMBER:	USMP-P19801 V01
DESCRIPTION:	.95" OLED, 65K Full Color, 68/80series MPU 8-bit, SPI 4-wire interface, SEPS114A Driver IC

ISSUE DATE	APPROVED BY	CHECKED BY	PREPARED BY
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REVISION RECORD

REV.	REVISION DESCRIPTION	REV. DATE	REMARK
X01	INITIAL RELEASE	2009. 09. 30	
X02	 Add lifetime specifications Add panel electrical specifications Modify power on/off sequence Add application circuit 	2009. 11. 20	Page 6, 7, 8, 15 & 17
A01	 ■ Transfer from X version ■ Add the information of module weight ■ Modify seal color (white→black) ■ Add the packing specification 	2009. 12. 10	Page 5, 19 & 20

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1. SCOPE

The purpose of this specification is to define the general provisions and quality requirements that apply to the supply of display cells manufactured by RiTdisplay. This document, together with the Module Assembly Drawing, is the highest-level specification for this product. It describes the product, identifies supporting documents and contains specifications, which are either not addressed, or are exceptions to the supporting documents.

2. WARRANTY

RiTdisplay warrants that the products delivered pursuant to this specification (or order) will conform to the agreed specifications for twelve (12) months from the shipping date ("Warranty Period"). RiTdisplay is obligated to repair or replace the products which are found to be defective or inconsistent with the specifications during the Warranty Period without charge, on condition that the products are stored or used as the conditions specified in the specifications. Nevertheless, RiTdisplay is not obligated to repair or replace the products without charge if the defects or inconsistency are caused by the force majeure or the reckless behaviors of the customer.

After the Warranty Period, all repairs or replacements of the products are subject to charge.

3. FEATURES

Small molecular organic light emitting diode.

Color :65K colors
Panel matrix : 96*3*64
Driver IC : SEPS114A

Excellent Quick response time: 10 µs

Extremely thin thickness for best mechanism design: 1.41 mm

High contrast : 2000:1 Wide viewing angle : 160°

Strong environmental resistance.

68/80series MPU 8 bit, SPI 4 wire interface.

Wide range of operating temperature: -40 to 70°C

Anti-glare polarizer.

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4. MECHANICAL DATA

NO	ITEM	SPECIFICATION	UNIT
1	Dot Matrix	96 (W) x (RxGxB) x 64 (H)	dot
2	Dot Size	0.045 (W) x 0.19 (H)	mm ²
3	Dot Pitch	0.07 (W) x 0.21 (H)	mm ²
4	Aperture Rate	58	%
5	Active Area	20.135 (W) x 13.42 (H)	mm ²
6	Panel Size	24.2 (W) x 20.9 (H)	mm ²
7*	Panel Thickness	1.22 ± 0.1	Mm
8	Module Size	24.2 (W) x 30.9 (H) x 1.41 (D)	mm ³
9	Diagonal A/A size	0.95	inch
10	Module Weight	1.44 ± 10%	gram

^{*} Panel thickness includes substrate glass, cover glass and UV glue thickness.

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5. MAXIMUM RATING

ITEM	MIN	MAX	UNIT	Condition	Remark
Supply Voltage (V _{DD})	-0.3	4	٧	Ta = 25°C	IC maximum rating
Supply Voltage (Vcc)	8	18	V	Ta = 25°C	IC maximum rating
Operating Temp.	-40	70	°C		_
Storage Temp	-40	85	°C		
Humidity		85	%		
Life Time	10,000	-	Hrs	120 cd/m ² , 50% checkerboard	Note (1)
Life Time	12,000	-	Hrs	100 cd/m ² , 50% checkerboard	Note (2)
Life Time	15,000	-	Hrs	80 cd/m ² , 50% checkerboard	Note (3)

Note:

- (A) Under Vcc =13V, Ta = 25°C, 50% RH.
- (B) Life time is defined the amount of time when the luminance has decayed to less than 50% of the initial measured luminance.
- (1) Setting of 120 cd/m²:

Blue contrast setting: 0x52Green contrast setting: 0x39Red contrast setting: 0x39

Frame rate: 105Hz
Duty setting: 1/64
(2) Setting of 100 cd/m²:

Blue contrast setting : 0x46Green contrast setting : 0x30Red contrast setting : 0x30

Frame rate: 105Hz
Duty setting: 1/64
(3) Setting of 80 cd/m²:

Blue contrast setting: 0x38Green contrast setting: 0x26Red contrast setting: 0x26

Frame rate : 105HzDuty setting : 1/64

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6. ELECTRICAL CHARACTERISTICS

6.1 D.C ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETERS	CONDITIONS	MIN	TYP	MAX	UNIT
VCC	Driver Power Supply (For OLED Panel)	-	12.5	13	13.5	V
VDD	Logic Power Supply	-	2.4	-	3.3	V
VDDIO	Logic I/O Operating Voltage	-	1.65	-	3.3	V
VIH	High logic input voltage	-	0.8*VDDIO	-	VDDIO	V
VIL	Low logic input voltage	1	0	-	0.4	V
VOH	High logic output voltage	IOH = 0.1mA	VDDIO-0.4	-	-	V
VOL	Low logic output voltage	IOL = 0.1mA	1	ı	0.4	V
ILI	Input leakage current	VI = VSS or VDDIO	-1	-	1	uA
ILO	Output leakage current	VI = VSS or VDDIO	-1	-	1	uA
FOSCE	Oscillator frequency By external resistor	$RF = 27K\Omega$	-	-	3	MHz

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6.2 ELECTRO-OPTICAL CHARACTERISTICS

PANEL ELECTRICAL SPECIFICATIONS

PARAMETER	MIN	TYP.	MAX	UNITS	COMMENTS
Normal mode current		11	13	mA	All pixels on (1)
Standby mode current		1	2	mA	Standby mode 10% pixels on (2)
Normal mode power consumption		143	169	mW	All pixels on (1)
Standby mode power consumption		13	26	mW	Standby mode 10% pixels on (2)
Normal mode Luminance	80	100		cd/m ²	Display Average
Standby mode Luminance		20		cd/m ²	
CIEx (White)	0.24	0.28	0.32		
CIEy (White)	0.28	0.32	0.36		
CIEx (Red)	0.62	0.66	0.70		
CIEy (Red)	0.29	0.33	0.37		x, y (CIE 1931)
CIEx (Green)	0.26	0.30	0.34		x, y (CIL 1931)
CIEy (Green)	0.59	0.63	0.67		
CIEx (Blue)	0.10	0.14	0.18		
CIEy (Blue)	0.14	0.18	0.22		
Dark Room Contrast	2000:1				
Viewing Angle	160			degree	
Response Time		10		μs	

(1) Normal mode condition:

Driving Voltage: 13V

Blue contrast setting: 0x46Green contrast setting: 0x30Red contrast setting: 0x30

Frame rate : 105HzDuty setting : 1/64

(2) Standby mode condition:

Driving Voltage: 13V

Blue contrast setting: 0x16
Green contrast setting: 0x10
Red contrast setting: 0x10

Frame rate : 105HzDuty setting : 1/64

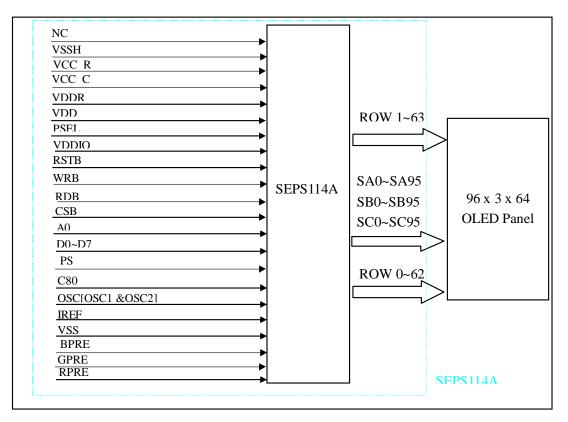
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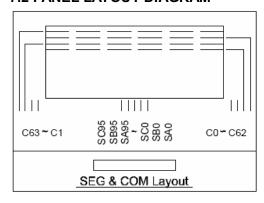
7. INTERFACE

7.1 FUNCTION BLOCK DIAGRAM



RiT display 96x3x64 OLED Module

7.2 PANEL LAYOUT DIAGRAM



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7.3 PIN ASSIGNMENTS

PIN NO	PIN NAME	DESCRIPTION
1	NC	No connection.
2	VSSH	Ground for VCC_C/VCC_R
3	VCC_R	Power Supply for Scan Driver
4	VCC_C	Data Driver Power Supply
5	VDDR	Logic Power Supply2
6	VDD	Logic Power Supply
7	PSEL	Regulator Enable/Disable for Logic Power Supply2
8	VDDIO	MPU I/F PAD Power Supply VDDIO should be lower than VDD or the same as VDD.
9	RSTB	Reset Signal Input (active low)
10	WRB	For an 80 serise bus interface, write strobe signal (active low) For an 68 serise bus interface, read/write select Low: Write, High: Read When using SPI, fix it to VDDIO or VSS level
11	RDB	For an 80-serise bus interface, read strobe signal (active low) For an 68-serise bus interface, bus enable strobe (active high) When using SPI, fix it to VDDIO or VSS level
12	CSB	Selects the chip Low: chip is selected and can be accessed High: chip is not selected and cannot be accessed
13	A0	Selects the data / command Low: command, High: parameter / data
14	D0	bi directional data bus
15	D1	bi directional data bus
16	D2	bi directional data bus
17	D3	bi directional data bus
18	D4	bi directional data bus
19	D5	bi directional data bus
20	D6	bi directional data bus
21	D7	bi directional data bus
22	PS	Selects parallel/Serial interface type Low: serial, High: parallel
23	C80	Selects the MPU type Low: 80 Series Interface, High: 68 Series Interface
24	OSC1	Please connect external resister between OSC1 and OSC2.
25	OSC2	
26	IREF	Tie resister to VSS
27	VSS	Ground for VDD/VDDR
28	BPRE	Pre Charge Voltage for Blue

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29	GPRE	Pre Charge Voltage for Green
30	RPRE	Pre Charge Voltage for Red
31	VCC C	Data Driver Power Supply
32	VCC_R	Power Supply for Scan Driver
33	VSSH	Ground for VCC_C/VCC_R
34	NC	No connection.

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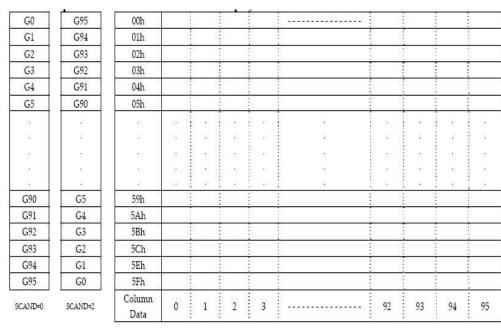




7.4 GRAPHIC DISPLAY DATA RAM ADDRESS MAP

The DDRAM stores pixel data for the display. It is composed of 96 row by 96 column x 16 bit addressable array. Address counter provides row and column address to DDRAM for access display pixel data from MPU.

Relationship between DDRAM Address and Display Position



D0	D1	D2	D3	 D92	D93	D94	D95
		_	8	 740			
S0	S1	52	8		S285	S286	S287

SCAND[1:0]: Row scan direction register(09h).

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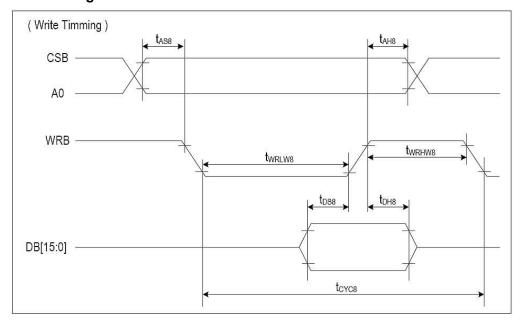
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7.5 INTERFACE TIMING CHART

System BUS Read/Write Timing (80 series CPU interface)

Write Timing



(VDD = 2.8V, Ta = 25°c)

ITEM	SYMBOL	CONDITION	MIN	MAX	UNIT	PORT
Address hold timing	tahs		5		ns	CSB
Address setup timing	t _{AS8}	*	5		ns	A0
System cycle timing	tcycs		100		ns	
Write "L" pulse width	twrlws	2	45	<u>8</u>	ns	WRB
Write "H" pulse width	twr.hws		45		ns	
Data setup timing	toss		30		ns	DDG E O
Data hold timing	tons	8	10	7	ns	DB[15:0]

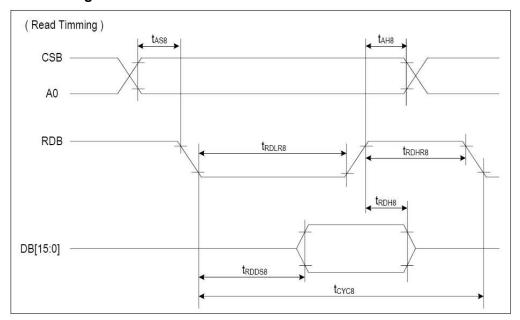
notice) All the timing reference is 10% and 90% of VDDIO.

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Read Timing



(VDD = 2.8V, Ta = 25℃)

	25 OF			(1DD 2.01, 1a 200)		
ITEM	SYMBOL	CONDITION	MIN	MAX	UNIT	PORT
Address hold timing	tans		5		ns	CSB
Address setup timing	t _{AS8}		5	152	ns	A0
System cycle timing	tcycs		200		ns	
Read "L" pulse width	trdlr8	(-)	90		ns	RDB
Read "H" pulse width	trohrs		90		ns	
Read data output delay time	trops	CI 15 F	2	(0)	ns	DRI1E OI
Data hold timing	trdH8	CL = 15 pF	0	60	ns	DB[15:0]

Notice) All the timing reference is 10% and 90% of VDDIO.

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8. POWER ON / OFF SEQUENCE & APPLICATION CIRCUIT

8.1 POWER ON / OFF SEQUENCE

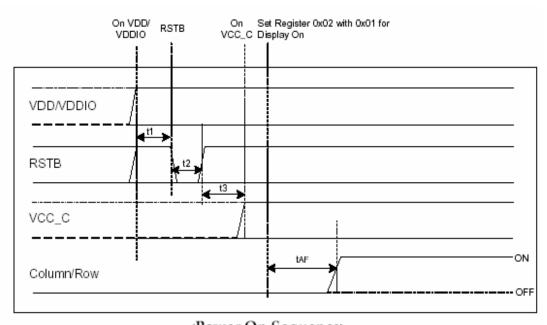
The following figures illustrate the recommended power ON and OFF sequence of SEPS114A.

Power ON sequence

- (1) Power On VDD, VDDIO.
- (2) After VDD, VDDIO become stable and wait for 100ms(t1), set RSTB pin LOW (logic low) for at least 1ms (t2) and then HIGH(logic high).
- (3) After set RSTB pin HIGH (logic high), wait for at least 50ms (t3). Then Power On VCC C
- (4) After VCC_C become stable, set register 0x02 with value 0x01 for display On.Data/Scan will be On after 200ms (tAF).

Power OFF sequence

- (1) Set register 0x02 with value 0x00 for display OFF.
- (2) Power OFF VCC_C.
- (3) Wait for tOFF. Power OFF VDD, VDDIO (where Minimum tOFF=80ms, Typical tOFF=100ms)

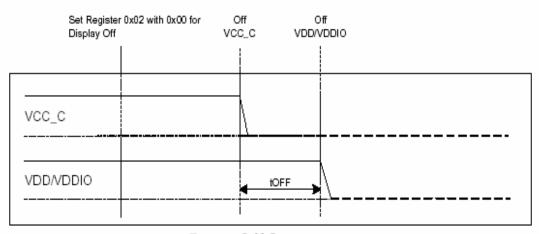


<Power On Sequence>

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<Power Off Sequence>

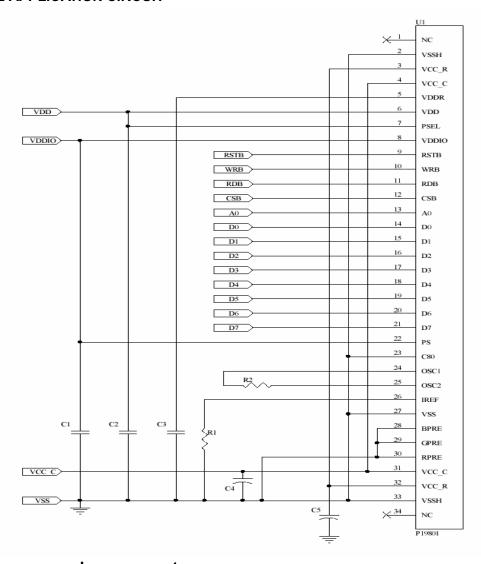
Note:

Since ESD protection circuit is connected between VDD, VDDIO and VCC_C, VCC_C becomes lower than VDD whenever VDD, VDDIO is On and VCC_C is Off. VCC_C should be kept disable when it is Off.





8.2 APPLICATION CIRCUIT



Recommend components:

C1, C2, C3: 1uF/16V(0603)

C4, C5: 2.2uF/25V(Tantalum type) or VISHAY (572D475X0025A2T)

R1: 39k ohm(0603) R2: 27k ohm(0603)

This circuit is for 8080 8bits interface.

8.3 COMMAND TABLE

Refer to IC Spec.: SEPS114A

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9. RELIABILITY TEST CONDITIONS

No.	Items	Specification	Quantity
1	High temp. (Non-operation)	85°C, 240hrs	5
2	High temp. (Operation)	70°C, 120hrs	5
3	Low temp. (Operation)	-40°C, 120hrs	5
4	High temp. / High humidity (Operation)	65°C, 90%RH, 96hrs	5
5	Thermal shock (Non-operation)	-40°C ~85°C (-40°C /30min; transit /3min; 85°C /30min; transit /3min) 1cycle: 66min, 20 cycles	5
6	Vibration	Frequency: 5~50HZ, 0.5G Scan rate: 1 oct/min Time: 2 hrs/axis Test axis: X, Y, Z	1 Carton
7	Drop	Height: 120cm Sequence : 1 angle \ 3 edges and 6 faces Cycles: 1	1 Carton
8	ESD (Non-operation)	Air discharge model, ±8kV, 10 times	5

Test and measurement conditions

- 1. All measurements shall not be started until the specimens attain to temperature stability.
- 2. All-pixels-on is used as operation test pattern.
- 3. The degradation of Polarizer are ignored for item 1, 4 & 5.

Evaluation criteria

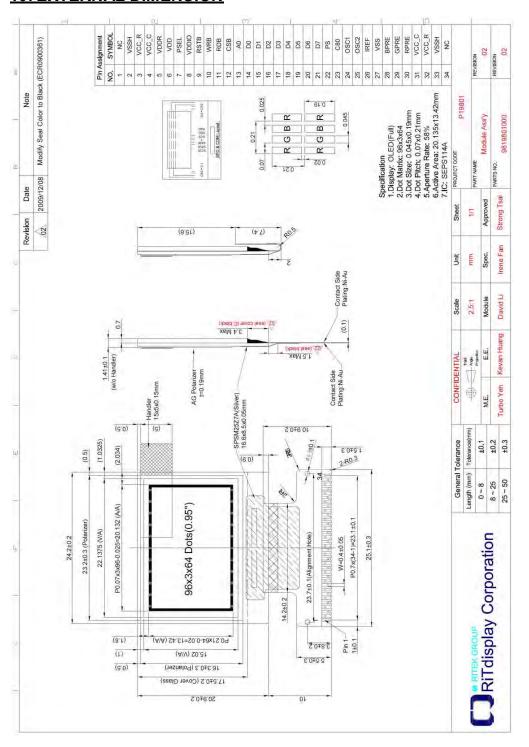
- 1. The function test is OK.
- 2. No observable defects.
- 3. Luminance: > 50% of initial value.
- 4. Current consumption: within \pm 50% of initial value.

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10. EXTERNAL DIMENSION

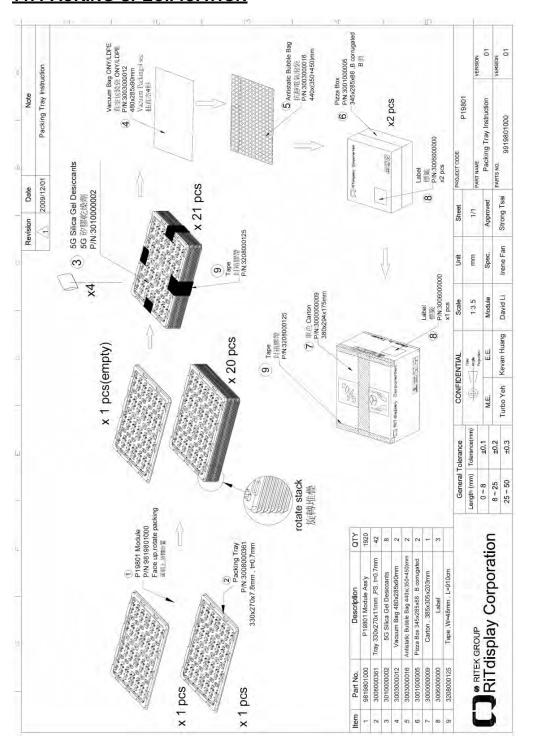


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11. PACKING SPECIFICATION



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12. APPENDIXES

APPENDIX 1: DEFINITIONS

A. DEFINITION OF CHROMATICITY COORDINATE

The chromaticity coordinate is defined as the coordinate value on the CIE 1931 color chart for R, G, B, W.

B. DEFINITION OF CONTRAST RATIO

The contrast ratio is defined as the following formula:

C. DEFINITION OF RESPONSE TIME

The definition of turn-on response time Tr is the time interval between a pixel reaching 10% of steady state luminance and 90% of steady state luminance. The definition of turn-off response time Tf is the time interval between a pixel reaching 90% of steady state luminance and 10% of steady state luminance. It is shown in Figure 2.

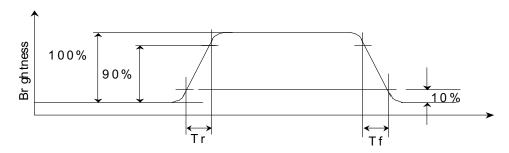


Figure 2: Response time

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D. DEFINITION OF VIEWING ANGLE

The viewing angle is defined as Figure 3. Horizontal and vertical (H & V) angles are determined for viewing directions where luminance varies by 50% of the perpendicular value.

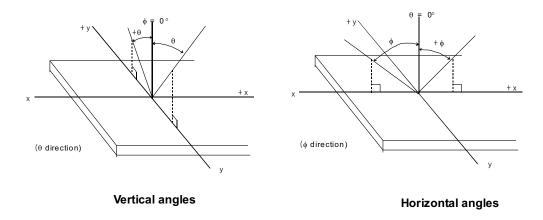


Figure 3: Viewing Angle

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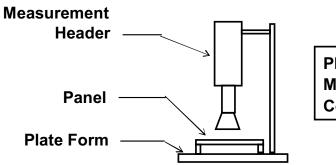




APPENDIX 2: MEASUREMENT APPARATUS

A. LUMINANCE/COLOR COORDINATE

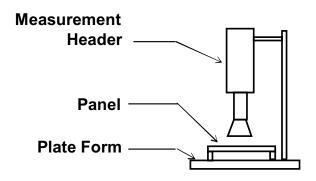
PHOTO RESEARCH PR-705, MINOLTA CS-100



PR-705 / MINOLTA CS-100 Color Analyzer

B. CONTRAST / RESPONSE TIME / VIEW ANGLE

WESTAR CORPORATION FPM-510



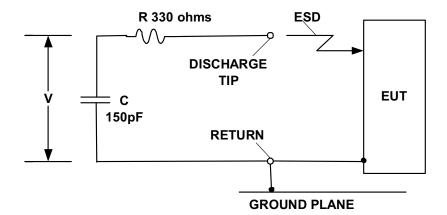
Westar FPM-510 Display Contrast / Response time / View angle Analyzer

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C. ESD ON AIR DISCHARGE MODE



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APPENDIX 3: PRECAUTIONS

A. RESIDUE IMAGE

Because the pixels are lighted in different time, the luminance of active pixels may reduce or differ from inactive pixels. Therefore, the residue image will occur. To avoid the residue image, every pixel needs to be lighted up uniformly.

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Displays

US Micro Products is an industrial distributor specializing in engineered display solutions. We dedicate ourselves to providing the best in displays for the medical, industrial, gaming, automotive, aerospace, military and consumer markets.

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Passive LCDs



TFT Display



Multitouch



Open Frame Monitors



Touch Screen



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Trackballs



Aerospace Trackballs



Printers



