



**US Micro Products**  
*Electronic Products for the OEM*

# OLED PRODUCT SPECIFICATION

Manufactured by:



<b>PART NUMBER:</b>	<b>USMP-P19401</b>
<b>DESCRIPTION:</b>	1.6", 128 x 64, Yellow, COF, SSD1325 IC

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## REVISION RECORD

REV.	REVISION DESCRIPTION	REV. DATE	REMARK
X01	INITIAL RELEASE	2007. 12. 21	
X02	<ul style="list-style-type: none"> <li>■ Add the operating conditions for different luminance</li> <li>■ Add the panel electrical specifications</li> <li>■ Modify power off sequence</li> <li>■ Add the application circuit</li> <li>■ Modify tape</li> </ul>	2008. 02. 13	Page 6, 7, 8, 16, 17 & 19

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## **1. SCOPE**

This specification is to define the general provisions and quality requirements that apply to the supply of display cells manufactured by RiTdisplay. This document, together with the Module Ass'y Drawing, is the highest-level specification for this product.

## **2. WARRANTY**

RiTdisplay warrants that the products delivered pursuant to this specification (or order) will conform to the agreed specifications for twelve (12) months from the shipping date ("Warranty Period"). RiTdisplay is obligated to repair or replace the products which are found to be defective or inconsistent with the specifications during the Warranty Period without charge, on condition that the products are stored or used as the conditions specified in the specifications. Nevertheless, RiTdisplay is not obligated to repair or replace the products without charge if the defects or inconsistency are caused by the force majeure or the reckless behaviors of the customer.

After the Warranty Period, all repairs or replacements of the products are subject to charge.

## **3. FEATURES**

- Small molecular organic light emitting diode
- Color : Yellow
- Panel matrix : 128\*64
- Driver IC : SSD1325
- Excellent quick response time.
- Extremely thin thickness for best mechanism design : 1.61mm
- High contrast : 2000:1
- Wide viewing angle : 160°
- 8-bit 6800-series parallel interface, 8-bit 8080-series parallel interface, serial peripheral interface
- Wide range of operating temperature : -40 to 70 °C
- Anti-glare polarizer.

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#### 4. MECHANICAL DATA

NO	ITEM	SPECIFICATION	UNIT
1	Dot Matrix	128 (W) x 64 (H)	dot
2	Dot Size	0.255 (W) x 0.255 (H)	mm <sup>2</sup>
3	Dot Pitch	0.285 (W) x 0.285 (H)	mm <sup>2</sup>
4	Aperture Rate	80	%
5	Active Area	36.45 (W) x 18.21 (H)	mm <sup>2</sup>
6	Panel Size	41.9 (W) x 28 (H)	mm <sup>2</sup>
7	Panel Thickness	1.61 ± 0.1	mm
8	Module Size	41.9 (W) x 65.1 (H) x 1.61 (D)	mm <sup>3</sup>
9	Diagonal A/A size	1.6	inch
10	Module Weight	TBD	gram

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## 5. MAXIMUM RATINGS

ITEM	MIN	MAX	UNIT	Condition	Remark
Supply Voltage ( $V_{DD}$ )	-0.3	3.5	V	$T_a = 25^\circ\text{C}$	IC maximum rating
Supply Voltage ( $V_{CC}$ )	8	16	V	$T_a = 25^\circ\text{C}$	IC maximum rating
Operating Temp.	-40	70	$^\circ\text{C}$		
Storage Temp	-40	85	$^\circ\text{C}$		
Humidity	-	85	%		
Life Time	24,000	-	Hrs	100 cd/m <sup>2</sup> , 50% checkerboard	Note (1)
Life Time	30,000	-	Hrs	80 cd/m <sup>2</sup> , 50% checkerboard	Note (2)
Life Time	40,000	-	Hrs	60 cd/m <sup>2</sup> , 50% checkerboard	Note (3)

Note:

(A) Under  $V_{CC} = 14\text{V}$ ,  $T_a = 25^\circ\text{C}$ , 50% RH.

(B) Life time is defined the amount of time when the luminance has decayed to less than 50% of the initial measured luminance.

(1) Setting of 100 cd/m<sup>2</sup> :

- Contrast setting : 0x68H
- Frame rate : 105Hz
- Duty setting : 1/64

(2) Setting of 80 cd/m<sup>2</sup> :

- Contrast setting : 0x4FH
- Frame rate : 105Hz
- Duty setting : 1/64

(3) Setting of 60 cd/m<sup>2</sup> :

- Contrast setting : 0x3AH
- Frame rate : 105Hz
- Duty setting : 1/64

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## 6. ELECTRICAL CHARACTERISTICS

### 6.1 D.C ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETERS	TEST CONDITION	MIN	TYP	MAX	UNIT
$V_{CC}$	Analog power supply (for OLED panel)	Ta=-20 °C to +70°C	13.5	14	14.5	V
$V_{DD}$	Digital power supply	Ta=-20 °C to +70°C	2.4	2.7	3.5	V
$I_{DD}$	Operating current for $V_{DD}$ $V_{DD} = 2.7V$ , $V_{CC} = 12V$ , $I_{REF} = 10\mu A$ No panel attached, All Display ON	Contrast=7F	-	-	650	$\mu A$
$I_{CC}$	Operating current for $V_{CC}$ $V_{DD} = 2.7V$ , $V_{CC} = 12V$ , $I_{REF} = 10\mu A$ No panel attached, All Display ON	Contrast=7F	-	700	-	$\mu A$
$V_{IH}$	Hi logic input level		0.8* $V_{DD}$	-	$V_{DD}$	V
$V_{IL}$	Low logic input level		0	-	0.2* $V_{DD}$	V
$V_{OH}$	Hi logic output level		0.9* $V_{DD}$	-	$V_{DD}$	V
$V_{OL}$	Low logic output level		0	-	0.1* $V_{DD}$	V
$I_{SEG}$	Segment on output current $V_{DD}=2.7V$ , $V_{CC}=12V$ , $I_{REF}=10\mu A$ , Display on, Segment pin under test is connected with a 20K resistive load to $V_{SS}$	Contrast=7F	270	300	370	$\mu A$
		Contrast=5F	-	225	-	$\mu A$
		Contrast=3F	-	150	-	$\mu A$
		Contrast=1F	-	75	-	$\mu A$

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## 6.2 ELECTRO-OPTICAL CHARACTERISTICS

### PANEL ELECTRICAL SPECIFICATIONS

PARAMETER	MIN	TYP.	MAX	UNITS	COMMENTS
Normal mode current		18	20	mA	All pixels on (1)
Standby mode current		1	2	mA	Standby mode 10% pixels on (2)
Normal mode power consumption		252	280	mW	All pixels on (1)
Standby mode power consumption		14	28	mW	Standby mode 10% pixels on (2)
Normal Luminance	60	80		cd/m <sup>2</sup>	Display Average
Standby Luminance		10		cd/m <sup>2</sup>	Display Average
CIE <sub>x</sub> (Yellow)	0.43	0.47	0.51		x, y (CIE 1931)
CIE <sub>y</sub> (Yellow)	0.45	0.49	0.53		
Dark Room Contrast	2000:1				
Viewing Angle	160			degree	
Response Time		10		μs	

(1) Normal mode condition :

- Driving Voltage : 14V
- Contrast setting : 0x4FH
- Frame rate : 105Hz
- Duty setting : 1/64

(2) Standby mode condition :

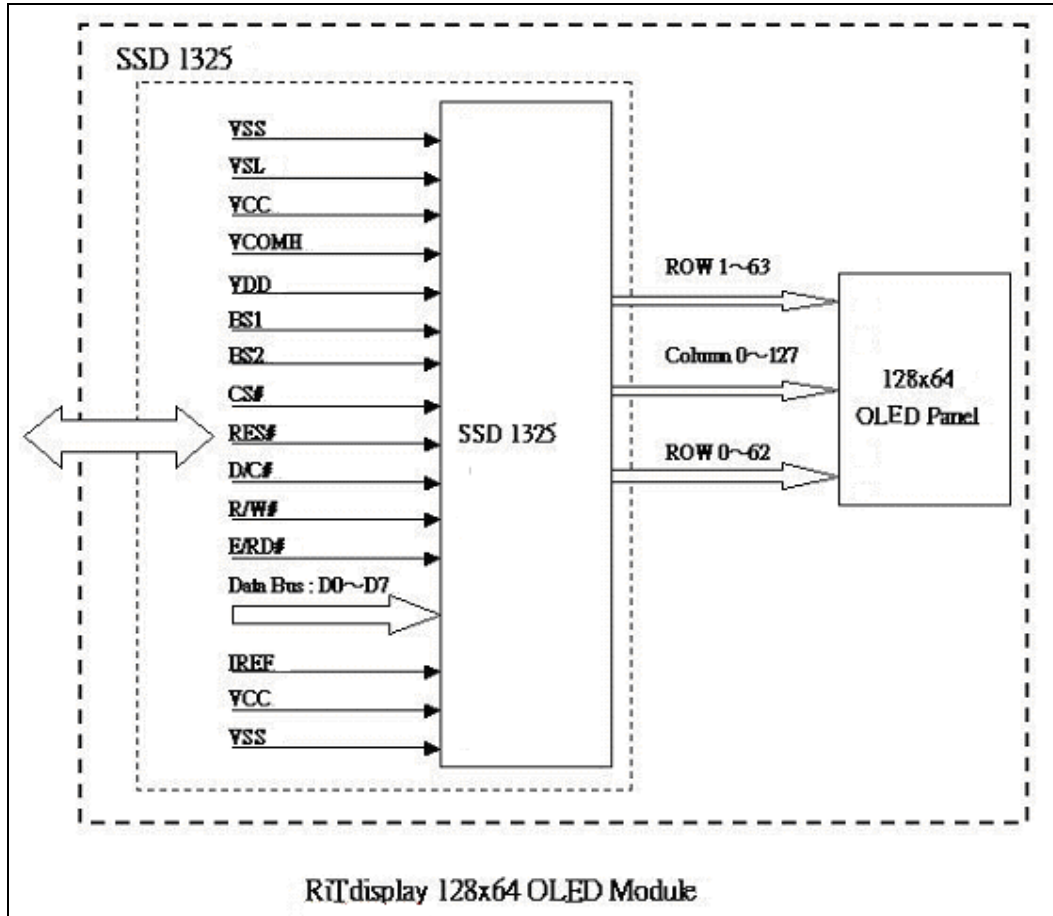
- Driving Voltage : 14V
- Contrast setting : 0x04H
- Frame rate : 105Hz
- Duty setting : 1/64
- 

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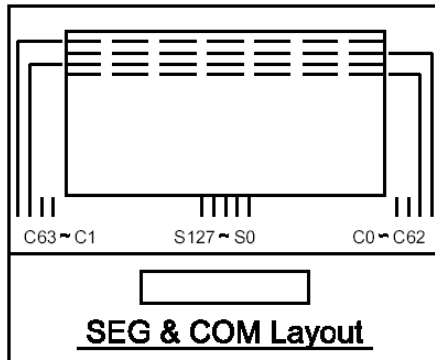
## 7. INTERFACE

### 7.1 FUNCTION BLOCK DIAGRAM



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### 7.2 PANEL LAYOUT DIAGRAM



### 7.3 PIN ASSIGNMENTS

Pin No.	Pin Name	TYPE	Description
1	VSS	I	This is a ground pin.
2	VSL	O	This pin is the output pin for the voltage output low level for SEG signals. This pin can be kept NC or connected with a capacitor to VSS for stability.
3	VCC	I	Positive OLED high voltage power supply
4	VCOMH	O	The COM voltage reference pin, this pin should be connected to ground through a capacitor.
5	VDD	I	Voltage power supply for logic
6	BS1	-	Interface select pin
7	BS2	-	Interface select pin
8	CS#	I	Chip select pin. The driver IC will be selected When CS pin is active low.
9	RES#	I	Hardware reset signal
10	D/C#	I	Data/Command control pin. When it pulled high, the input at D0-D7 is treated as display data. When it pulled low, the input at D0-D7 is transferred to command register
11	R/W#	I	Write strobe signal and reads data at the low level
12	E(RD#)	I	Read strobe signal and reads data at the low level
13	D0	I/O	8-bit data bus
14	D1	I/O	8-bit data bus
15	D2	I/O	8-bit data bus
16	D3	I/O	8-bit data bus
17	D4	I/O	8-bit data bus
18	D5	I/O	8-bit data bus
19	D6	I/O	8-bit data bus
20	D7	I/O	8-bit data bus
21	IREF	I	The current reference input pin, this pin should be connected to ground through a resistor.
22	VCC	I	Positive OLED high voltage power supply
23	NC	I	No connection.
24	VSS	I	This is a ground pin.

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### 7.4 GRAPHIC DISPLAY DATA RAM ADDRESS MAP

The GDDRAM is a bit mapped static RAM holding the bit pattern to be displayed. The size of the RAM is 128x80x4 bits. For mechanical flexibility, re-mapping on both Segment and Common outputs can be selected by software. (Refer to Table 3-7 for GDDRAM address map description)

		SEG0	SEG1	SEG2	SEG3		SEG124	SEG125	SEG126	SEG127	SEG Outputs Column Address (HEX)
		00		01			3E		3F		
COM0	00	D0[3:0]	D0[7:4]	D1[3:0]	D1[7:4]		D62[3:0]	D62[7:4]	D63[3:0]	D63[7:4]	
COM1	01	D64[3:0]	D64[7:4]	D65[3:0]	D65[7:4]		D126[3:0]	D126[7:4]	D127[3:0]	D127[7:4]	
COM78	4E	D4992[3:0]	D4992[7:4]	D4993[3:0]	D4993[7:4]		D5054[3:0]	D5054[7:4]	D5055[3:0]	D5055[7:4]	
COM79	4F	D5056[3:0]	D5056[7:4]	D5057[3:0]	D5057[7:4]		D5118[3:0]	D5118[7:4]	D5119[3:0]	D5119[7:4]	
COM Outputs	Row Address (HEX)										

(Display Startline=0)

**Table 3– GDDRAM address map showing Horizontal Address Increment A[2]=0, Column Address Re-map A[0]=0, Nibble Re-map A[1]=0, COM Re-map A[4]=0, and Display Start Line=00H (Data byte sequence: D0, D1, ... , D5118, D5119)**

		SEG0	SEG1	SEG2	SEG3		SEG124	SEG125	SEG126	SEG127	SEG Outputs Column Address (HEX)
		00		01			3E		3F		
COM0	00	D0[3:0]	D0[7:4]	D80[3:0]	D80[7:4]		D4960[3:0]	D4960[7:4]	D5040[3:0]	D5040[7:4]	
COM1	01	D1[3:0]	D1[7:4]	D81[3:0]	D81[7:4]		D4961[3:0]	D4961[7:4]	D5041[3:0]	D5041[7:4]	
COM78	4E	D78[3:0]	D78[7:4]	D158[3:0]	D158[7:4]		D5038[3:0]	D5038[7:4]	D5118[3:0]	D5118[7:4]	
COM79	4F	D79[3:0]	D79[7:4]	D159[3:0]	D159[7:4]		D5039[3:0]	D5039[7:4]	D5119[3:0]	D5119[7:4]	
COM Outputs	Row Address (HEX)										

(Display Startline=0)

**Table 4–GDDRAM address map showing Vertical Address Increment A[2]=1, Column Address Re-map A[0]=0, Nibble Re-map A[1]=0, COM Re-map A[4]=0, and Display Start Line=00H (Data byte sequence: D0, D1, ... , D5118, D5119)**

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		SEG0	SEG1	SEG2	SEG3		SEG124	SEG125	SEG126	SEG127	SEG Outputs Column Address (HEX)
		3F		3E			01		00		
COM0	00	D63[7:4]	D63[3:0]	D62[7:4]	D62[3:0]		D1[7:4]	D1[3:0]	D0[7:4]	D0[3:0]	
COM1	01	D127[7:4]	D127[3:0]	D126[7:4]	D126[3:0]		D65[7:4]	D65[3:0]	D64[7:4]	D64[3:0]	
		←									
COM78	4E	D5055[7:4]	D5055[3:0]	D5054[7:4]	D5054[3:0]		D4993[7:4]	D4993[3:0]	D4992[7:4]	D4992[3:0]	
COM79	4F	D5119[7:4]	D5119[3:0]	D5118[7:4]	D5118[3:0]		D5057[7:4]	D5057[3:0]	D5056[7:4]	D5056[3:0]	

COM Outputs      Row Address (HEX)  
(Display Startline=0)

**Table 5—GDDRAM address map showing Horizontal Address Increment A[2]=0, Column Address Re-map A[0]=1, Nibble Re-map A[1]=1, COM Re-map A[4]=0, and Display Start Line=00H (Data byte sequence: D0, D1, ... , D5118, D5119)**

		SEG0	SEG1	SEG2	SEG3		SEG124	SEG125	SEG126	SEG127	SEG Outputs Column Address (HEX)
		00		01			3E		3F		
COM15	0F	D0[3:0]	D0[7:4]	D1[3:0]	D1[7:4]		D62[3:0]	D62[7:4]	D63[3:0]	D63[7:4]	
COM14	0E	D64[3:0]	D64[7:4]	D65[3:0]	D65[7:4]		D126[3:0]	D126[7:4]	D127[3:0]	D127[7:4]	
		→									
COM17	11	D4992[3:0]	D4992[7:4]	D4993[3:0]	D4993[7:4]		D5054[3:0]	D5054[7:4]	D5055[3:0]	D5055[7:4]	
COM16	10	D5056[3:0]	D5056[7:4]	D5057[3:0]	D5057[7:4]		D5118[3:0]	D5118[7:4]	D5119[3:0]	D5119[7:4]	

COM Outputs      Row Address (HEX)  
(Display Startline=10H)

**Table 6—GDDRAM address map showing Horizontal Address Increment A[2]=0, Column Address Re-map A[0]=0, Nibble Re-map A[1]=0, COM Re-map A[4]=1, and Display Start Line=16H (Data byte sequence: D0, D1, ... , D5118, D5119)**

		SEG0	SEG1	SEG2	SEG3		SEG124	SEG125	SEG126	SEG127	SEG Outputs Column Address (HEX)
		00		01			3E		3F		
COM0	00										
COM1	01			D0[3:0]	D0[7:4]		D61[3:0]	D61[7:4]			
		→									
COM78	4E			D4774[3:0]	D4774[7:4]		D4835[3:0]	D4835[7:4]			
COM79	4F										

COM Outputs      Row Address (HEX)  
(Display Startline=0)

**Table 7—GDDRAM address map showing Horizontal Address Increment A[2]=0, Column Address Re-map A[0]=0, Nibble Re-map A[1]=0, COM Re-map A[4]=0, Display Start Line=00H (Data byte sequence: D0, D1, ... , D4834, D4835), Column Start Address=01H, Column End Address=3EH, Row Start Address=01H and Row End Address=4EH**

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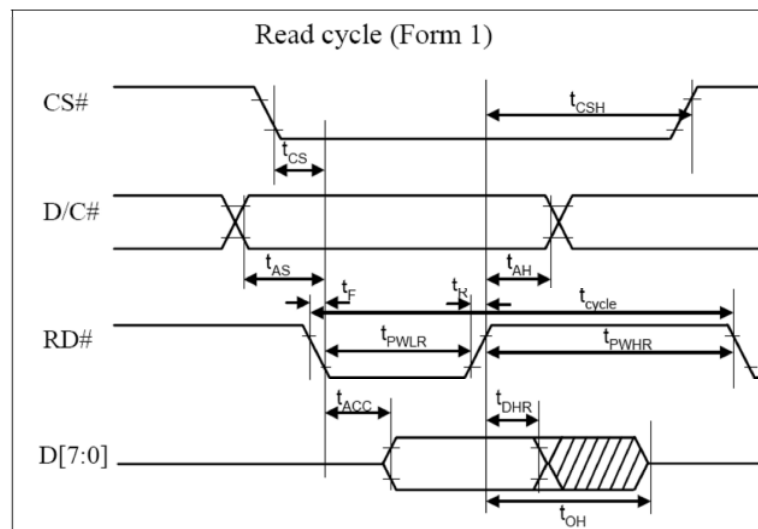
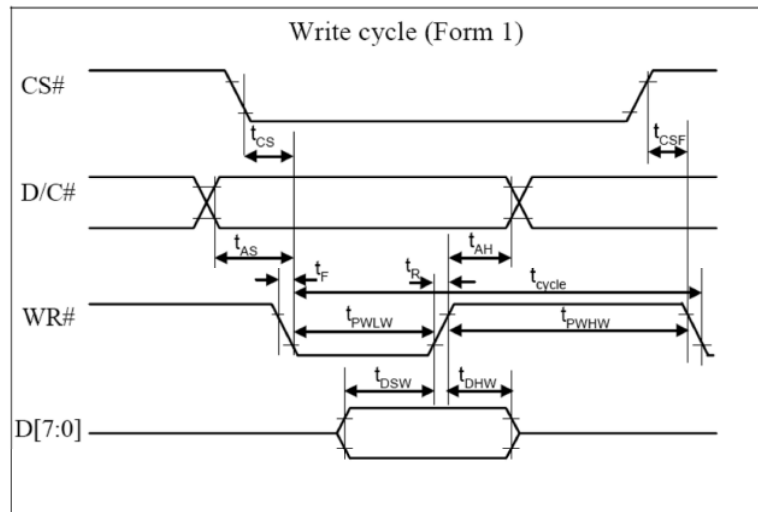
### 7.5 INTERFACE TIMING CHART

#### 8080-Series MPU Parallel Interface Timing Characteristics

( $V_{DD} - V_{SS} = 2.4$  to  $3.5V$ ,  $T_A = 25^\circ C$ )

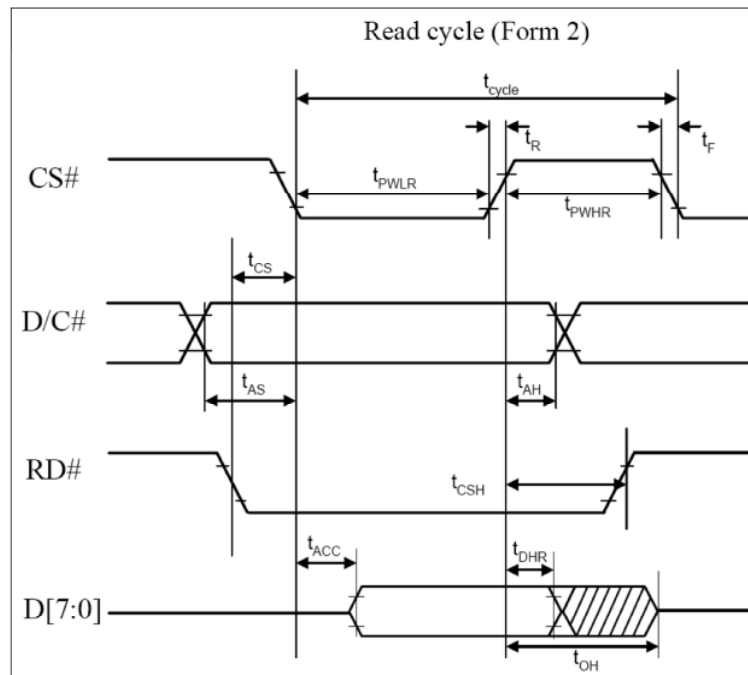
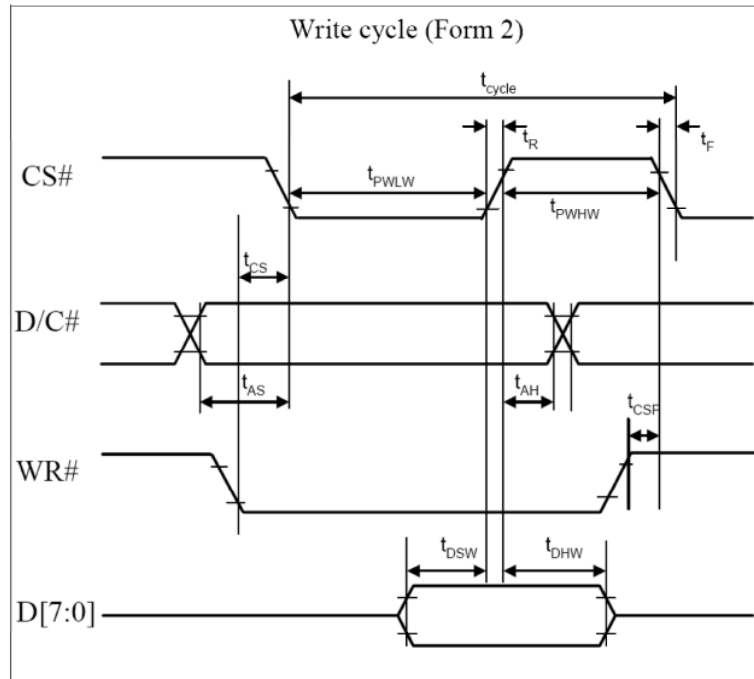
Symbol	Parameter	Min	Typ	Max	Unit
$t_{cycle}$	Clock Cycle Time	300	-	-	ns
$t_{AS}$	Address Setup Time	10	-	-	ns
$t_{AH}$	Address Hold Time	0	-	-	ns
$t_{DSW}$	Write Data Setup Time	40	-	-	ns
$t_{DHW}$	Write Data Hold Time	15	-	-	ns
$t_{DHR}$	Read Data Hold Time	20	-	-	ns
$t_{OH}$	Output Disable Time	-	-	70	ns
$t_{ACC}$	Access Time	-	-	140	ns
$t_{PWLr}$	Read Low Time	120	-	-	ns
$t_{PWLW}$	Write Low Time	60	-	-	ns
$t_{PWHr}$	Read High Time	60	-	-	ns
$t_{PWHW}$	Write High Time	60	-	-	ns
$t_R$	Rise Time	-	-	15	ns
$t_F$	Fall Time	-	-	15	ns
$t_{CS}$	Chip select setup time	0	-	-	ns
$t_{CSH}$	Chip select hold time to read signal	0	-	-	ns
$t_{CSF}$	Chip select hold time	20	-	-	ns

#### 8080-series parallel interface characteristics (Form 1)



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**8080-series parallel interface characteristics (Form2)**



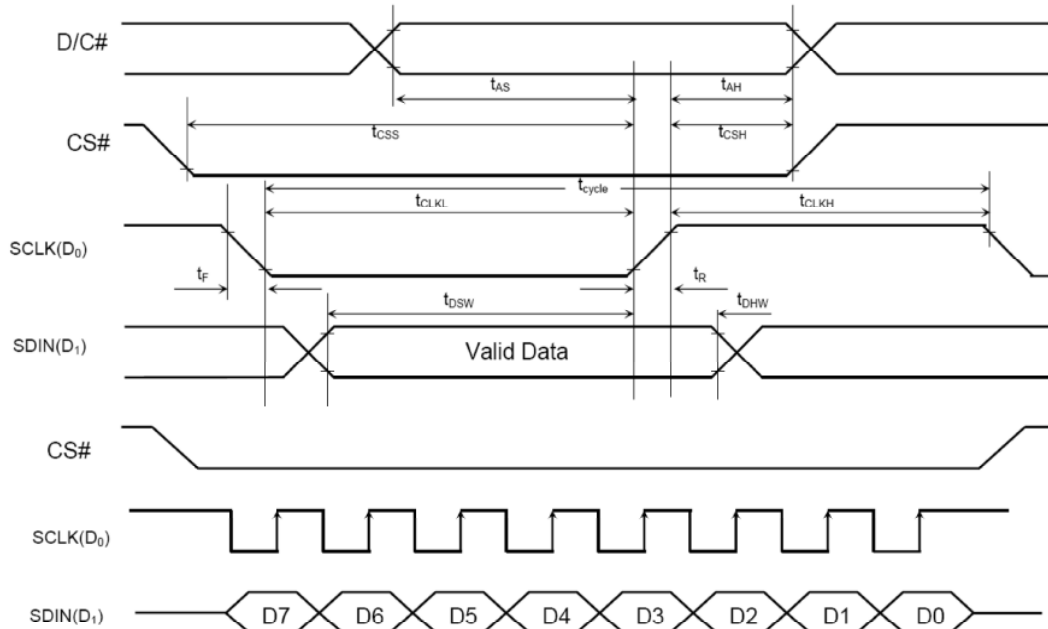
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### Serial Interface Timing Characteristics

( $V_{DD} - V_{SS} = 2.4$  to  $3.5V$ ,  $T_A = 25^\circ C$ )

Symbol	Parameter	Min	Typ	Max	Unit
$t_{cycle}$	Clock Cycle Time	250	-	-	ns
$t_{AS}$	Address Setup Time	150	-	-	ns
$t_{AH}$	Address Hold Time	150	-	-	ns
$t_{CSS}$	Chip Select Setup Time	120	-	-	ns
$t_{CSH}$	Chip Select Hold Time	60	-	-	ns
$t_{DSW}$	Write Data Setup Time	100	-	-	ns
$t_{DHW}$	Write Data Hold Time	100	-	-	ns
$t_{CLKL}$	Clock Low Time	100	-	-	ns
$t_{CLKH}$	Clock High Time	100	-	-	ns
$t_R$	Rise Time	-	-	15	ns
$t_F$	Fall Time	-	-	15	ns

### Serial Interface Characteristics



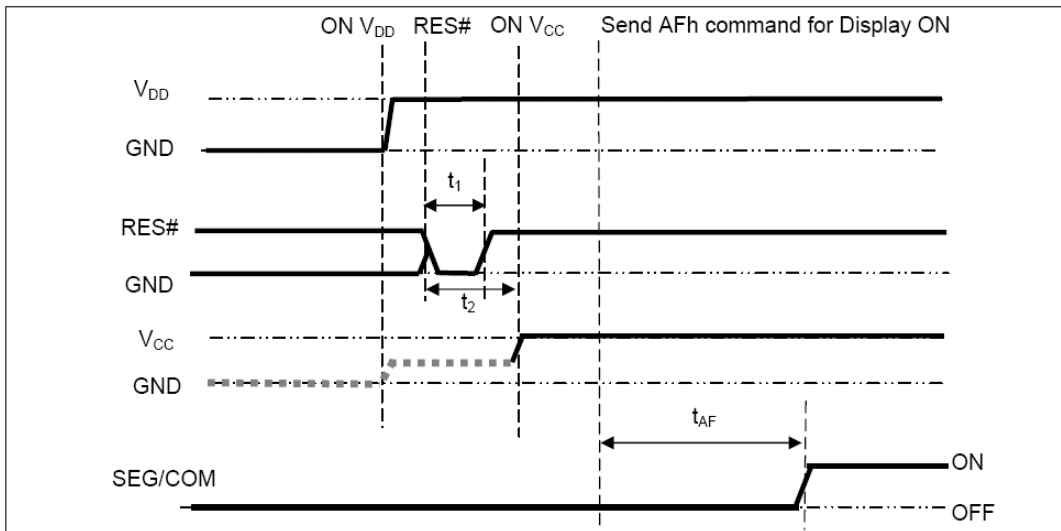
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## 8. POWER ON / OFF SEQUENCE & APPLICATION CIRCUIT

### 8.1 POWER ON / OFF SEQUENCE

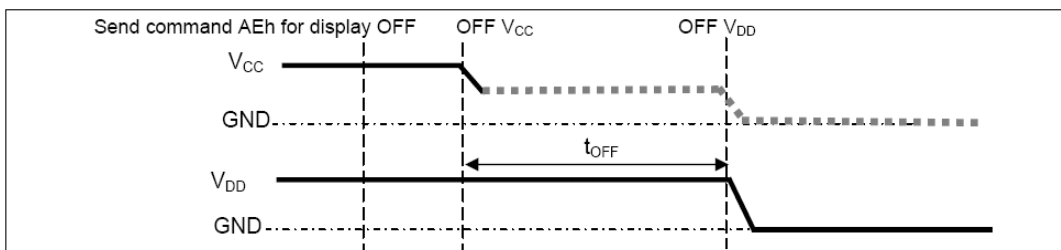
#### Power ON sequence:

1. Power ON V<sub>DD</sub>.
2. After V<sub>DD</sub> become stable, set RES# pin LOW (logic low) for at least 3us(t<sub>1</sub>) and then HIGH (logic high).
3. After set RES# pin LOW (logic low), wait for at least 3us(t<sub>2</sub>). Then Power ON V<sub>CC</sub>.(1)
4. After V<sub>CC</sub> become stable, send command AFh for display ON. SEG/COM will be ON after 100ms(t<sub>AF</sub>).



#### Power OFF sequence:

1. Send command AEh for display OFF.
2. Wait until panel discharges completely.
3. Power OFF V<sub>CC</sub>. (1), (2)
4. Wait for t<sub>OFF</sub>. Power OFF V<sub>DD</sub>. (where Minimum t<sub>OFF</sub>=80ms, Typical t<sub>OFF</sub>=100ms )

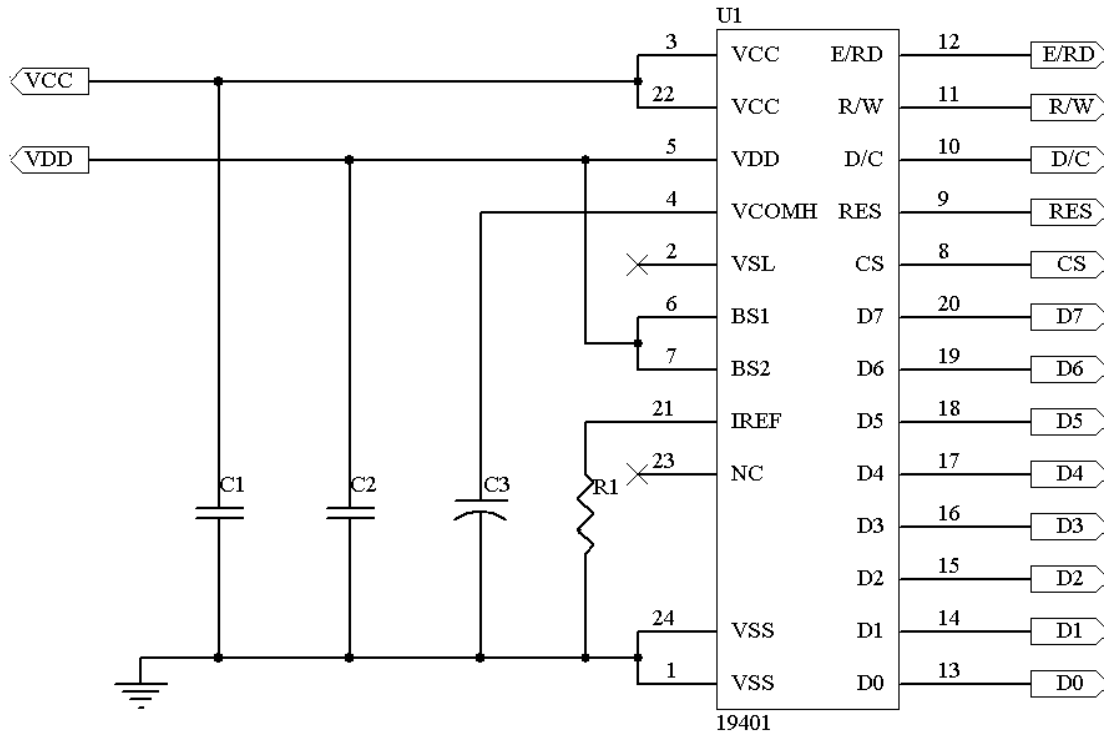


#### Note:

- (1) Since an ESD protection circuit is connected between V<sub>DD</sub> and V<sub>CC</sub>, V<sub>CC</sub> becomes lower than V<sub>DD</sub> whenever V<sub>DD</sub> is ON and V<sub>CC</sub> is OFF as shown in the dotted line of V<sub>CC</sub> in above figures.
- (2) V<sub>CC</sub> should be disabled when it is OFF.



## 8.2 APPLICATION CIRCUIT



### Recommend components:

C1: 2.2uF/25V (0805)

C2: 1uF/16V (0603)

C3: 4.7uF/25V (TANTALUM or Solid Tantalum 4.7uF/ 25V/ A Case (Vishay 572D))

R1: 1M ohm/1% (0603)

**Notes: This circuit is for 8080 interface.**

## 8.3 COMMAND TABLE

Refer to SSD1325 IC Spec.

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## 9. RELIABILITY TEST CONDITIONS

No.	Items	Specification	Quantity
1	High temp. (Non-operation)	85°C, 240hrs	5
2	High temp. (Operation)	70°C, 120hrs	5
3	Low temp. (Operation)	-40°C, 120hrs	5
4	High temp. / High humidity (Operation)	65°C, 90%RH, 120hrs	5
5	Thermal shock (Non-operation)	-40°C ~85°C (-40°C /30min; transit /3min; 85°C /30min; transit /3min) 1cycle: 66min, 100 cycles	5
6	Vibration	Frequency : 5~50HZ, 0.5G Scan rate : 1 oct/min Time : 2 hrs/axis Test axis : X, Y, Z	1 Carton
7	Drop	Height: 120cm Sequence : 1 angle 、 3 edges and 6 faces Cycles: 1	1 Carton
8	ESD (Non-operation)	Air discharge model, ±8kV, 10 times	5

### Test and measurement conditions

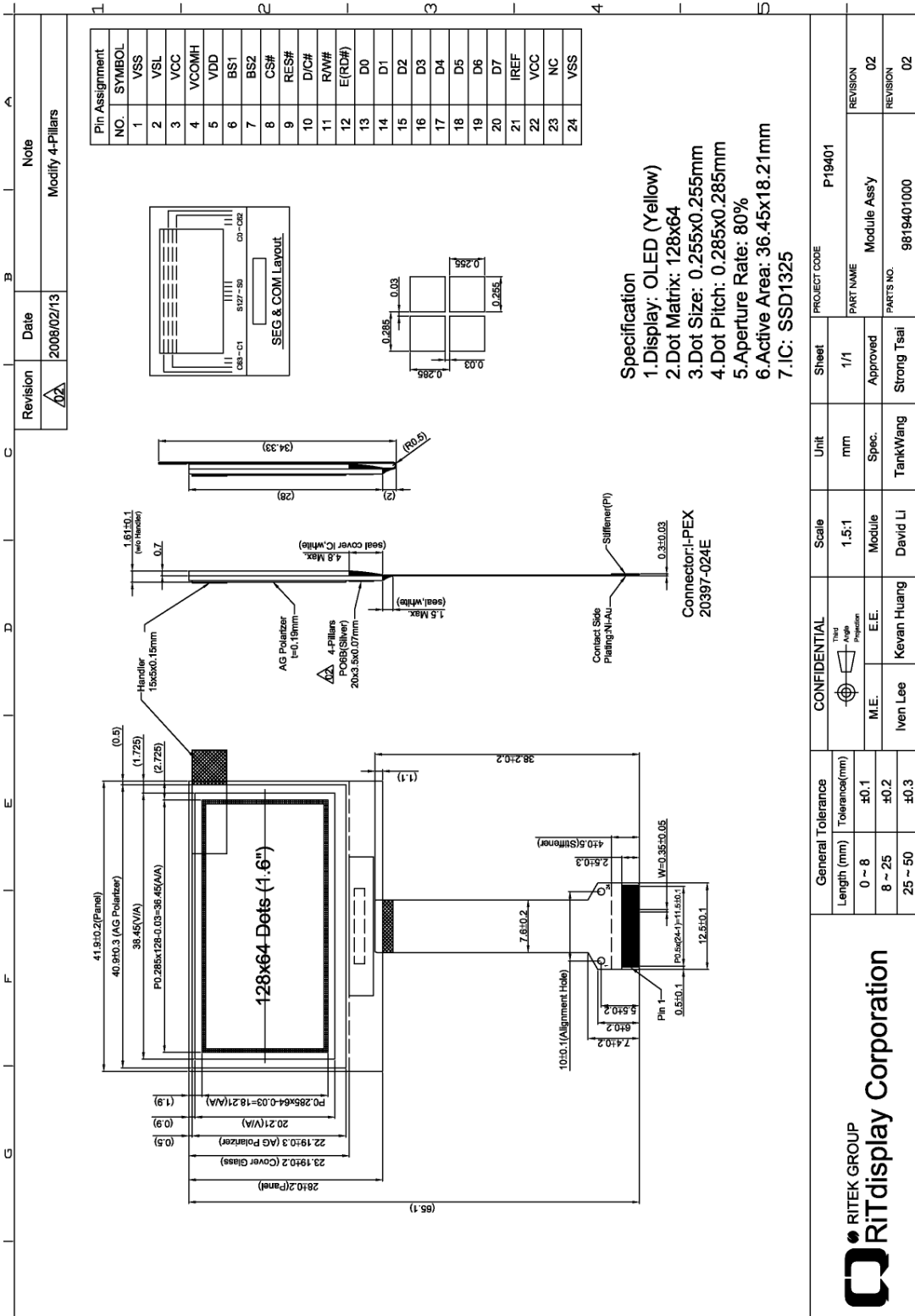
1. All measurements shall not be started until the specimens attain to temperature stability.
2. All-pixels-on is used as operation test pattern.
3. The degradation of Polarizer are ignored for item 1, 4 & 5.

### Evaluation criteria

1. The function test is OK.
2. No observable defects.
3. Luminance: > 50% of initial value.
4. Current consumption: within  $\pm$  50% of initial value.

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**10. EXTERNAL DIMENSION**



## 11. PACKING SPECIFICATION

TBD

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**12. APPENDIXES**

**APPENDIX 1: DEFINITIONS**

**A. DEFINITION OF CHROMATICITY COORDINATE**

The chromaticity coordinate is defined as the coordinate value on the CIE 1931 color chart for R, G, B, W.

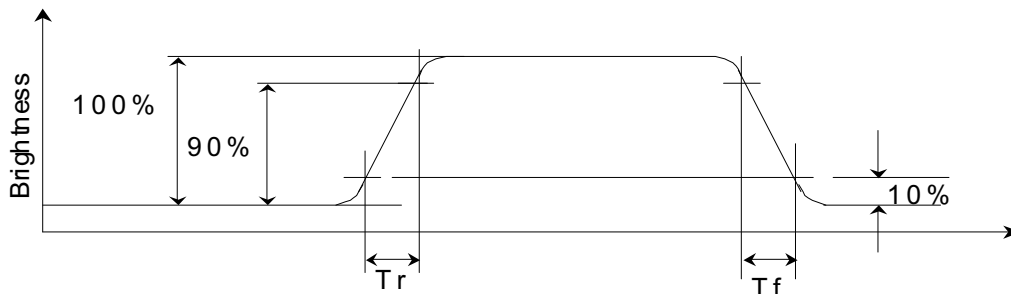
**B. DEFINITION OF CONTRAST RATIO**

The contrast ratio is defined as the following formula:

$$\text{Contrast Ratio} = \frac{\text{Luminance of all pixels on measurement}}{\text{Luminance of all pixels off measurement}}$$

**C. DEFINITION OF RESPONSE TIME**

The definition of turn-on response time  $T_r$  is the time interval between a pixel reaching 10% of steady state luminance and 90% of steady state luminance. The definition of turn-off response time  $T_f$  is the time interval between a pixel reaching 90% of steady state luminance and 10% of steady state luminance. It is shown in Figure 2.

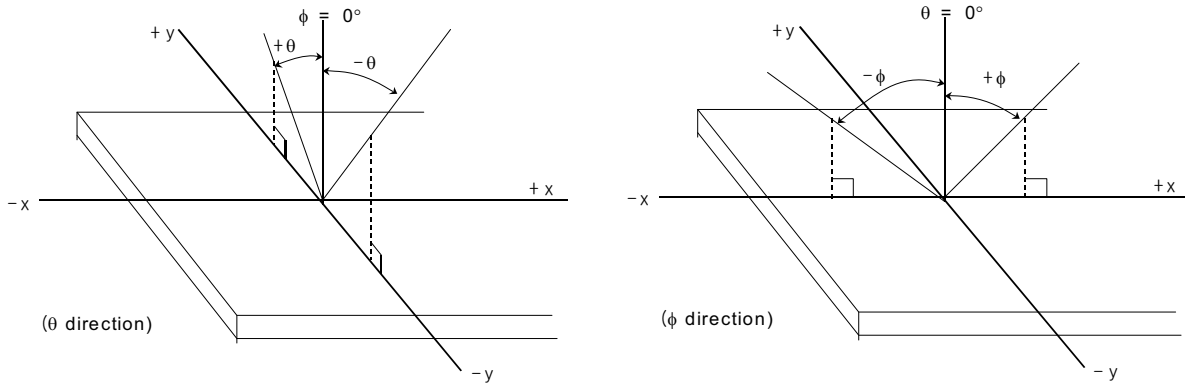


**Figure 2: Response time**

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**D. DEFINITION OF VIEWING ANGLE**

The viewing angle is defined as Figure 3. Horizontal and vertical (H & V) angles are determined for viewing directions where luminance varies by 50% of the perpendicular value.



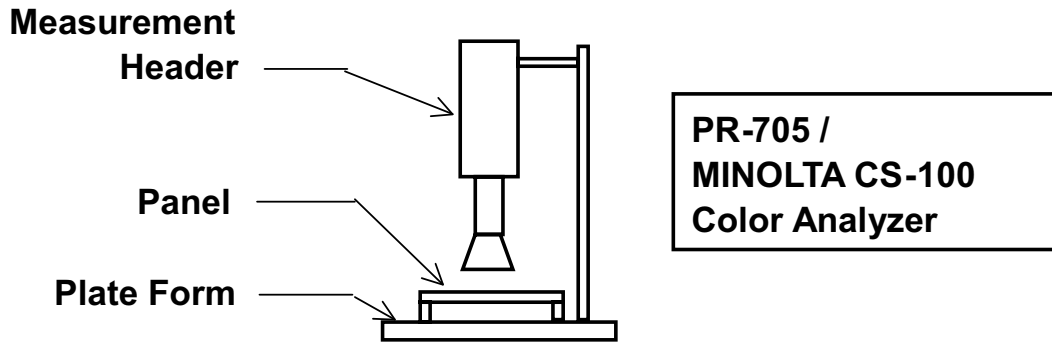
**Figure 3: Viewing Angle**

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**APPENDIX 2: MEASUREMENT APPARATUS**

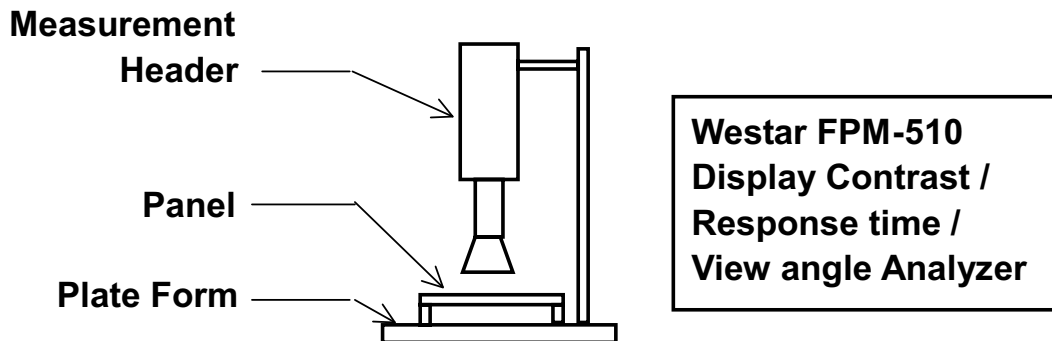
**A. LUMINANCE/COLOR COORDINATE**

PHOTO RESEARCH PR-705, MINOLTA CS-100



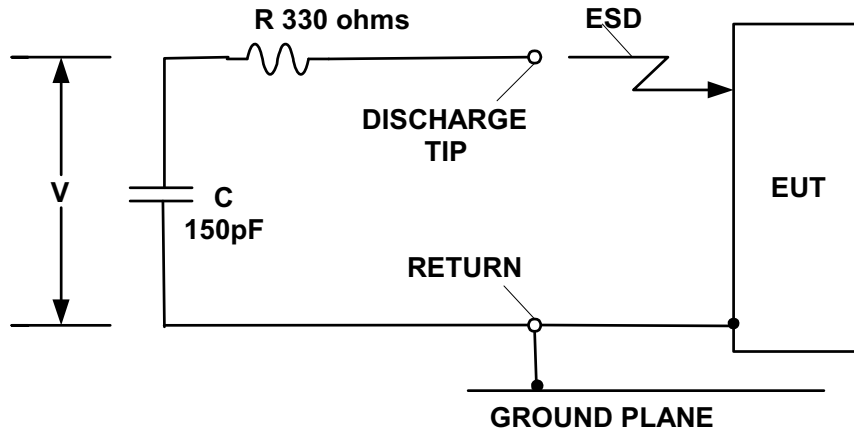
**B. CONTRAST / RESPONSE TIME / VIEW ANGLE**

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**C. ESD ON AIR DISCHARGE MODE**



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## APPENDIX 3: PRECAUTIONS

### A. RESIDUE IMAGE

Because the pixels are lighted in different time, the luminance of active pixels may reduce or differ from inactive pixels. Therefore, the residue image will occur. To avoid the residue image, every pixel needs to be lighted up uniformly.

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