

TFT-LCD PRODUCT SPECIFICATION

PART NUMBER:	USMP-TT024Q-01K
DESCRIPTION:	2.4" Active Matrix TFT-LCD, 240 x 320 RGB, 262K Full Colors

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History of Version

	Date (mm / dd / yyyy)	Ver.	Edi.	Description	Page	Design by
	10/25/2012	01	001	New Drawing	-	Yuan
				Modify Optical Characteristics	6	
	11/02/2012	01	002	Modify Backlight & LED Characteristics	9	Vuon
	11/02/2012	01	002	Modify interface	12,13	Yuan
				Modify FPC	Appendix	
				Modify Counter Drawing	10	
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				Modify FPC	Appendix	
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\bigcirc	01/07/2013	01	004	Modify Drawing	Appendix	Tuan
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Note: For detailed information please refer to IC data sheet: ILITEK - ILI9341



1. SPECIFICATIONS

1.1 Features

Main LCD Panel

	Walli LCD Fallel					
	Item	Standard Value				
	Display Type	240 * (R · G · B) * 320 Dots				
	LCD Type	a-Si TFT , Normally Black VA , Transmissive				
	Screen size(inch)	2.4 (Diagonal)				
	Color configuration	R.G.B. vertical stripe				
	Backlight	White LED				
	Interface	8 /9/16/18 Bit Interface for i80 system and serial /RGB interface				
	Driver IC	ILI9341				
		THIS PRODUCT CONFORMS TO THE ROHS OF USMP				
Ö	ROHS	Detailed information please to refer website:				
Z		http://www.usmicroproducts.com				
1.2	ROHS Mechanical Specifica	tions				
	Item	Standard Value	Unit			
Ξ	Outline Dimension	41.87 (W) * 59.35 (L) * 2.6 (H)max	mm			
ENTIAL	LCD Panel					
•	Item	Standard Value	Unit			

Item	Standard Value	Unit
Outline Dimension	41.87 (W) * 59.35 (L) * 2.6 (H)max	mm

Item	Standard Value	Unit
Viewing Area	38.5 (W) * 50.96(L)	mm
Active Area	36.72(W) * 48.96(L)	mm

Note: For detailed information please refer to LCM drawing



1.3 Absolute Maximum Ratings

Module

Item	Symbol	Condition	Min.	Max.	Unit	
System Dower Supply Voltage	VDD	VDD0.3		4.6	V	
System Power Supply Voltage	VGH-VGL	GND	0	+32	V	
Logic Input Voltage	VIN	-	-0.3	VDD+0.3	V	
Operating Temperature	TOP	-	-20	70	°C	
Storage Temperature	TST	-	-30	80	°C	

1.4 DC Electrical Characteristics

Module

GND = 0V, Ta = 25°C

Item	Symbol	Condition	Min.	Тур.	Max.	Unit
Power Supply Voltage	VDD	-	-	2.8	-	V
Input High Voltage	V _{IH}	-	0.7*VDD	-	VDD	V
Input Low Voltage	V _{IL}	-	GND	-	0.3*VDD	V
Output High Voltage	V _{OH}	IOH=-0.1mA	0.8*VDD	-	VDD	V
Output Low Voltage	V _{OL}	IOL=0.1mA	GND	-	0.2*VDD	V
Supply Current	IDD	VDD = 2.8V	_	(10)	(15)	mA
Oupply Ourient	טטו	Pattern= Full display *1	_	(10)	(13)	

Note 1: Maximum current display



1.5 Optical Characteristics TFT LCD panel

VDD= 2.8 V, Ta=25°C

•				1	1	1		
Item		Symbol	Condition	Min.	Тур.	Max.	unit	
Response time	Rise Fall	Tr+Tf	Ta = 25°C θX, θY = 0°	-	(35)	-	ms	Note2
	Тор	θΥ+		-	(80)	-		
Viewing angle	Bottom	θΥ-	CR ≥ 10	-	(80)	-	Dog	
Viewing angle	Left	θX-	CR 2 10	-	(80)	-	Deg.	Note4
	Right	θX+		-	(80)	-		
Contrast ration	0	CR	Ta = 25° C θ X , θ Y = 0°	-	(500)	-	-	Note3
	White	Х		(0.286)	(0.306)	(0.326)		
	VVIIILE	Υ	Ta = 25°C θX , θY = 0°	(0.298)	(0.318)	(0.338)	-	
0.1(015	Red	Χ		(0.637)	(0.657)	(0.677)		
Color of CIE Coordinate	Red	Υ		(0.306)	(0.326)	(0.346)		Note1
(With B/L & T/P)	Green	Χ		(0.249)	(0.269)	(0.289)		NOLET
(**************************************	Green	Υ		(0.569)	(0.589)	(0.609)		
	Blue	Χ		(0.129)	(0.149)	(0.169)		
	Dide	Υ		(0.060)	(0.080)	(0.100)		
Average Brightr	ness							
Pattern=white display		IV	IF=TBD mA	(180)	(200)	-	cd/m ²	Note1
(With B/L)								
Uniformity (With B/L)		∆B	IF=TBD mA	80	-	-	%	Note1



Note1:

*1 : △B=B(min) / B(max) * 100%

*2 : Measurement Condition for Optical Characteristics:

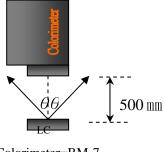
a: Environment: 25°C±5°C / 60±20%R.H, no wind, dark room below 10 Lux at typical lamp current and typical operating frequency.

b : Measurement Distance: $500 \pm 50 \text{ mm}$, $(\theta = 0^{\circ})$

c: Equipment: TOPCON BM-7 fast, (field 1°), after 10 minutes operation.

d: The uncertainty of the C.I.E coordinate measurement ±0.01, Average Brightness ± 4%





Colorimeter=BM-7

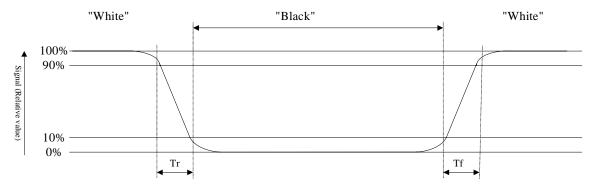
To be measured at the center area of panel with a viewing cone of 1? by Topcon luminance meter BM-7, after 10 minutes operation (module)

Note2: Definition of response time:

The output signals of photo detector are measured when the input signals are changed from "black" to "white" (falling time) and from "white" to "black" (rising time), respectively. The response time is defined as the time interval between the 10% and 90% of Amplitudes.

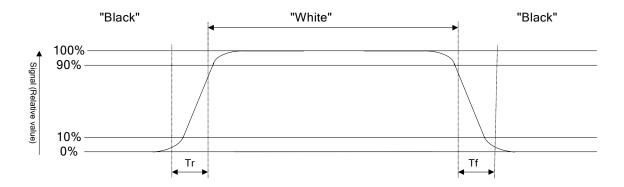
Refer to figure as below:

Normally White





Normally Black



Note3: Definition of contrast ratio:

Contrast ratio is calculated with the following formula

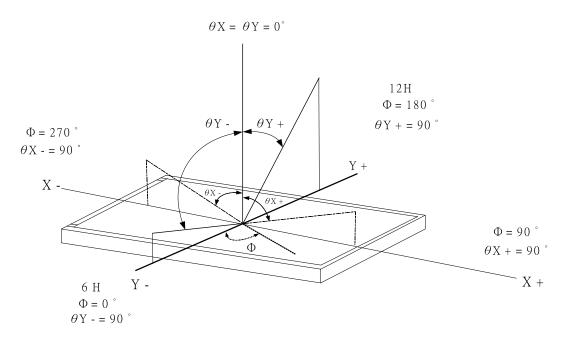
Photo detector output when LCD is at "White" state

Contrast ratio (CR) =

Photo detector output when LCD is at "Black" state

Note4: Definition of viewing angle:

Refer to figure as below:





Backlight & LED Characteristics 1.6

LCD Module with LED Backlight

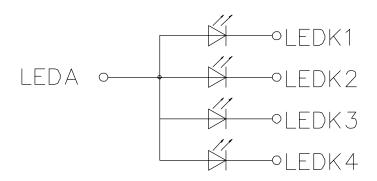
Maximum Ratings

Item	Symbol	Conditions	Min.	Max.	Unit
Forward Current	IF	Ta =25°ℂ	-	TBD	mA
Reverse Voltage	VR	Ta =25°ℂ	-	TBD	V

Electrical / Optical Characteristics

	Item	Symbol	Conditions	Min.	Тур.	Max.	Unit
	Forward Voltage	VF		(2.9)	(3.2)	(3.5)	V
CO	Average Brightness (without LCD)	IV	IF= TBD mA	(5000)	-	-	cd/m ²
ONFID	Color of CIE Coordinate*1	Х		(0.25)	(0.275)	(0.3)	*2
	(Without LCD)	Υ		(0.25)	(0.275)	(0.3)	
DE	Color			White			
Z *1: ⁷	Γhis value will be changed wh ∆B=B(min) / B(max) *100%	nile mass pro	oduction.				

*2 : △B=B(min) / B(max) *100% B/L Internal Circuit Diagram





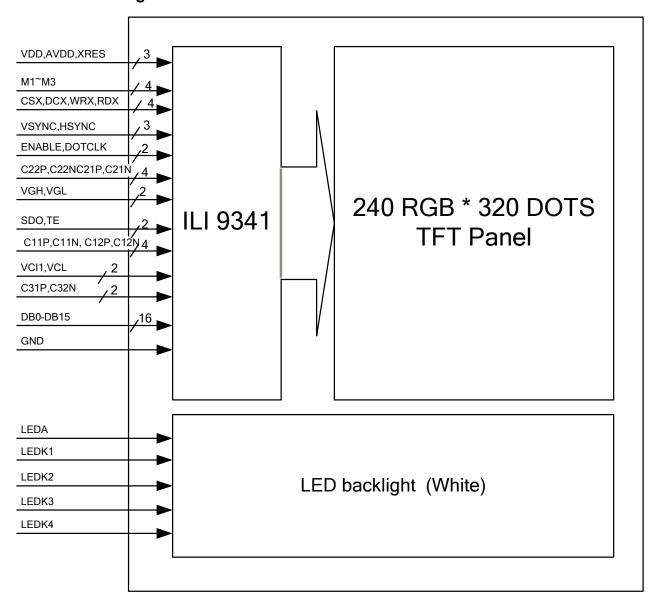
2. MODULE STRUCTURE

2.1 Counter Drawing

2.1.1 LCM Mechanical Diagram

* See Appendix

2.1.2 Block Diagram





2.2 Interface Pin Description

Pin No.	Symbol	Function
1	GND	System Ground.(0V)
2	GND	System Ground.(0V)
3	LEDK4	Power supply for LED Backlight Cathode input.
4	LEDK3	Power supply for LED Backlight Cathode input.
5	LEDK2	Power supply for LED Backlight Cathode input.
6	LEDK1	Power supply for LED Backlight Cathode input.
7	LEDA	Power supply for LED Backlight Anode input.
8	C22P	Place a 1uF/25V capacitor between C22P and C22N.
9	C22N	Place a 1uF/25V capacitor between C22N and C22P.
10	C21P	Place a 1uF/10V capacitor between C21P and C21N.
11	C21N	Place a 1uF/10V capacitor between C21N and C21P.
12	VGH	VGH pad. Place a 1uF/25V capacitor to GND.
13	VGL	VGL pad. Place a 1uF/25V capacitor to GND.
14	AVDD	AVDD pad. Place a 1uF/10V capacitor to GND.
15	C12P	Place a 1uF/10V capacitor between C12P and C12N.
16	C12N	Place a 1uF/10V capacitor between C12N and C12P.
17	C11P	Place a 1uF/10V capacitor between C11P and C11N.
18	C11N	Place a 1uF/10V capacitor between C11N and C11P.
19	GND	System Ground.(0V)
20	GND	System Ground.(0V)
21	GND	System Ground.(0V)
22	IM3	MPU Parallel interface bus and serial interface select
23	IM2	If use RGB Interface must select serial interface. * : Fix this pin at VDDI or VSS.



Pin No.	Symbol	Function
24	IM1	MPU Parallel interface bus and serial interface select
25	IMO	If use RGB Interface must select serial interface. * : Fix this pin at VDDI or VSS.
26	RESX	This signal will reset the device and must be applied to properly initialize the chip. Signal is active low.
27	CSX	Chip select input pin ("Low" enable).
28	D/CX (SCL)	This pin is used to select "Data or Command" in the parallel interface or 4-wire 8-bit serial data interface. When DCX = '1', data is selected. When DCX = '0', command is selected. This pin is used serial interface clock in 3-wire 9-bit / 4-wire 8-bit serial data interface. If not used, this pin should be connected to VDDI or VSS.
29	WRX (D/CX)	 - 8080- I /8080- II system (WRX): Serves as a write signal and writes data at the rising edge. - 4-line system (D/CX): Serves as command or parameter select. Fix to VDDI level when not in use.
30	RDX	8080- I /8080- II system (RDX): Serves as a read signal and MCU read data at the rising edge. Fix to VDDI level when not in use.
31	VSYNC	Frame synchronizing signal for RGB interface operation. Fix to VDDI or VSS level when not in use.
32	HSYNC	Line synchronizing signal for RGB interface operation. Fix to VDDI or VSS level when not in use
33	ENABLE	Data enable signal for RGB interface operation. Fix to VDDI or VSS level when not in use
34	DOTCLK	Dot clock signal for RGB interface operation. Fix to VDDI or VSS level when not in use
35	SDA	The data is applied on the rising edge of the SCL signal. If not used, fix this pin at VDDI or VSS.
36	DB0	Bi-directional data bus.
37	DB1	Bi-directional data bus.
38	DB2	Bi-directional data bus.
39	DB3	Bi-directional data bus.



Pin No.	Symbol	Function
40	DB4	Bi-directional data bus.
41	DB5	Bi-directional data bus.
42	DB6	Bi-directional data bus.
43	DB7	Bi-directional data bus.
44	DB8	Bi-directional data bus.
45	DB9	Bi-directional data bus.
46	DB10	Bi-directional data bus.
47	DB11	Bi-directional data bus.
48	DB12	Bi-directional data bus.
49	DB13	Bi-directional data bus.
50	DB14	Bi-directional data bus.
51	DB15	Bi-directional data bus.
52	DB16	Bi-directional data bus.
53	DB17	Bi-directional data bus.
54	TE	Tearing effect output pin to synchronize MPU to frame writing, activated by S/W command. When this pin is not activated, this pin is low. If not used, open this pin.
55	VDD	Power supply.(2.8V) .
56	VDD	Power supply.(2.8V) .
57	VDD	Power supply.(2.8V) .
58	VCI1	VCI1 pad. Place a 1uF/10V capacitor to GND.
59	VCL	VCL pad. Place a 1uF/10V capacitor to GND.
60	GND	System Ground.(0V)
61	GND	System Ground.(0V)



_								
	IM3	IM2	IM1	IM0	Interface	Register/Content	GRAM	
	0	1	0	1	3-wire 9-bit data serial I	SDA:	In/OUT	
	0	1	1	0	4-wire 8-bit data serial I	SDA:	In/OUT	
	1	1	0	1	3-wire 9-bit data serial II	SDA: In	/ SDO: Out	
	1	1	1	0	4-wire 8-bit data serial II	SDA: In / SDO: Out		
	0	0	0	0	8080 MCU 8-bit Parallel I	D[7:0] D[7:0]		
	0	0	0	1	8080 MCU 16-bit Parallel I	D[7:0] D[15:0]		
	0	0	1	0	8080 MCU 9-bit Parallel I	D[7:0] D[8:0]		
	0	0	1	1	8080 MCU 18-bit Parallel I	D[7:0]	D[17:0]	
	1	0	0	0	8080 MCU 16-bit Parallel II	D[8:1]	D[17:10] D[8:1]	
	1	0	0	1	8080 MCU 8-bit Parallel II	D[17:10]	D[17:10]	
	1	0	1	0	8080 MCU 18-bit Parallel II	D[8:11]	D[17:0]	
1	1	0	1	1	8080 MCU 9-bit Parallel II	D[17:10]	D[17:9]	
1								



2.2.1 Application Notes:

TBD

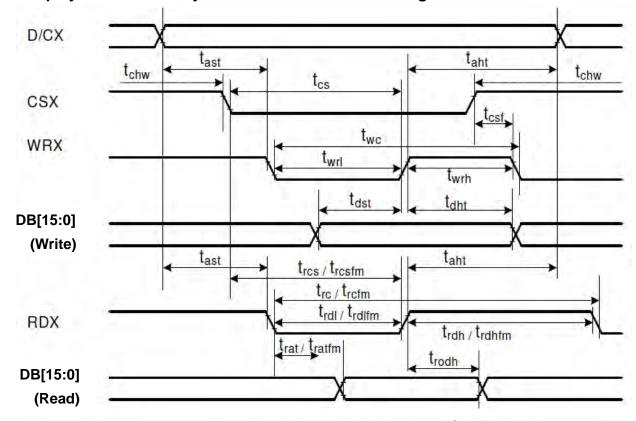
2.2.2 Refer Initial code:

TBD



2.3 Timing Characteristics

Display Parallel 8080 system 16/8-bit Interface Timing Characteristics

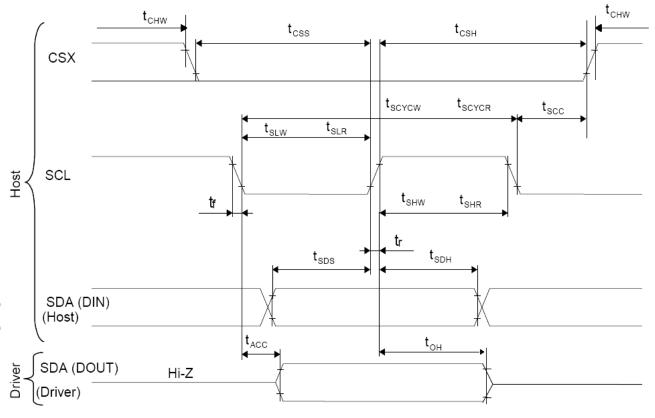


Signal	Symbol	Parameter	min	max	Unit	Description
DCV	tast	Address setup time	0	*	ns	
DCX	taht	Address hold time (Write/Read)	0	-	ns	
	tchw	CSX "H" pulse width	0		ns	
CSX	tcs	Chip Select setup time (Write)	15	3.4	ns	
	trcs	Chip Select setup time (Read ID)	45	- 2	ns);
	trcsfm	Chip Select setup time (Read FM)	355		ns	
	tcsf	Chip Select Wait time (Write/Read)	10		ns	
DCX	twc	Write cycle	66		ns	
	twrh	Write Control pulse H duration	15	380	ns	
	twrl	Write Control pulse L duration	15	-	ns	
WRX RDX (FM)	trcfm	Read Cycle (FM)	450	- 2	ns	
	trdhfm	Read Control H duration (FM)	90		ns	
	trdlfm	Read Control L duration (FM)	355	-	ns	
	trc	Read cycle (ID)	160		ns	
RDX (ID)	trdh	Read Control pulse H duration	90	1	ns	
	trdl	Read Control pulse L duration	45		ns	
RDX (ID)	tdst	Write data setup time	10		ns	
	tdht	Write data hold time	10	154	ns	For maximum CL 20nE
	trat	Read access time	-	40	ns	For maximum CL=30pF For minimum CL=8pF
	tratfm	Read access time		340	ns	I of minimum GL=opF
	trod	Read output disable time	20	80	ns	

Note: Ta = -30 to 70 °C, VCC=1.65V to 3.3V, VCI=2.5V to 3.3V, GND=0V

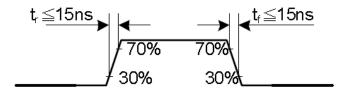


Display Serial Interface Timing Characteristics (3-line SPI system)



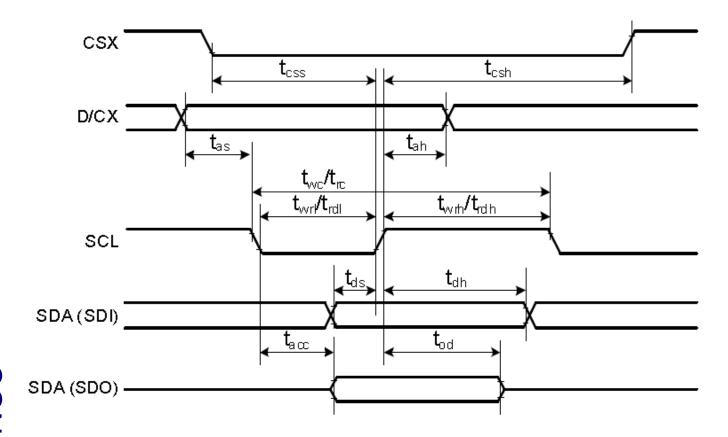
Signal	Symbol	Parameter	min	max	Unit	Description
	tscycw	Serial Clock Cycle (Write)	100	-	ns	
	tshw	SCL "H" Pulse Width (Write)	40	-	ns	
SCL	tslw	SCL "L" Pulse Width (Write)	40	-	ns	
SCL SCL	tscycr	Serial Clock Cycle (Read)	150	-	ns	
	tshr	SCL "H" Pulse Width (Read)	60	-	ns	
	tsir	SCL "L" Pulse Width (Read)	60	-	ns	
SDA / SDI	tsds	Data setup time (Write)	30	-	ns	
(Input)	tsdh	Data hold time (Write)	30	_	ns	
SDA / SDO	tacc	Access time (Read)	10	-	ns	
(Output)	toh	Output disable time (Read)	10	50	ns	
	tscc	SCL-CSX	20	-	ns	
Cev	tchw	CSX "H" Pulse Width	40	-	ns	
CSX	tcss	CSX-SCL Time	60	-	ns	
	tcsh	CSA-SCL TIME	65	-	ns	

Note: Ta = 25 °C, VDDI=1.65V to 3.3V, VCI=2.5V to 3.3V, AGND=VSS=0V



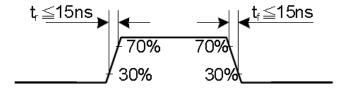
Display Serial Interface Timing Characteristics (4-line SPI system)





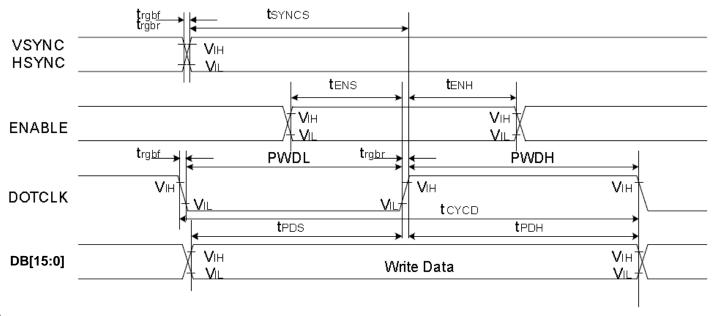
Signal	Symbol	Parameter	min	max	Unit	Description
csx	tcss	Chip select time (Write)	40	_	ns	
CSA	tcsh	Chip select hold time (Read)	40	-	ns	
	twc	Serial clock cycle (Write)	100	-	ns	
	twrh	SCL "H" pulse width (Write)	40	-	ns	
SCL	twrl	SCL "L" pulse width (Write)	40	-	ns	
SCL	trc	Serial clock cycle (Read)	150	-	ns	
	trdh	SCL "H" pulse width (Read)	60	-	ns	
	trdl	SCL "L" pulse width (Read)	60	-	ns	
D/CX	tas	D/CX setup time	10	-		
D/CX	tah	D/CX hold time (Write / Read)	10	-		
SDA / SDI	tds	Data setup time (Write)	30	-	ns	
(Input)	tdh	Data hold time (Write)	30	-	ns	
SDA / SDO	tacc	Access time (Read)	10	-	ns	For maximum CL=30pF
(Output)	tod	Output disable time (Read)	10	50	ns	For minimum CL=8pF

Note: Ta = 25 °C, VDDI=1.65V to 3.3V, VCI=2.5V to 3.3V, AGND=VSS=0V



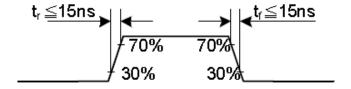


Parallel 16-bit RGB Interface Timing Characteristics



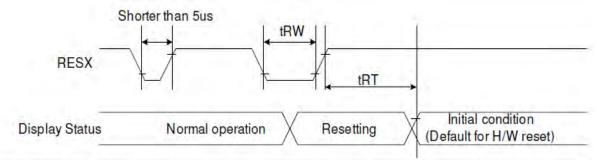
Signal	Symbol	Parameter	min	max	Unit	Description
VSYNC/	tsyncs VSYNC/HSYNC setup time tsynch VSYNC/HSYNC hold time tens DE setup time tenh DE hold time tpos Data setup time tpoh DOTCLK high-level period PWDL DOTCLK low-level period tcyco DOTCLK cycle time tsyncs VSYNC/HSYNC setup time tsynch VSYNC/HSYNC setup time tsynch VSYNC/HSYNC hold time tens DE setup time tens DE setup time tpos Data setup time tpos Data setup time tpoh DOTCLK high-level pulse period	VSYNC/HSYNC setup time	15	-	ns	
HSYNC	tsynch	VSYNC/HSYNC hold time	15	-	ns	
n=	t _{ENS}	DE setup time	15	-	ns	
DE	tenh	DE hold time	15	-	ns	
VSYNC / HSYNC DE DB[15:0] DOTCLK VSYNC / HSYNC DE DB[15:0]	t _{POS}	Data setup time	15	-	ns	18/16-bit bus RGB
DB[13.0]	tрон	Data hold time	15	-	ns	interface mode
	PWDH	DOTCLK high-level period	15	-	ns	
VSYNC / HSYNC DE DB[15:0] DOTCLK VSYNC / HSYNC DE	PWDL	DOTCLK low-level period	15	-	ns	
	toyoo	DOTCLK cycle time	100	-	ns	
	trgbr , trgbf	DOTCLK,HSYNC,VSYNC rise/fall time	-	15	ns	
VSYNC/	tsyncs	VSYNC/HSYNC setup time	15	-	ns	
HSYNC	tsynch	VSYNC/HSYNC hold time	15	-	ns	
DE	tens	DE setup time	15	-	ns	
DE	t _{ENH}	DE hold time	15	-	ns	
DR[15:0]	tros	Data setup time	15	-	ns	6-bit bus RGB
JB[13.0]	t _{PDH}	Data hold time	15	-	ns	interface mode
	PWDH	DOTCLK high-level pulse period	15	-	ns	
DOTCLK	PWDL	DOTCLK low-level pulse period	15	-	ns	
DOTCER	toyoo	DOTCLK cycle time	100	-	ns	
	t _{rgbr} , t _{rgbf}	DOTCLK,HSYNC,VSYNC rise/fall time	-	15	ns	

Note: Ta = -30 to 70 °C, VDDI=1.65V to 3.3V, VCI=2.5V to 3.3V, AGND=VSS=0V





Reset Timing



Signal	Symbol	Parameter	Min	Max	Unit
RESX	tRW	Reset pulse duration			uS
	+DT	Decet concel		5 (note 1,5)	mS
	tRT	Reset cancel		120 (note 1,6,7)	mS

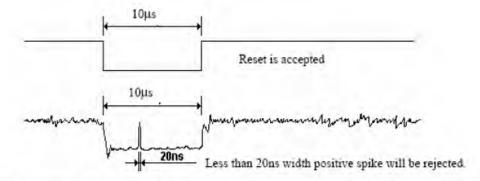
Note 1: The reset cancel includes also required time for loading ID bytes, VCOM setting and other settings from NV memory to registers. This loading is done every time when there is HW reset cancel time (tRT) within 5 ms after a rising edge of RESX.

Note 2: Spike due to an electrostatic discharge on RESX line does not cause irregular system reset according to the table below: -

RESX Pulse	Action
Shorter than 5us	Reset Rejected
Longer than 10us	Reset
Between 5us and 10us	Reset starts

Note 3: During the Resetting period, the display will be blanked (The display is entering blanking sequence, which maximum time is 120 ms, when Reset Starts in Sleep Out –mode. The display remains the blank state in Sleep In -mode.) And then return to Default condition for Hardware Reset.

Note 4: Spike Rejection also applies during a valid reset pulse as shown below:

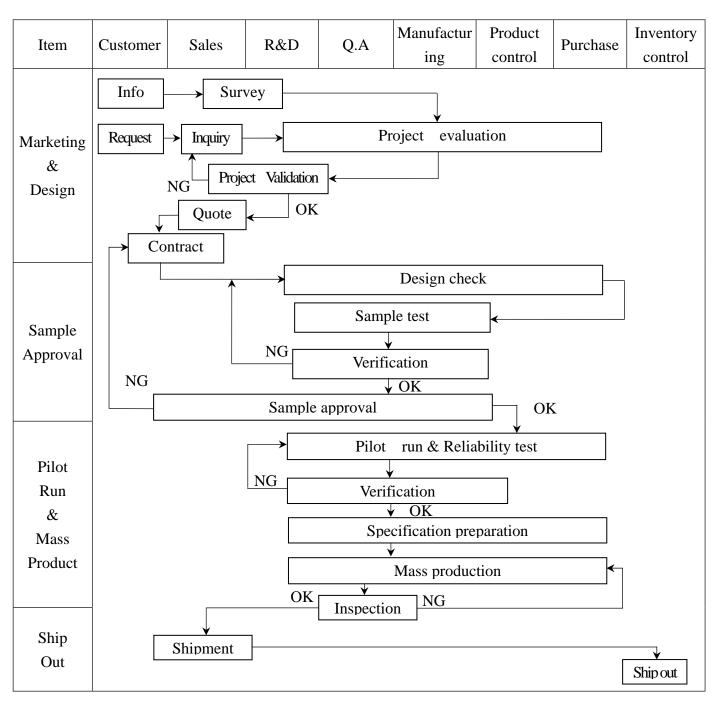


- Note 5: When Reset applied during Sleep In Mode.
- Note 6: When Reset applied during Sleep Out Mode.
- Note 7: It is necessary to wait 5msec after releasing RESX before sending commands. Also Sleep Out command cannot be sent for 120msec.

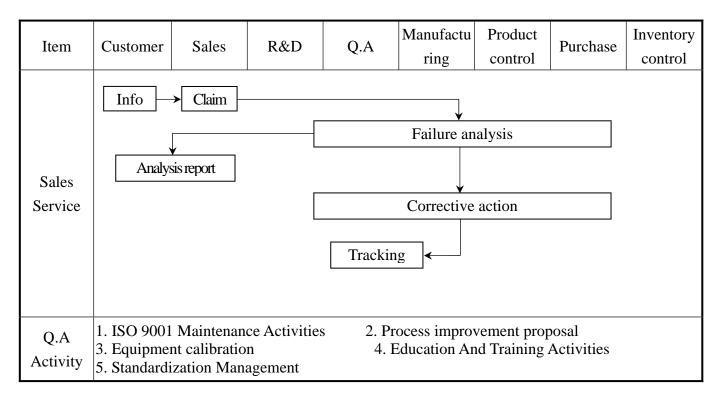


3. QUALITY ASSURANCE SYSTEM

3.1 Quality Assurance Flow Chart



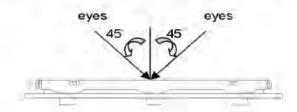




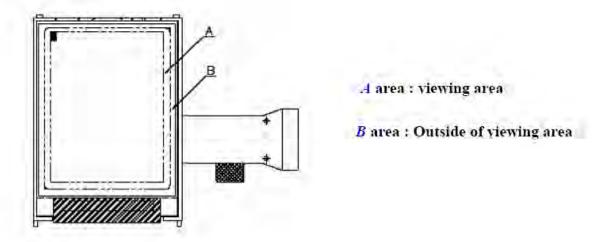


3.2. Inspection Specification

- ◆Scope : The document shall be applied to TFT-LCD Module for less than 3, 5" (Ver.B01).
- ◆Inspection Standard: MIL-STD-105E Table Normal Inspection Single Sampling Level Ⅱ.
- ◆Equipment : Gauge · MIL-STD · Powertip Tester · Sample
- ◆Defect Level: Major Defect AQL: 0.4 : Minor Defect AQL: 1,5
- OUT Going Defect Level : Sampling.
- Standard of the product appearance test:
 - a. Manner of appearance test:
 - (1). The test best be under 20W×2 fluorescent light, and distance of view must be at 30 cm.
 - (2). The test direction is base on about around 45° of vertical line.



(3). Definition of area.



(4). Standard of inspection: (Unit: mm)



◆Specification For TFT-LCD Module Less Than 3.5":

◆Spe	ecification For TFT-LC	D Module Less	Than 3.5":		(Ver.B01)		
NO	Item		Criter	ion	Level		
		1. 1The part number is inconsistent with work order of production.					
01	Product condition Quantity Outline dimension	1, 2 Mixed proc	luct types.		Major		
		1. 3 Assembled	in inverse direction	ı .	Major		
02	Quantity	2. 1The quantit	The part number is inconsistent with work order of production. Mixed product types. Assembled in inverse direction. The quantity is inconsistent with work order of production. Product dimension and structure must conform to structur diagram. Missing line character and icon. No function or no display. Display malfunction. LCD viewing angle defect. Current consumption exceeds product specifications. Item Acceptance (Q'ty) Bright Dot ≤ 2 Dot Dark Dot ≤ 3 Doffect Joint Dot ≤ 2 Total ≤ 3				
03	Outline dimension		Assembled in inverse direction. The quantity is inconsistent with work order of production. Product dimension and structure must conform to structure diagram. Missing line character and icon. No function or no display. Display malfunction. LCD viewing angle defect. Current consumption exceeds product specifications.				
		4. 1 Missing lin	e character and ico	n.	Major		
	Electrical Testing	4, 2 No function or no display.					
04		4. 3 Display malfunction.					
		4. 4 LCD viewing angle defect.					
		4. 5 Current co	nsumption exceeds	ion. gle defect. otion exceeds product specifications.	Major		
			Item	Acceptance (Q'ty)			
	Dot defect		Bright Dot	≦ 2			
	Dot defect	Dot	Dark Dot	≦ 3			
05	(Bright dot \	Defect	Joint Dot	≦ 2	1.5		
บอ	Dark dot)		Total	≦ 3	Minor		
	On -display	5. 1 Inspection pattern: full white, full black, Red, Green and					
				fect area $>1/2$ dot.			



◆Specification For TFT-LCD Module Less Than 3.5":

Specif	fication For TFT-LCI	Module Less T	han 3.5":				(Ver.B0		
NO	Item		Crite	erion			Level		
	Black or white dot \ scratch \ contamination Round type	Di (dia	6. 1 Round type (Non-display or d Dimension (diameter : Φ) $\Phi \le 0.15$ $0.15 < \Phi \le 0.20$ $0.20 < \Phi \le 0.30$ $\Phi > 0.30$		Acceptance A area Ignore 2 2	(Q'ty) B area Ignore			
06	Y		Total		3		Minor		
	$\Phi = (x+y)/2$	6. 2 Line type(Non-display or d	displa	ıy) :				
	Line type	I	Dimension		Acceptai	ace (Q'ty)			
	→ L W	Length (L)	Width (W)		A area	B area			
			$\mathbf{W} \leq 0$.03	Ignore				
		→ L +-	→ L +	→ L I←	L ≦5.0	$0.03 < W \le 0.05$		3	
			W >0.05		As round type	Ignore			
			Total		3				
		Dim	ension		Acceptance	(Q'ty)			
		(diam	neter : Φ)	A	A area	B area			
	Polarizer		$\Phi \leq 0.20$	Ignore					
07	Bubble	0.20 <	$0.20 < \Phi \leq 0.50$		3	Ignore	Mino		
			$\Phi > 0.50$		0	ignore			
		Т	otal		3				



◆Specification For TFT-LCD Module Less Than 3, 5":

NO	Item		Criterion		Level
		Z: The th	ickness of crack	Y : The width of crack. W : terminal length a : LCD side length	
			l glass chip: p on panel surface and cra	ack between panels:	
			X Z	Z Y	
08	The crack of glass	SP-	Y [OK]	SP [NG]	Mino
			Seal width Z	Y	
		X	Y	z	
		≦ a	Crack can't enter viewing area	≦1/2 t	
		≦ a	Crack can't exceed the half of SP width.	1/2 t < Z ≤2 t	



NO	Item	Criterion		Leve	
	The crack of glass	X: The length of crack Z: The thickness of crack t: The thickness of glass 8, 1, 2 Corner crack:			nal length ide length
		X ≤1/5 a ≤1/5 a	Crack can't enviewing area Crack can't excee half of SP widt	ed the	
08			sion over termina p on electrode pa		Mine
			_	X	
		Front	X ≤ a	Y ≤ 1/2 W	Z ≤ t



◆Specification For TFT-LCD Module Less Than 3.5″:

Criterion		
Z : The thic	Item The crack of	NO
kness of cra kness of glas	X: The length of crack Z: The thickness of cra t: The thickness of glas 8. 2. 2 Non-conductive	Symbols : X: The length of crack Z: The thickness of cra t: The thickness of glas 8. 2. 2 Non-conductive
eng hic	X : The l Z : The t t : The t	Symbols : X: The l Z: The t t: The t 8. 2. 2 No



◆Specification For TFT-LCD Module Less Than 3.5":

Spec	ecification For TFT-LCD Module Less Than 3, 5":		
NO	Item	Criterion	Level
	Backlight elements	9, 1 Backlight can't work normally.	Major
09		9, 2 Backlight doesn't light or color is wrong.	
		9, 3 Illumination source flickers when lit.	Major
10	General appearance	10. 1 Pin type \quantity \quantity \dimension must match type in structure diagram.	Major
		10, 2 No short circuits in components on PCB or FPC .	Major
		10. 3 Parts on PCB or FPC must be the same as on the production characteristic chart .There should be no wrong parts , missing parts or excess parts.	Majoi
		10. 4 Product packaging must the same as specified on packaging specification sheet.	Minor
		10, 5 The folding and peeled off in polarizer are not acceptable.	Minoi
		10. 6 The PCB or FPC between B/L assembled distance(PCB or FPC) is ≤1.5 mm.	Minor



4. RELIABILITY TEST

4.1 Reliability Test Condition

NO.	TEST ITEM	TEST CONDITION			
1	High Temperature Storage Test	Keep in +80 ±2°C 96 hrs Surrounding temperature, then storage at normal condition 4hrs.			
2	Low Temperature Storage Test	Keep in -30 ±2°C 96 hrs Surrounding temperature, then storage at normal condition 4hrs.			
3	High Temperature / High Humidity Storage Test	Keep in +60°C /90% R.H duration for 96 hrs Surrounding temperature, then storage at normal condition 4hrs. (Excluding the polarizer)			
4		Air Discharge: Apply 2 KV with 5 times Discharge for each polarity +/- 1. Temperature ambian	Contact Discharge: Apply 250V with 5 times discharge for each polarity +/-		
	ESD Test	 Temperature ambiance:15°C ~35°C Humidity relative:30% ~60% Energy Storage Capacitance(Cs+Cd):150pF±10% Discharge Resistance(Rd):330 Ω±10% Discharge, mode of operation: Single Discharge (time between successive discharges at least 1 s) (Tolerance if the output voltage indication: ±5%) 			
5	Temperature Cycling Storage Test	$-30^{\circ}\text{C} \rightarrow +25^{\circ}\text{C} \rightarrow +80^{\circ}\text{C} \rightarrow +25^{\circ}\text{C}$ $(30\text{mins}) (5\text{mins}) (5\text{mins})$ 10 Cycle Surrounding temperature, then storage at normal condition 4hrs.			
6	Vibration Test (Packaged)	 Sine wave 10~55 Hz frequency (1 min) The amplitude of vibration :1.5 mm Each direction (X \ Y \ Z) duration for 2 Hrs 			
7	Drop Test (Packaged)	Packing Weight (Kg) 0 ~ 45.4	Drop Height (cm)		
		45.4 ~ 90.8	76		
7		90.8 ~ 454	61		
		0ver 454	46		
		Drop direction: * 1 corner / 3 edges / 6 sides each 1 times			



5. PRECAUTION RELATING PRODUCT HANDLING

5.1 SAFETY

- 5.1.1 If the LCD panel breaks, be careful not to get the liquid crystal to touch your skin.
- 5.1.2 If the liquid crystal touches your skin or clothes, please wash it off immediately by using soap and water.

5.2 HANDLING

- 5.2.1 Avoid any strong mechanical shock which can break the glass.
- 5.2.2 Avoid static electricity which can damage the CMOS LSI—When working with the module, be sure to ground your body and any electrical equipment you may be using.
- 5.2.3 Do not remove the panel or frame from the module.
- 5.2.4 The polarizing plate of the display is very fragile. So , please handle it very carefully ,do not touch , push or rub the exposed polarizing with anything harder than an HB pencil lead (glass , tweezers , etc.)
- 5.2.5 Do not wipe the polarizing plate with a dry cloth, as it may easily scratch the surface of plate.
- 5.2.6 Do not touch the display area with bare hands, this will stain the display area.
- 5.2.7 Do not use ketonics solvent & aromatic solvent. Use with a soft cloth soaked with a cleaning naphtha solvent.
- 5.2.8 To control temperature and time of soldering is 320±10°C and 3-5 sec.
- 5.2.9 To avoid liquid (include organic solvent) stained on LCM.

5.3 STORAGE

- 5.3.1 Store the panel or module in a dark place where the temperature is 25° C $\pm 5^{\circ}$ C and the humidity is below 65% RH.
- 5.3.2 Do not place the module near organics solvents or corrosive gases.
- 5.3.3 Do not crush, shake, or jolt the module.

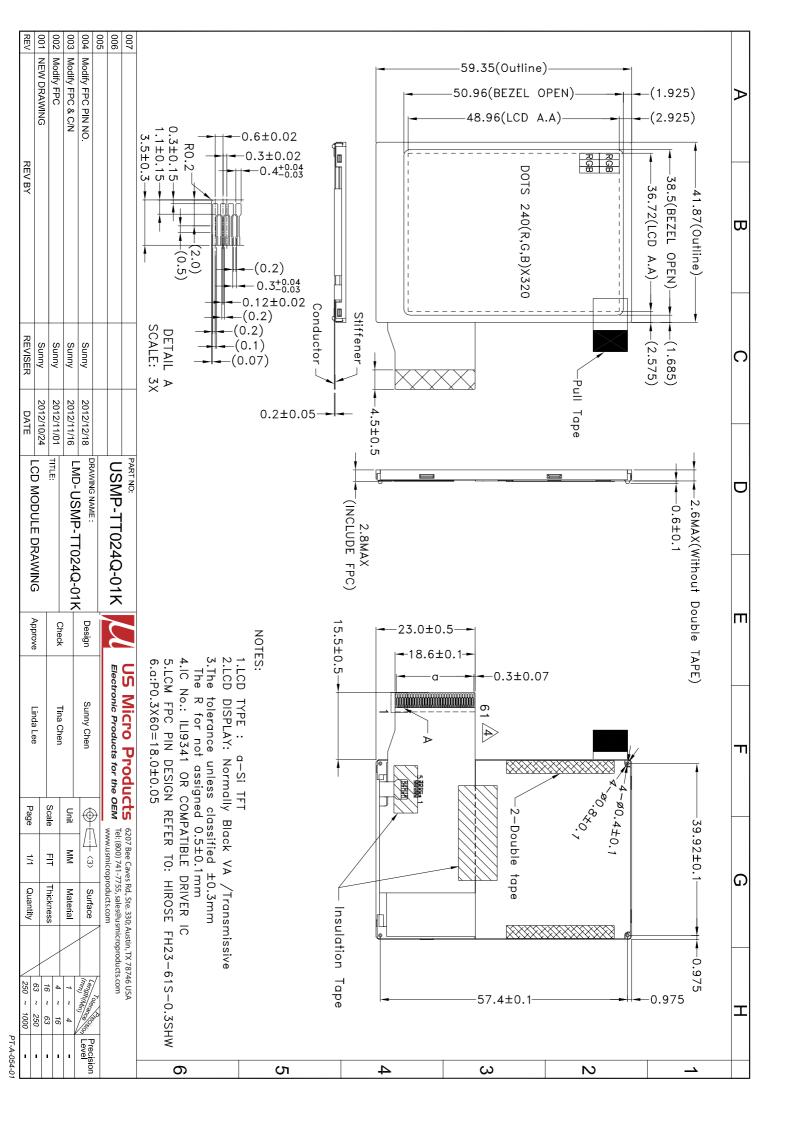
5.4 TERMS OF WARRANTY

5.4.1 Applicable warrant period

The period is within Twenty-four months since the date of shipping out under normal using and storage conditions.

5.4.2 Unaccepted responsibility

This product has been manufactured to your company's specification as a part for use in your company's general electronic products. It is guaranteed to perform according to delivery specifications. For any other use apart from general electronic equipment, we cannot take responsibility if the product is used in nuclear power control equipment, aerospace equipment, fire and security systems or any other applications in which there is a direct risk to human life and where extremely high levels of reliability are required.



Displays

US Micro Products is an industrial distributor specializing in engineered display solutions. We dedicate ourselves to providing the best in displays for the medical, industrial, gaming, automotive, aerospace, military and consumer markets.

OLEDs



Passive LCDs



TFT Display



Multitouch



Open Frame Monitors



Touch Screen



As our customer, you receive expert knowledge, support and service. Our technical sales staff and experienced design engineers provide answers to your questions and engineered solutions to meet your display needs.

Peripheral Devices

Our full line of peripheral devices includes keyboards, trackballs and printers. These rugged industrial products are designed to meet the rigorous demands of your equipment and are available in a variety of standard and custom options.

Keyboards



Trackballs



Aerospace Trackballs



Printers



