

# PMOLED SPECIFICATION

Part Number	USMP-P22403
Size	1.6"
Resolution	128 x 64
Color	White
IC	SSD1325
Brightness	80 cd/m <sup>2</sup>
Contrast	2000:1
Operating temp.	-40 ~ 70°C

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## REVISION RECORD

REV.	REVISION DESCRIPTION	REV. DATE	REMARK
X01	■ INITIAL RELEASE	2012. 08. 09	
X02	■ Modify driving voltage ■ Modify luminance specifications ■ Modify application circuit	2012. 09. 14	Page 6, 7, 8 & 15
X03	■ Modify driving voltage (15.5→14.5V) ■ Modify panel electrical specifications	2012. 11. 20	Page 6, 7 & 8
A01	■ Transfer from X version	2012. 11. 21	

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## **1. SCOPE**

## **2. WARRANTY**

USMP warrants that the products delivered pursuant to this specification (or order) will conform to the agreed specifications for twelve (12) months from the shipping date ("Warranty Period"). USMP is obligated to repair or replace the products which are found to be defective or inconsistent with the specifications during the Warranty Period without charge, on condition that the products are stored or used as the conditions specified in the specifications. Nevertheless, USMP is not obligated to repair or replace the products without charge if the defects or inconsistency are caused by the force majeure or the reckless behaviors of the customer.

After the Warranty Period, all repairs or replacements of the products are subject to charge.

## **3. FEATURES**

- Small molecular organic light emitting diode
- Color : White
- Panel matrix : 128\*64
- Driver IC : SSD1325
- Excellent quick response time.
- Extremely thin thickness for best mechanism design : 1.61mm
- High contrast : 2000:1
- Wide viewing angle : 160°
- Serial Peripheral Interface.
- Wide range of operating temperature : -40 to 70 °C
- Anti-glare polarizer.

#### **4. MECHANICAL DATA**

NO	ITEM	SPECIFICATION	UNIT
1	Dot Matrix	128 (W) x 64 (H)	dot
2	Dot Size	0.255 (W) x 0.255 (H)	mm <sup>2</sup>
3	Dot Pitch	0.285 (W) x 0.285 (H)	mm <sup>2</sup>
4	Aperture Rate	80	%
5	Active Area	36.45 (W) x 18.21 (H)	mm <sup>2</sup>
6	Panel Size	41.9 (W) x 25.3 (H)	mm <sup>2</sup>
7*	Panel Thickness	1.42 ± 0.1	mm
8	Module Size	41.9 (W) x 65.751 (H) x 2.41 (D)	mm <sup>3</sup>
9	Diagonal A/A size	1.6	inch
10	Module Weight	3.88 ± 10%	gram

\* Panel thickness includes substrate glass, cover glass and UV glue thickness.

## 5. MAXIMUM RATINGS

ITEM	MIN	MAX	UNIT	Condition	Remark
Supply Voltage ( $V_{DD}$ )	-0.3	3.5	V	$T_a = 25^\circ\text{C}$	IC maximum rating
Supply Voltage ( $V_{CC}$ )	8	16	V	$T_a = 25^\circ\text{C}$	IC maximum rating
Operating Temp.	-40	70	$^\circ\text{C}$		
Storage Temp	-40	85	$^\circ\text{C}$		
Humidity	-	85	%		
Life Time	30,000	-	Hrs	80 cd/m <sup>2</sup> , 50% checkerboard	Note (1)
Life Time	40,000	-	Hrs	60 cd/m <sup>2</sup> , 50% checkerboard	Note (2)

Note:

(A) Under  $V_{CC} = 14.5\text{V}$ ,  $T_a = 25^\circ\text{C}$ , 50% RH.

(B) Life time is defined the amount of time when the luminance has decayed to less than 50% of the initial measured luminance.

(1) Setting of 80cd/m<sup>2</sup> :

- Contrast setting : 0x3a
- Frame rate : 105Hz
- Duty setting : 1/64

(2) Setting of 60 cd/m<sup>2</sup> :

- Contrast setting : 0x2d
- Frame rate : 105Hz
- Duty setting : 1/64

## 6. ELECTRICAL CHARACTERISTICS

### 6.1 D.C ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETERS	TEST CONDITION	MIN	TYP	MAX	UNIT
$V_{CC}$	Analog power supply (for OLED panel)	$T_a = -20\text{ }^{\circ}\text{C}$ to $+70\text{ }^{\circ}\text{C}$	14	14.5	15	V
$V_{DD}$	Digital power supply	$T_a = -20\text{ }^{\circ}\text{C}$ to $+70\text{ }^{\circ}\text{C}$	2.4	2.7	3.5	V
$I_{DD}$	Operating current for $V_{DD}$ $V_{DD} = 2.7\text{V}$ , $V_{CC} = 12\text{V}$ , $I_{REF} = 10\text{uA}$ No panel attached, All Display ON	Contrast=7F	-	-	650	$\text{uA}$
$I_{CC}$	Operating current for $V_{CC}$ $V_{DD} = 2.7\text{V}$ , $V_{CC} = 12\text{V}$ , $I_{REF} = 10\text{uA}$ No panel attached, All Display ON	Contrast=7F	-	700	-	$\text{uA}$
$V_{IH}$	Hi logic input level		$0.8^* V_{DD}$	-	$V_{DD}$	V
$V_{IL}$	Low logic input level		0	-	$0.2^* V_{DD}$	V
$V_{OH}$	Hi logic output level		$0.9^* V_{DD}$	-	$V_{DD}$	V
$V_{OL}$	Low logic output level		0	-	$0.1^* V_{DD}$	V
$I_{SEG}$	Segment on output current $V_{DD}=2.7\text{V}$ , $V_{CC}=12\text{V}$ , $I_{REF}=10\text{uA}$ , Display on, Segment pin under test is connected with a 20K resistive load to $V_{SS}$	Contrast=7F	270	300	370	$\text{uA}$
		Contrast=5F	-	225	-	$\text{uA}$
		Contrast=3F	-	150	-	$\text{uA}$
		Contrast=1F	-	75	-	$\text{uA}$

## 6.2 ELECTRO-OPTICAL CHARATERISTICS

### PANEL ELECTRICAL SPECIFICATIONS

PARAMETER	MIN	TYP.	MAX	UNITS	COMMENTS
Normal mode current		26	28	mA	All pixels on (1)
Standby mode current		2	3	mA	Standby mode 10% pixels on (2)
Normal mode power consumption		377	406	mW	All pixels on (1)
Standby mode power consumption		29	43.5	mW	Standby mode 10% pixels on (2)
Normal Luminance	60	80		cd/m <sup>2</sup>	Display Average
Standby Luminance		10		cd/m <sup>2</sup>	Display Average
CIE <sub>x</sub> (White)	0.27	0.31	0.35		x, y (CIE 1931)
CIE <sub>y</sub> (White)	0.31	0.35	0.39		
Dark Room Contrast	2000:1				
Viewing Angle	160			degree	
Response Time		10		μs	

(1) Normal mode condition :

- Driving Voltage : 14.5V
- Contrast setting : 0x3a
- Frame rate : 105Hz
- Duty setting : 1/64

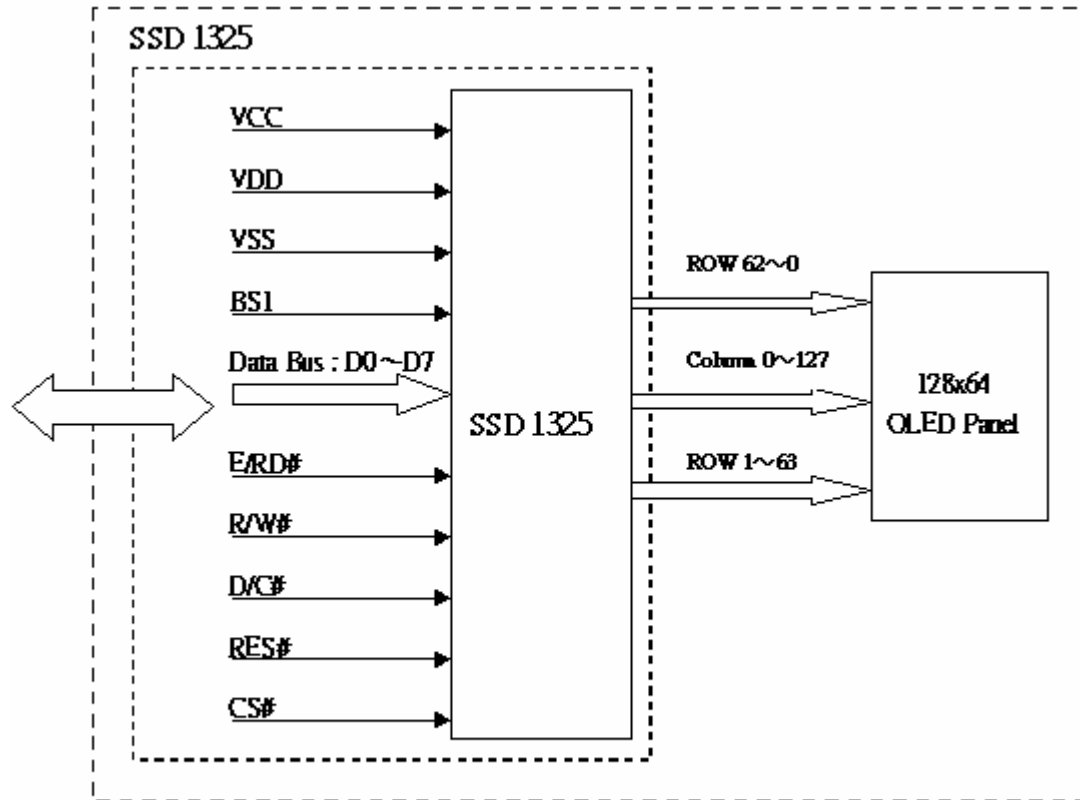
(2) Standby mode condition :

- Driving Voltage : 14.5V
- Contrast setting : 0x0a
- Frame rate : 105Hz
- Duty setting : 1/64

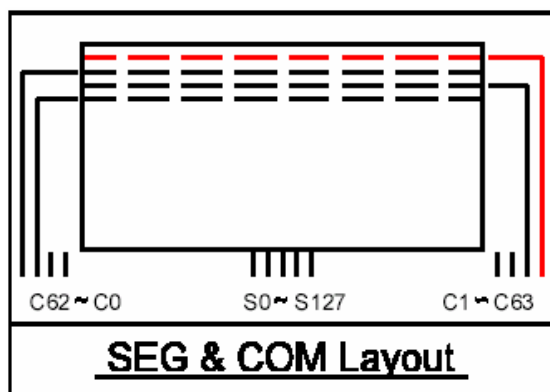


## 7. INTERFACE

### 7.1 FUNCTION BLOCK DIAGRAM



### 7.2 PANEL LAYOUT DIAGRAM

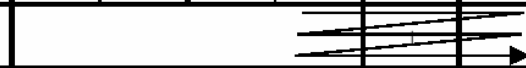


### 7.3 PIN ASSIGNMENTS

Pin No.	Pin Name	Description
1	VSS	This is a ground pin.
2	VCC	Positive OLED high voltage power supply
3	VDD	Voltage power supply for logic
4	NC	No connection.
5	D7	8-bit data bus
6	D6	8-bit data bus
7	D5	8-bit data bus
8	D4	8-bit data bus
9	D3	8-bit data bus
10	D2	8-bit data bus
11	D1	8-bit data bus
12	D0	8-bit data bus
13	E(RD#)	Read strobe signal and reads data at the low level
14	R/W#	Write strobe signal and reads data at the low level
15	D/C#	Data/Command control pin. When it pulled high, the input at D0-D7 is treated as display data. When it pulled low, the input at D0-D7 is transferred to command register
16	BS1	Interface select pin
17	RES#	Hardware reset signal
18	CS#	Chip select pin. The driver IC will be selected When CS pin is active low.


## 7.4 GRAPHIC DISPLAY DATA RAM ADDRESS MAP

The GDDRAM is a bit mapped static RAM holding the bit pattern to be displayed. The size of the RAM is 128x80x4 bits. For mechanical flexibility, re-mapping on both Segment and Common outputs can be selected by software. (Refer to Table 3-7 for GDDRAM address map description)

		SEG0	SEG1	SEG2	SEG3		SEG124	SEG125	SEG126	SEG127	SEG Outputs
		00		01			3E		3F		Column Address
											(HEX)
COM0	00	D0[3:0]	D0[7:4]	D1[3:0]	D1[7:4]		D62[3:0]	D62[7:4]	D63[3:0]	D63[7:4]	
COM1	01	D64[3:0]	D64[7:4]	D65[3:0]	D65[7:4]		D126[3:0]	D126[7:4]	D127[3:0]	D127[7:4]	
											
COM78	4E	D4992[3:0]	D4992[7:4]	D4993[3:0]	D4993[7:4]		D5054[3:0]	D5054[7:4]	D5055[3:0]	D5055[7:4]	
COM79	4F	D5056[3:0]	D5056[7:4]	D5057[3:0]	D5057[7:4]		D5118[3:0]	D5118[7:4]	D5119[3:0]	D5119[7:4]	
COM Outputs	Row Address (HEX)										


(Display Startline=0)

**Table 3– GDDRAM address map showing Horizontal Address Increment A[2]=0, Column Address Re-map A[0]=0, Nibble Re-map A[1]=0, COM Re-map A[4]=0, and Display Start Line=00H (Data byte sequence: D0, D1, ... , D5118, D5119)**

		SEG0	SEG1	SEG2	SEG3		SEG124	SEG125	SEG126	SEG127	SEG Outputs
		00		01			3E		3F		Column Address
											(HEX)
COM0	00	D0[3:0]	D0[7:4]	D80[3:0]	D80[7:4]		D4960[3:0]	D4960[7:4]	D5040[3:0]	D5040[7:4]	
COM1	01	D1[3:0]	D1[7:4]	D81[3:0]	D81[7:4]		D4961[3:0]	D4961[7:4]	D5041[3:0]	D5041[7:4]	
											
COM78	4E	D78[3:0]	D78[7:4]	D158[3:0]	D158[7:4]		D5038[3:0]	D5038[7:4]	D5118[3:0]	D5118[7:4]	
COM79	4F	D79[3:0]	D79[7:4]	D159[3:0]	D159[7:4]		D5039[3:0]	D5039[7:4]	D5119[3:0]	D5119[7:4]	
COM Outputs	Row Address (HEX)										

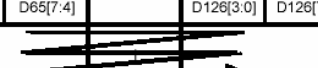
(Display Startline=0)

**Table 4–GDDRAM address map showing Horizontal Address Increment A[2]=1, Column Address Re-map A[0]=0, Nibble Re-map A[1]=0, COM Re-map A[4]=0, and Display Start Line=00H (Data byte sequence: D0, D1, ... , D5118, D5119)**

		SEG0	SEG1	SEG2	SEG3		SEG124	SEG125	SEG126	SEG127	SEG Outputs	
		3F		3E			01		00		Column Address	
												(HEX)
COM0	00	D63[7:4]	D63[3:0]	D62[7:4]	D62[3:0]		D1[7:4]	D1[3:0]	D0[7:4]	D0[3:0]		
COM1	01	D127[7:4]	D127[3:0]	D126[7:4]	D126[3:0]		D65[7:4]	D65[3:0]	D64[7:4]	D64[3:0]		
												
COM78	4E	D5055[7:4]	D5055[3:0]	D5054[7:4]	D5054[3:0]		D4993[7:4]	D4993[3:0]	D4992[7:4]	D4992[3:0]		
COM79	4F	D5119[7:4]	D5119[3:0]	D5118[7:4]	D5118[3:0]		D5057[7:4]	D5057[3:0]	D5056[7:4]	D5056[3:0]		
COM Outputs	Row Address (HEX)											

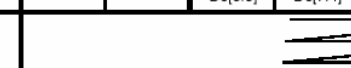
(Display Startline=0)

**Table 5—GDDRAM address map showing Horizontal Address Increment A[2]=0, Column Address Re-map A[0]=1, Nibble Re-map A[1]=1, COM Re-map A[4]=0, and Display Start Line=00H (Data byte sequence: D0, D1, ... , D5118, D5119)**

		SEG0	SEG1	SEG2	SEG3		SEG124	SEG125	SEG126	SEG127	SEG Outputs	
		00		01			3E		3F		Column Address	
												(HEX)
COM15	0F	D0[3:0]	D0[7:4]	D1[3:0]	D1[7:4]		D62[3:0]	D62[7:4]	D63[3:0]	D63[7:4]		
COM14	0E	D64[3:0]	D64[7:4]	D65[3:0]	D65[7:4]		D126[3:0]	D126[7:4]	D127[3:0]	D127[7:4]		
												
COM17	11	D4992[3:0]	D4992[7:4]	D4993[3:0]	D4993[7:4]		D5054[3:0]	D5054[7:4]	D5055[3:0]	D5055[7:4]		
COM16	10	D5056[3:0]	D5056[7:4]	D5057[3:0]	D5057[7:4]		D5118[3:0]	D5118[7:4]	D5119[3:0]	D5119[7:4]		
COM Outputs	Row Address (HEX)											

(Display Startline=10H)

**Table 6—GDDRAM address map showing Horizontal Address Increment A[2]=0, Column Address Re-map A[0]=0, Nibble Re-map A[1]=0, COM Re-map A[4]=1, and Display Start Line=16H (Data byte sequence: D0, D1, ... , D5118, D5119)**

		SEG0	SEG1	SEG2	SEG3		SEG124	SEG125	SEG126	SEG127	SEG Outputs	
		00		01			3E		3F		Column Address	
												(HEX)
COM0	00											
COM1	01			D0[3:0]	D0[7:4]		D61[3:0]	D61[7:4]				
												
COM78	4E			D4774[3:0]	D4774[7:4]		D4835[3:0]	D4835[7:4]				
COM79	4F											
COM Outputs	Row Address (HEX)											

(Display Startline=0)

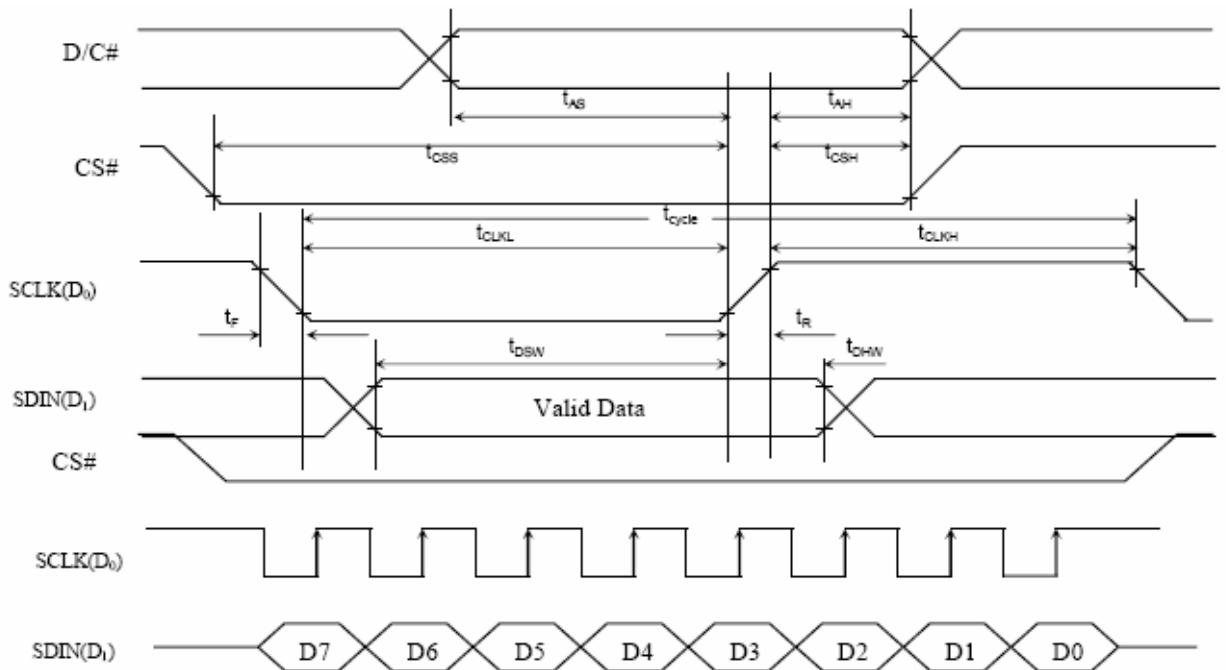
**Table 7—GDDRAM address map showing Horizontal Address Increment A[2]=0, Column Address Re-map A[0]=0, Nibble Re-map A[1]=0, COM Re-map A[4]=0, Display Start Line=00H (Data byte sequence: D0, D1, ... , D4834, D4835), Column Start Address=01H, Column End Address=3EH, Row Start Address=01H and Row End Address=4EH**

## 7.5 INTERFACE TIMING CHART

### Serial Interface Timing Characteristics

Symbol	Parameter	Min	Typ	Max	Unit
$t_{cycle}$	Clock Cycle Time	250	-	-	ns
$t_{AS}$	Address Setup Time	150	-	-	ns
$t_{AH}$	Address Hold Time	150	-	-	ns
$t_{CSS}$	Chip Select Setup Time	120	-	-	ns
$t_{CSH}$	Chip Select Hold Time	60	-	-	ns
$t_{DSW}$	Write Data Setup Time	100	-	-	ns
$t_{DHW}$	Write Data Hold Time	100	-	-	ns
$t_{CLKL}$	Clock Low Time	100	-	-	ns
$t_{CLKH}$	Clock High Time	100	-	-	ns
$t_R$	Rise Time	-	-	15	ns
$t_F$	Fall Time	-	-	15	ns

### Serial Interface Characteristics

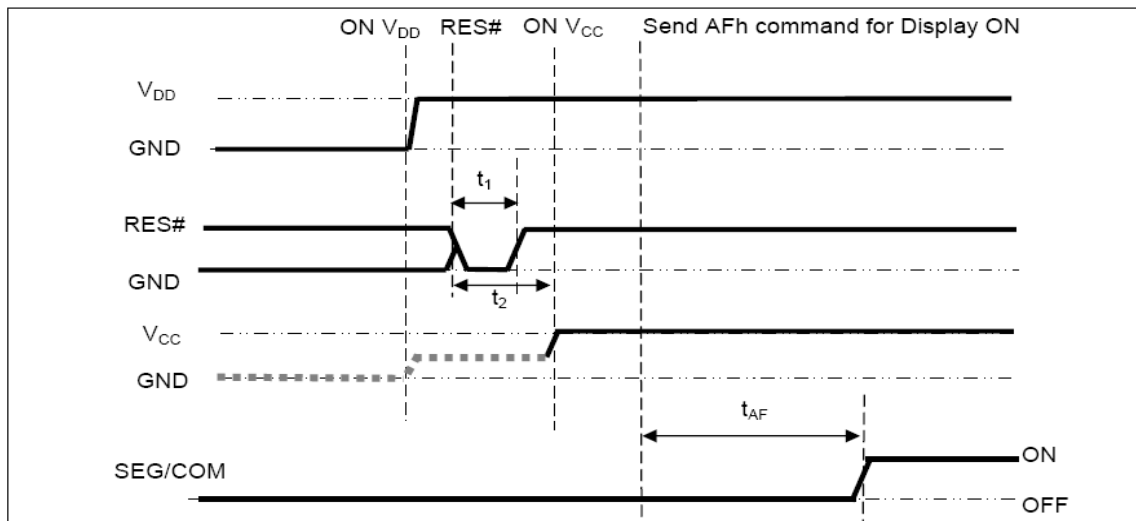


## 8. POWER ON / OFF SEQUENCE & APPLICATION CIRCUIT

### 8.1 POWER ON / OFF SEQUENCE

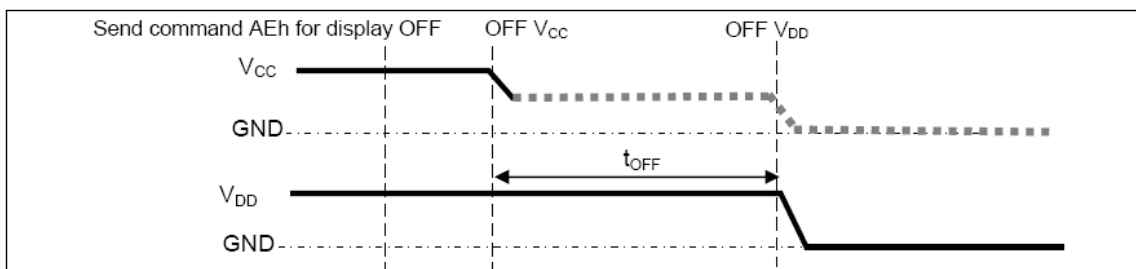
*Power ON sequence:*

1. Power ON VDD.
2. After VDD become stable, set RES# pin LOW (logic LOW) for at least 3us ( $t_1$ ) (4) and then HIGH (logic HIGH).
3. After set RES# pin LOW (logic LOW), wait for at least 3us ( $t_2$ ). Then Power ON VCC.(1)
4. After VCC become stable, send command AFh for display ON. SEG/COM will be ON after 100ms( $t_{AF}$ ).



*Power OFF sequence:*

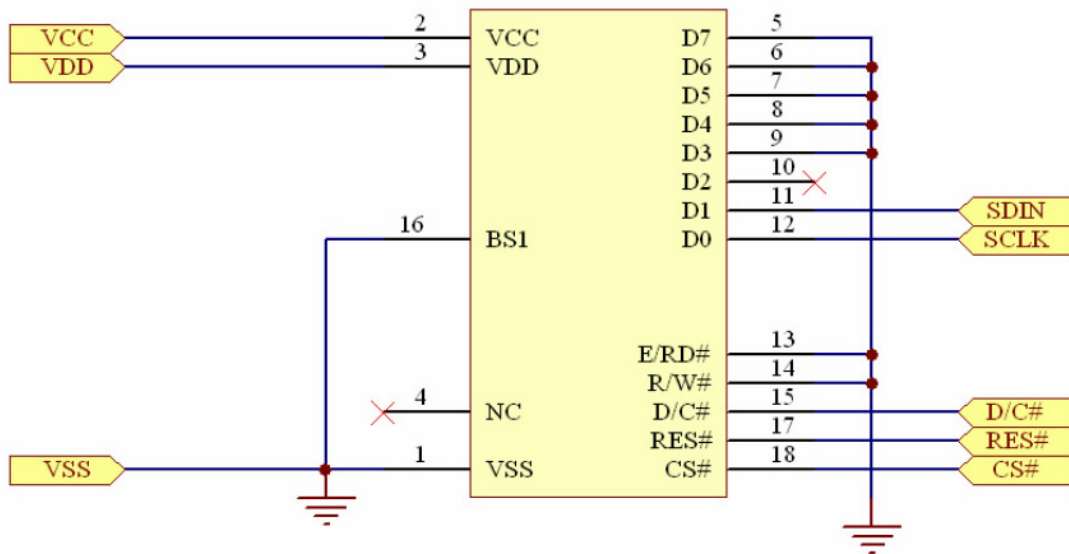
1. Send command AEh for display OFF.
2. Wait until panel discharges completely.
3. Power OFF VCC.(1), (2), (3)
4. Wait for  $t_{OFF}$ . Power OFF VDD. (where Minimum  $t_{OFF}$ =80ms (5) Typical  $t_{OFF}$ =100ms)



**Note:**

- (1) Since an ESD protection circuit is connected between VDD and VCC, VCC becomes lower than VDD whenever VDD is ON and VCC is OFF as shown in the dotted line of VCC.
- (2) VCC should be kept float (disable) when it is OFF.
- (3) Power Pins (VDD, VCC) can never be pulled to ground under any circumstance.
- (4) The register values are reset after  $t_1$ .
- (5) VDD should not be Power OFF before VCC Power OFF.

## 8.2 APPLICATION CIRCUIT



**Notes: This circuit is for Serial Peripheral Interface.**

## 8.3 COMMAND TABLE

Refer to SSD1325 IC Spec.

## **9. RELIABILITY TEST CONDITIONS**

No.	Items	Specification	Quantity
1	High temp. (Non-operation)	85 °C, 240hrs	5
2	High temp. (Operation)	70 °C, 120hrs	5
3	Low temp. (Operation)	-40 °C, 120hrs	5
4	High temp. / High humidity (Operation)	65 °C, 90%RH, 120hrs	5
5	Thermal shock (Non-operation)	-40 °C ~85 °C (-40 °C /30min; transit /3min; 85 °C /30min; transit /3min) 1cycle: 66min, 100 cycles	5
6	Vibration	Frequency : 5~50HZ, 0.5G Scan rate : 1 oct/min Time : 2 hrs/axis Test axis : X, Y, Z	1 Carton
7	Drop	Height: 120cm Sequence : 1 angle 、 3 edges and 6 faces Cycles: 1	1 Carton
8	ESD (Non-operation)	Air discharge model, ±8kV, 10 times	5

### **Test and measurement conditions**

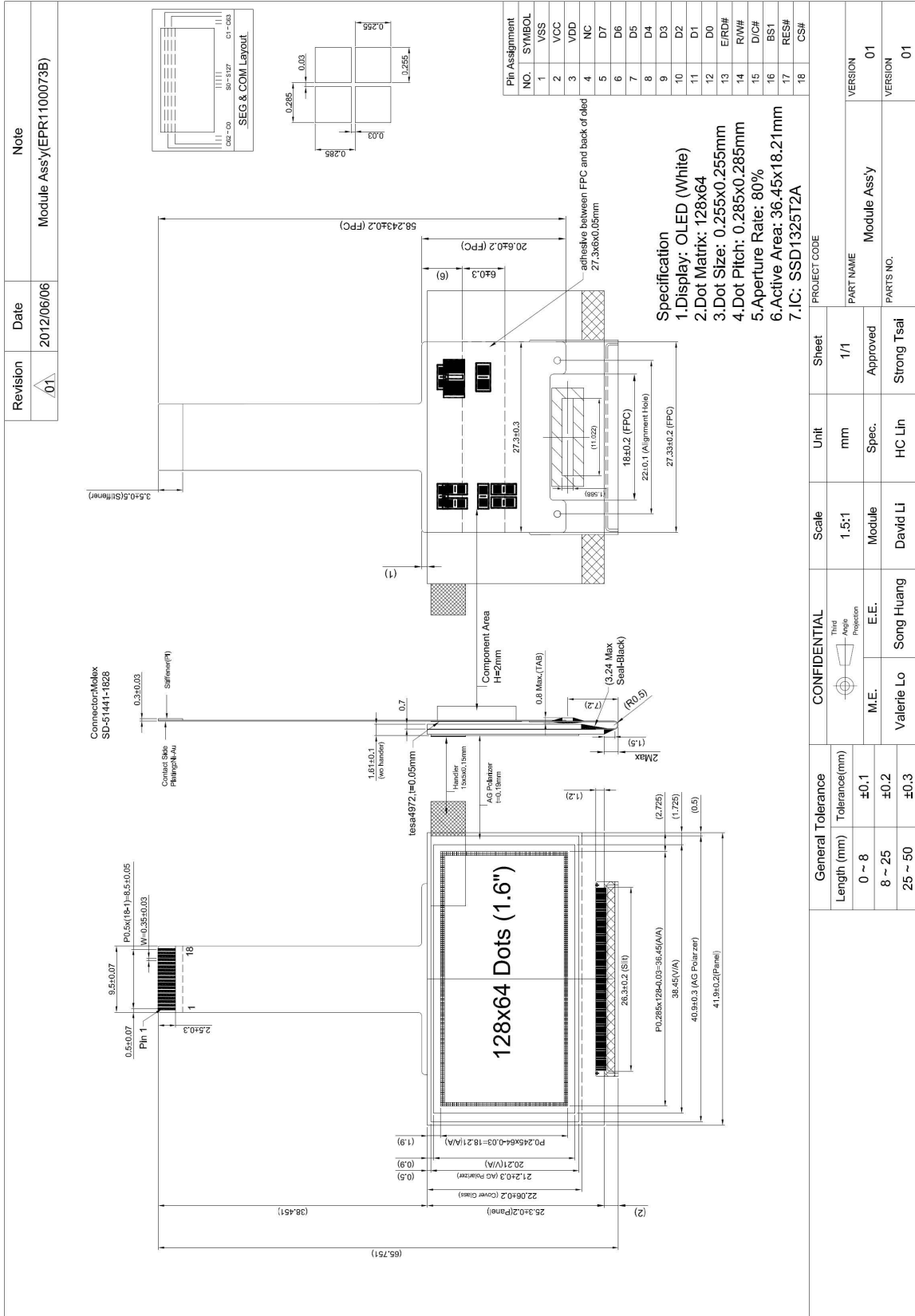
1. All measurements shall not be started until the specimens attain to temperature stability.
2. All-pixels-on is used as operation test pattern.
3. The degradation of Polarizer are ignored for item 1, 4 & 5.

### **Evaluation criteria**

1. The function test is OK.
2. No observable defects.
3. Luminance: > 50% of initial value.
4. Current consumption: within ± 50% of initial value.



# 10. EXTERNAL DIMENSION



## 11. PACKING SPECIFICATION

Revision ▲.01	Date 2012/07/30	Note Packing Tray Instruction
------------------	--------------------	----------------------------------

**1** Module Face down 旋轉放置 x 1 pcs

**2** Packing Tray P/N:3008000453 330x270x11.7mm, l=0.7mm x 1 pcs

**3** 5G 矽膠乾膜 P/N:3010000000.3 x4

**4** 真空包裝袋 ONVLDPE P/N:30030000012 480x285x90mm 抽真空4秒 x 9 pcs

**5** Antistatic Bubble Bag P/N:3003000016 440X(350+450)mm

**6** Pizza Box P/N:3001000005 345x285x88, B浪 x 2 pcs

**7** 單色 Carton P/N:3000000009 385x305x203mm

**8** Label P/N:3006000000 x 2 pcs

旋轉堆疊

以膠帶固定

Item	Part No.	Description	QTY
1		Module Assy	384
2	3008000453	Tray 330x270x11.7mm, PS, l=0.7mm	18
3	3010000003	5G 矽膠乾膜	8
4	3003000012	真空包裝袋 480x285x90mm	2
5	3003000016	Antistatic Bubble Bag 440x(350+450)mm	2
6	3001000005	Pizza Box 345x285x88, B浪	2
7	3000000009	單色 Carton, 385x305x203mm	1
8	3006000000	Label	3
9	3208000125	封箱膠帶, W=48mm, L=910cm	

<b>General Tolerance</b>		<b>CONFIDENTIAL</b>		PROJECT CODE
Length (mm)	Tolerance(mm)	Third Angle Projection	Scale	Sheet
0 ~ 8	±0.1	M.E.	1:3.5	1/1
8 ~ 25	±0.2	E.E.	Module	Approved
25 ~ 50	±0.3	Iven Lee	Valerie Lo	Strong Tsai
			Irene Fan	REVISION 01
				Packing Tray Instruction
				REVISION 01

## 12. APPENDIXES

### APPENDIX 1: DEFINITIONS

#### A. DEFINITION OF CHROMATICITY COORDINATE

The chromaticity coordinate is defined as the coordinate value on the CIE 1931 color chart for R, G, B, W.

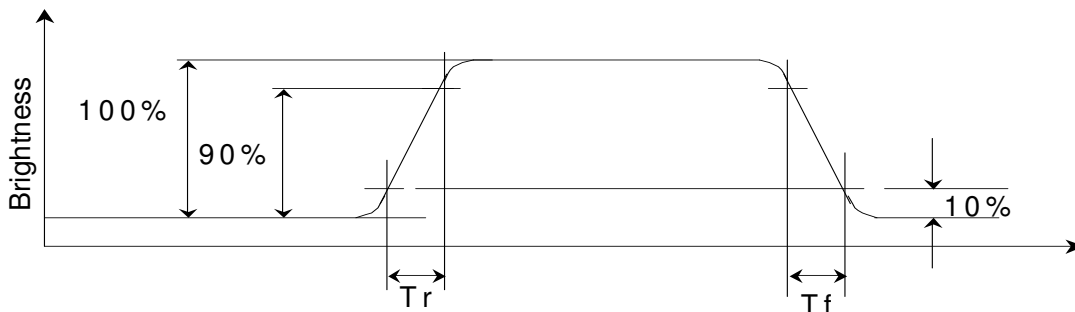
#### B. DEFINITION OF CONTRAST RATIO

The contrast ratio is defined as the following formula:

$$\text{Contrast Ratio} = \frac{\text{Luminance of all pixels on measurement}}{\text{Luminance of all pixels off measurement}}$$

#### C. DEFINITION OF RESPONSE TIME

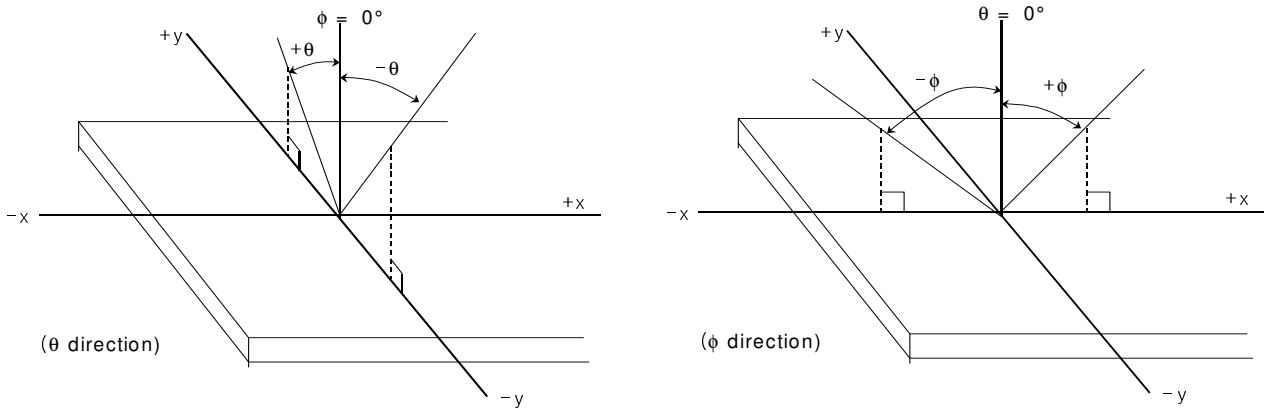
The definition of turn-on response time  $T_r$  is the time interval between a pixel reaching 10% of steady state luminance and 90% of steady state luminance. The definition of turn-off response time  $T_f$  is the time interval between a pixel reaching 90% of steady state luminance and 10% of steady state luminance. It is shown in Figure 2.



**Figure 2: Response time**

### D. DEFINITION OF VIEWING ANGLE

The viewing angle is defined as Figure 3. Horizontal and vertical (H & V) angles are determined for viewing directions where luminance varies by 50% of the perpendicular value.

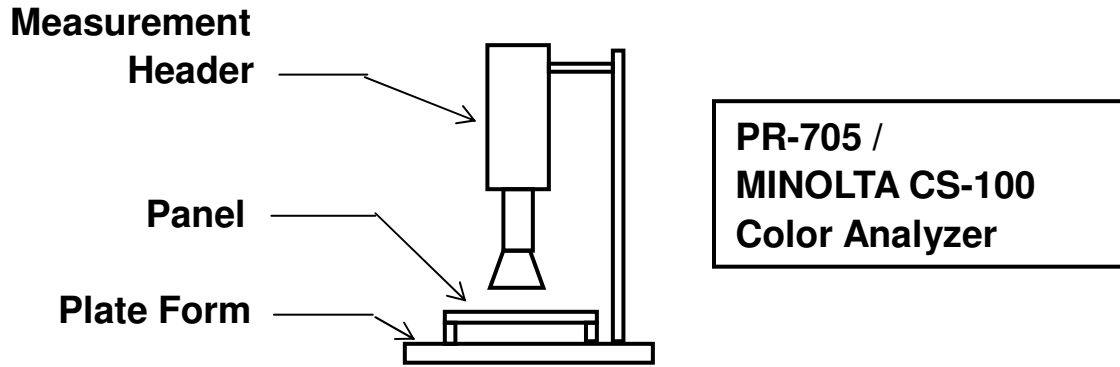


**Figure 3: Viewing Angle**

## APPENDIX 2: MEASUREMENT APPARATUS

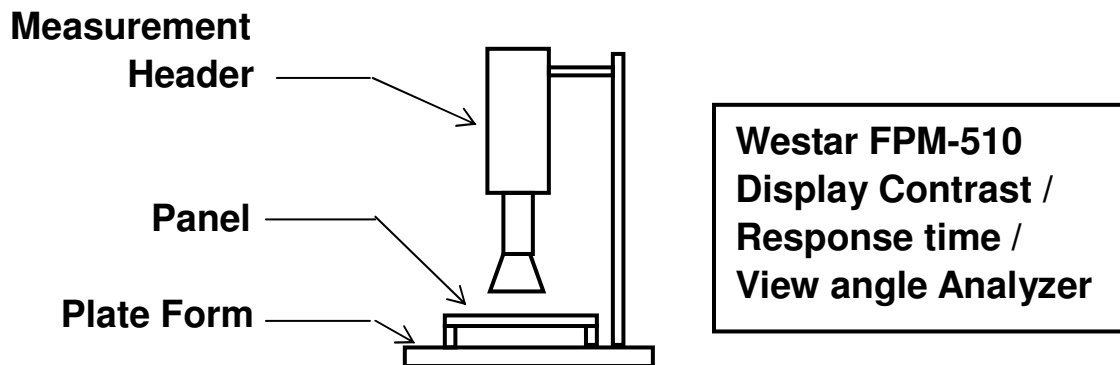
### A. LUMINANCE/COLOR COORDINATE

PHOTO RESEARCH PR-705, MINOLTA CS-100

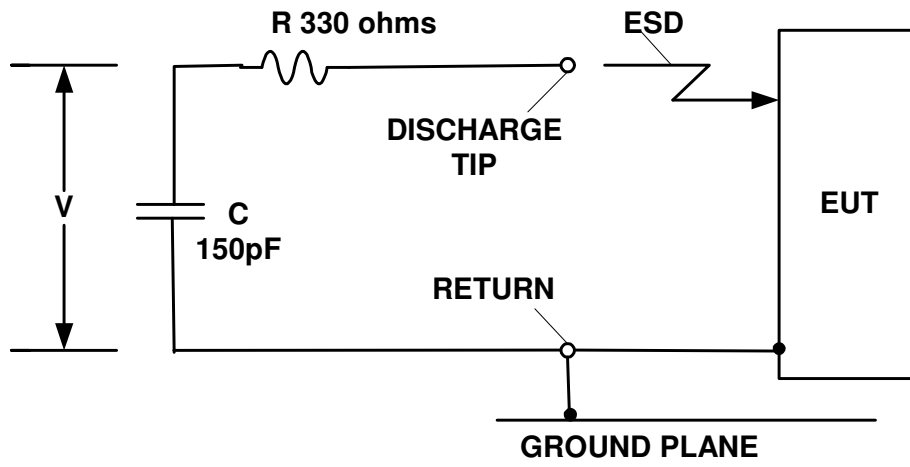


### B. CONTRAST / RESPONSE TIME / VIEW ANGLE

WESTAR CORPORATION FPM-510



### C. ESD ON AIR DISCHARGE MODE



## **APPENDIX 3: PRECAUTIONS**

### **A. RESIDUE IMAGE**

Because the pixels are lighted in different time, the luminance of active pixels may reduce or differ from inactive pixels. Therefore, the residue image will occur. To avoid the residue image, every pixel needs to be lighted up uniformly.