US Micro Products
Electronic Products for the OEM

OLED PRODUCT SPECIFICATION

MANUFACTURED BY RITDISPLAY

RITEK GROUP
RiTdisplay Corporation

PART NUMBER:	**USMP-P21501**
DESCRIPTION:	2.4", 128 x 22, Yellow, COG, SSD1305

ISSUE DATE	APPROVED BY (Customer Use Only)	CHECKED BY	PREPARED BY
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REVISION RECORD

REV.	REVISION DESCRIPTION	REV. DATE	REMARK
X01	■ INITIAL RELEASE	2008. 05. 07	
X02	■ Add the operating conditions for different luminance ■ Add the panel electrical specifications ■ Add the application circuit	2008. 06. 13	Page 4, 6, 7, 8 & 14
A01	■ Transfer from X version ■ Modify definition of panel thickness ■ Add the information of module weight ■ Add the packing specification	2009. 05. 05	Page 4, 5 & 17

CONTENTS

1. SCOPE

The purpose of this specification is to define the general provisions and quality requirements that apply to the supply of display cells manufactured by RiTdisplay. This document, together with the Module Assembly Drawing, is the highest-level specification for this product. It describes the product, identifies supporting documents and contains specifications.

2. WARRANTY

RiTdisplay warrants that the products delivered pursuant to this specification (or order) will conform to the agreed specifications for twelve (12) months from the shipping date ("Warranty Period"). RiTdisplay is obligated to repair or replace the products which are found to be defective or inconsistent with the specifications during the Warranty Period without charge, on condition that the products are stored or used as the conditions specified in the specifications. Nevertheless, RiTdisplay is not obligated to repair or replace the products without charge if the defects or inconsistency are caused by the force majeure or the reckless behaviors of the customer.
After the Warranty Period, all repairs or replacements of the products are subject to charge.

3. FEATURES

- Small molecular organic light emitting diode.
- Color : Yellow
- Panel resolution : 128*22
- Driver IC : SSD1305
- Excellent Quick response time : 10μs
- Extremely thin thickness for best mechanism design : 2.15 mm
- High contrast : 2000:1
- Wide viewing angle : 160°
- Strong environmental resistance.
- 8-bit 6800-series Parallel Interface, 8-bit 8080-series Parallel Interface, Serial Peripheral Interface, I^2C Interface.
- Wide range of operating temperature : -40 to 70°C
- Anti-glare polarizer.

4. MECHANICAL DATA

NO	ITEM	SPECIFICATION	UNIT
1	Dot Matrix	128 x 22	dot
2	Dot Size	0.43 (W) x 0.51 (H)	mm^2
3	Dot Pitch	0.46 (W) x 0.54 (H)	mm^2
4	Aperture Rate	88	%
5	Active Area	58.85 (W) x 11.85 (H)	mm^2
6	Panel Size	63.3 (W) x 20.8 (H)	mm^2
7*	Panel Thickness	1.42 ± 0.1	mm
8	Module Size	64.8 (W) x 59.5 (H) x 2.15 (T)	mm^3
9	Diagonal A/A size	2.36	inch
10	Module Weight	4.97 ± 10%	gram

* Panel thickness includes substrate glass, cover glass and UV glue thickness.

5. MAXIMUM RATINGS

ITEM	MIN	MAX	UNIT	Condition	Remark
Supply Voltage (V_{DD})	-0.3	3.5	V	Ta = 25°C	IC maximum rating
Supply Voltage (Vcc)	8	16	V	Ta = 25°C	IC maximum rating
Operating Temp.	-40	70	°C		
Storage Temp	-40	85	°C		
Humidity		85	%		
Life Time	33,000	-	Hrs	120 cd/m^2, 50% checkerboard	Note (1)
Life Time	40,000	-	Hrs	100 cd/m^2, 50% checkerboard	Note (2)
Life Time	50,000	-	Hrs	80 cd/m^2, 50% checkerboard	Note (3)

Note:

(A) Under Vcc = 12V, Ta = 25°C, 50% RH.

(B) Life time is defined the amount of time when the luminance has decayed to less than 50% of the initial measured luminance.

(1) Setting of 120 cd/m^2 :

- Contrast setting : 0xACH
- Frame rate : 105Hz
- Duty setting : 1/22

(2) Setting of 100 cd/m^2 :

- Contrast setting : 0x8EH
- Frame rate : 105Hz
- Duty setting : 1/22

(3) Setting of 80 cd/m^2 :

- Contrast setting : 0x6DH
- Frame rate : 105Hz
- Duty setting : 1/22

6. ELECTRICAL CHARACTERISTICS

6.1 D.C ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETERS	TEST CONDITION	MIN	TYP	MAX	UNIT
V_{CC}	Analog power supply (for OLED panel)		11.5	12	12.5	V
V_{DD}	Digital power supply		2.4	-	3.5	V
I_{DD}	Operating current for V_{DD} V_{DD} = 2.7V, V_{CC} = 12V, IREF = 10uA No loading, All Display ON	Contrast=FF	-	100	300	uA
I_{CC}	Operating current for V_{CC} V_{DD} = 2.7V, V_{CC} = 12V, IREF = 10uA, No loading, All Display ON	Contrast=FF	-	550	1000	uA
V_{IH}	Hi logic input level		0.8* V_{DD}	-	-	V
V_{IL}	Low logic input level		0	-	0.2* V_{DD}	V
V_{OH}	Hi logic output level		0.9* V_{DD}	-	-	V
V_{OL}	Low logic output level		0	-	0.1* V_{DD}	V
I_{SEG}	Segment on output current V_{DD}=2.7V, V_{CC}=12V, IREF=10uA, Display on, Segment pin under test is connected with a 20K resistive load to V_{SS}	Contrast=FF	294	320	346	uA
		Contrast=AF	-	220	-	uA
		Contrast=7F	-	159	-	uA
		Contrast=3F	-	79	-	uA
		Contrast=0F	-	19	-	uA

6.2 ELECTRO-OPTICAL CHARACTERISTICS

PANEL ELECTRICAL SPECIFICATIONS

PARAMETER	MIN	TYP.	MAX	UNITS	COMMENTS
Normal mode current consumption	-	14	16	mA	All pixels on (1)
Standby mode current consumption	-	2	3	mA	Standby mode 10% pixels on (2)
Normal mode power consumption	-	168	192	mW	All pixels on (1)
Standby mode power consumption	-	24	36	mW	Standby mode 10% pixels on (2)
Pixel Luminance	80	100		cd/m^2	Display Average
Standby Luminance		20		cd/m^2	
CIEx (Yellow)	0.43	0.47	0.51		CIE1931
CIEy (Yellow)	0.45	0.49	0.53		CIE1931
Dark Room Contrast	2000:1				
Viewing Angle	160			degree	
Response Time		10		μs	

(1) Normal mode condition :

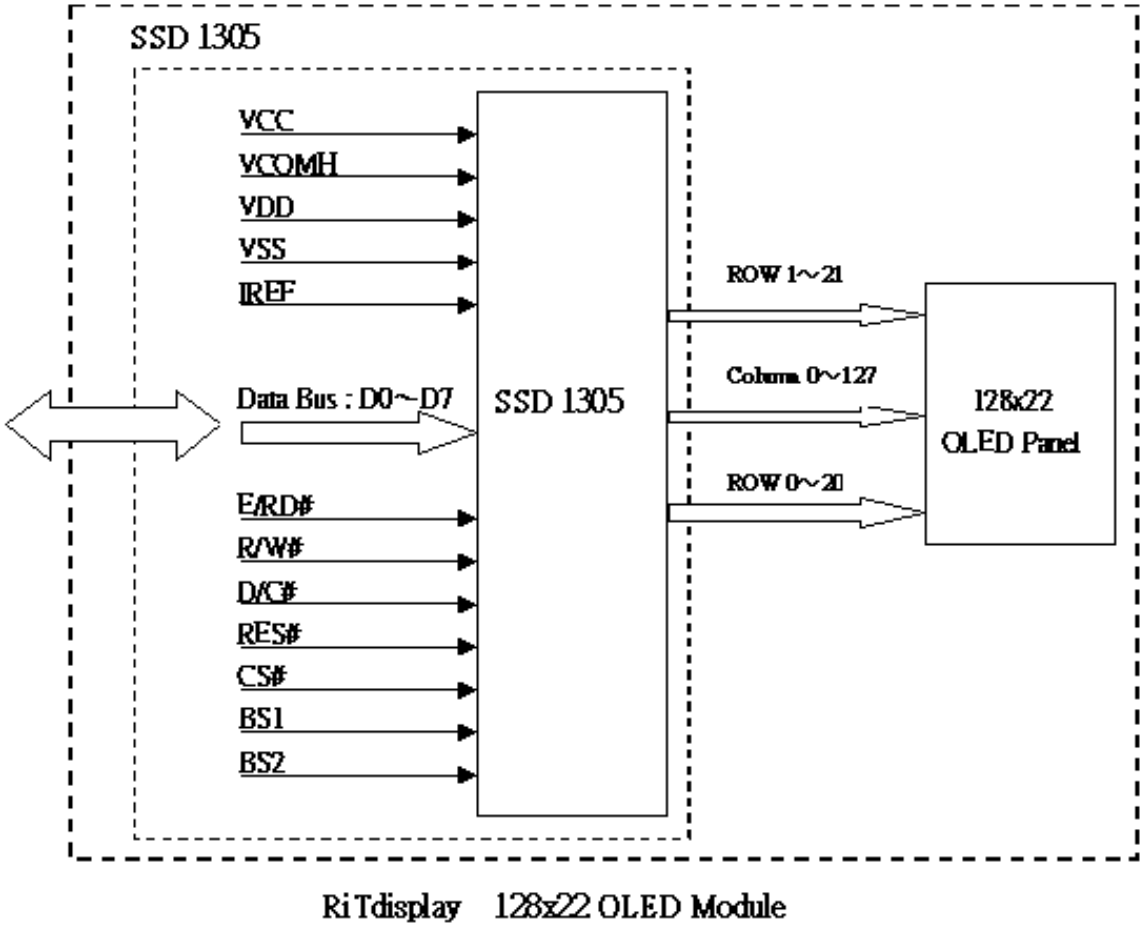
- Driving Voltage : 12V
- Contrast setting : 0x8EH
- Frame rate : 105Hz
- Duty setting : 1/22

(2) Standby mode condition :

- Driving Voltage : 12V
- Contrast setting : 0x12H
- Frame rate : 105Hz
- Duty setting : 1/22

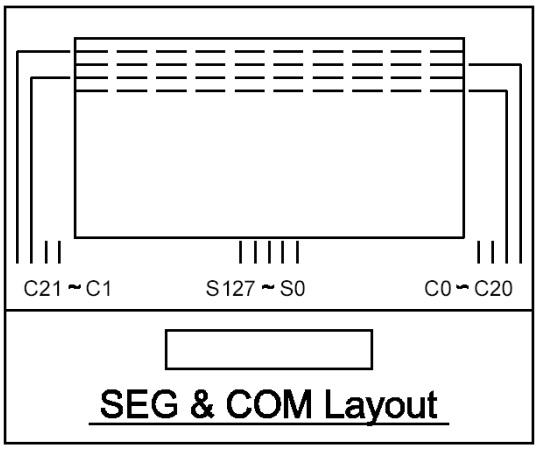
7. INTERFACE

7.1 FUNCTION BLOCK DIAGRAM



RiTdisplay 128x22 OLED Module

7.2 PANEL LAYOUT DIAGRAM



7.3 PIN ASSIGNMENTS

Pin No.	Pin Name	Description
1	NC	No connection.
2	VSS	This is a ground pin.
3	VSS	This is a ground pin.
4	NC	No connection.
5	VDD	Voltage power supply for logic
6	BS1	MCU interface selection pin.
7	BS2	MCU interface selection pin.
8	CS#	Chip select pin. The driver IC will be selected When CS pin is active low.
9	RES#	Hardware reset signal
10	D/C#	Data/Command control pin. When it pulled high, the input at D0-D7 is treated as display data. When it pulled low, the input at D0-D7 is transferred to command register
11	R/W#	Write strobe signal and reads data at the low level
12	E(RD#)	Read strobe signal and reads data at the low level
13	D0	8-bit data bus
14	D1	8-bit data bus
15	D2	8-bit data bus
16	D3	8-bit data bus
17	D4	8-bit data bus
18	D5	8-bit data bus
19	D6	8-bit data bus
20	D7	8-bit data bus
21	IREF	The current reference input pin, this pin should be connected to ground through a resistor.
22	VCOMH	The COM voltage reference pin, this pin should be connected to ground through a capacitor.
23	VCC	Positive OLED high voltage power supply
24	NC	No connection.

7.4 GRAPHIC DISPLAY DATA RAM ADDRESS MAP

The GDDRAM is a bit mapped static RAM holding the bit pattern to be displayed. The size of the RAM is 132x64= 8448bits.

For mechanical flexibility, re-mapping on both Segment and Common outputs can be selected by software.

OUT	Row Address Direction='1'	Row Address Direction='0'			OUT	SEG0	SEG1	SEG2	SEG3	SEG4	SEG5	SEG6	SEG7	...	SEG128	SEG129	SEG130	SEG131
				Column Address Remap='1'		0x83h	0x82h	0x81h	0x80h	0x7Fh	0x7Eh	0x7Dh	0x7Ch		0x03h	0x02h	0x01h	0x00h
				Column Address Remap='0'		0x00h	0x01h	0x02h	0x03h	0x04h	0x05h	0x06h	0x07h		0x80h	0x81h	0x82h	0x83h
COM0	0x3Fh	0x00h	PAGE 0		D0													
COM1	0x3Eh	0x01h			D1													
COM2	0x3Dh	0x02h			D2													
COM3	0x3Ch	0x03h			D3													
COM4	0x3Bh	0x04h			D4													
COM5	0x3Ah	0x05h			D5													
COM6	0x39h	0x06h			D6													
COM7	0x38h	0x07h			D7													
COM8	0x37h	0x08h	PAGE 1		D0													
COM9	0x36h	0x09h			D1													
COM10	0x35h	0x0Ah			D2													
COM11	0x34h	0x0Bh			D3													
COM12	0x33h	0x0Ch			D4													
COM13	0x32h	0x0Dh			D5													
COM14	0x31h	0x0Eh			D6													
COM15	0x30h	0x0Fh			D7													
COM16	0x2Fh	0x10h	PAGE 2		D0													
COM17	0x2Eh	0x11h			D1													
COM18	0x2Dh	0x12h			D2													
COM19	0x2Ch	0x13h			D3													
COM20	0x2Bh	0x14h			D4													
COM21	0x2Ah	0x15h			D5													
COM22	0x29h	0x16h			D6													
COM23	0x28h	0x17h			D7													
.																		
.																		
.																		
COM48	0x0Fh	0x30h	PAGE 6		D0													
COM49	0x0Eh	0x31h			D1													
COM50	0x0Dh	0x32h			D2													
COM51	0x0Ch	0x33h			D3													
COM52	0x0Bh	0x34h			D4													
COM53	0x0Ah	0x35h			D5													
COM54	0x09h	0x36h			D6													
COM55	0x08h	0x37h			D7													
COM56	0x07h	0x38h	PAGE 7		D0													
COM57	0x06h	0x39h			D1													
COM58	0x05h	0x3Ah			D2													
COM59	0x04h	0x3Bh			D3													
COM60	0x03h	0x3Ch			D4													
COM61	0x02h	0x3Dh			D5													
COM62	0x01h	0x3Eh			D6													
COM63	0x00h	0x3Fh			D7													

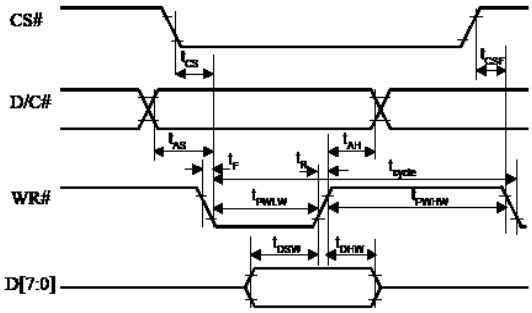
7.5 INTERFACE TIMING CHART

8080-Series MCU Parallel Interface Timing Characteristics

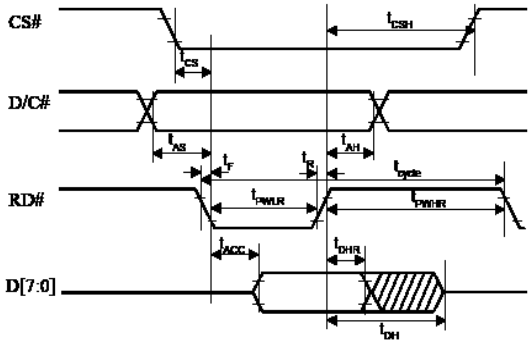
(V_{DD} - V_{SS} = 2.4V to 3.5V, V_{DDIO} = V_{DD}, T_A = 25°C)

Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time	300	-	-	ns
t_{AS}	Address Setup Time	10	-	-	ns
t_{AH}	Address Hold Time	0	-	-	ns
t_{DSW}	Write Data Setup Time	40	-	-	ns
t_{DHW}	Write Data Hold Time	7	-	-	ns
t_{DHR}	Read Data Hold Time	20	-	-	ns
t_{OH}	Output Disable Time	-	-	70	ns
t_{ACC}	Access Time	-	-	140	ns
t_{PWLR}	Read Low Time	120	-	-	ns
t_{PWLW}	Write Low Time	60	-	-	ns
t_{PWHR}	Read High Time	60	-	-	ns
t_{PWHW}	Write High Time	60	-	-	ns
t_R	Rise Time	-	-	40	ns
t_F	Fall Time	-	-	40	ns
t_{CS}	Chip select setup time	0	-	-	ns
t_{CSH}	Chip select hold time to read signal	0	-	-	ns
t_{CSF}	Chip select hold time	20	-	-	ns

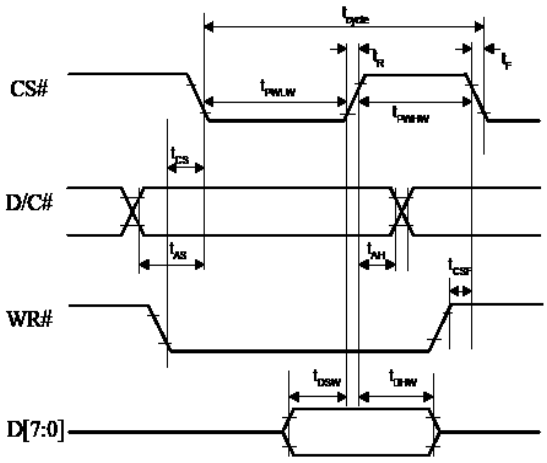
Write cycle (Form 1)



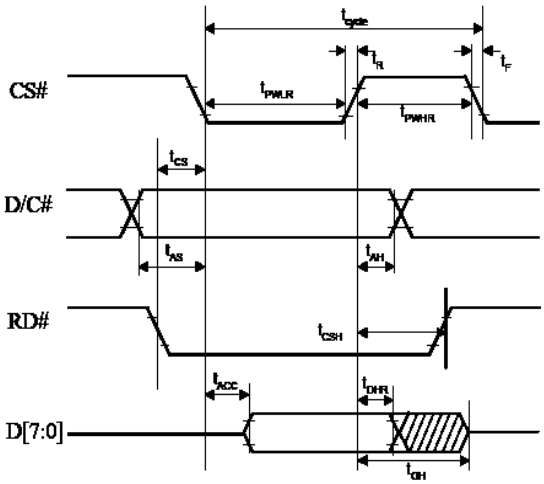
Read cycle (Form 1)



Write cycle (Form 2)



Read cycle (Form 2)

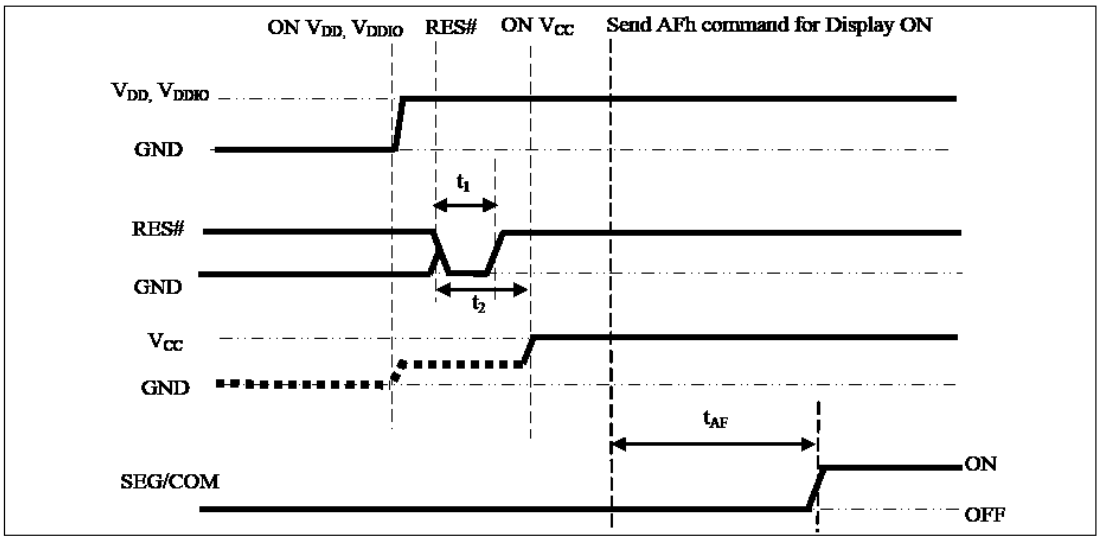


8. POWER ON / OFF SEQUENCE & APPLICATION CIRCUIT

8.1 POWER ON / OFF SEQUENCE

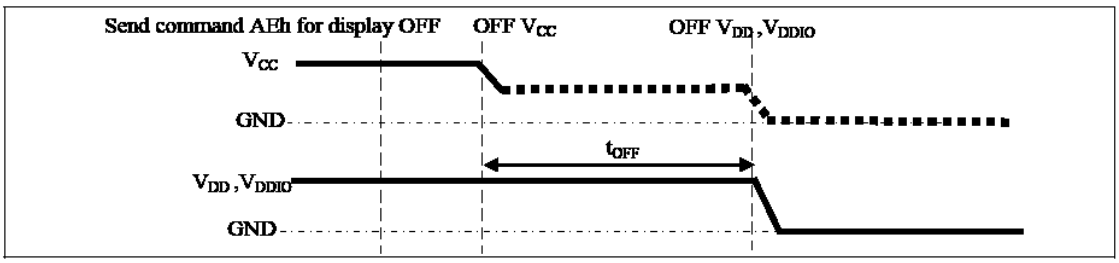
Power ON sequence:

1. Power ON V_{DD}, V_{DDIO}.
2. After V_{DD}, V_{DDIO} become stable, set RES# pin LOW (logic low) for at least 3us(t_1) and then HIGH (logic high).
3. After set RES# pin LOW (logic low), wait for at least 3us(t_2).Then Power ON V_{CC}.(1)
4. After V_{CC} become stable, send command AFh for display ON. SEG/COM will be ON after 100ms(t_{AF}).



Power OFF sequence:

1. Send command AEh for display OFF.
2. Power OFF V_{CC}. (1), (2)
3. Wait for t_{OFF}. Power OFF V_{DD}, V_{DDIO}. (where Minimum t_{OFF}=80ms, Typical t_{OFF}=100ms)

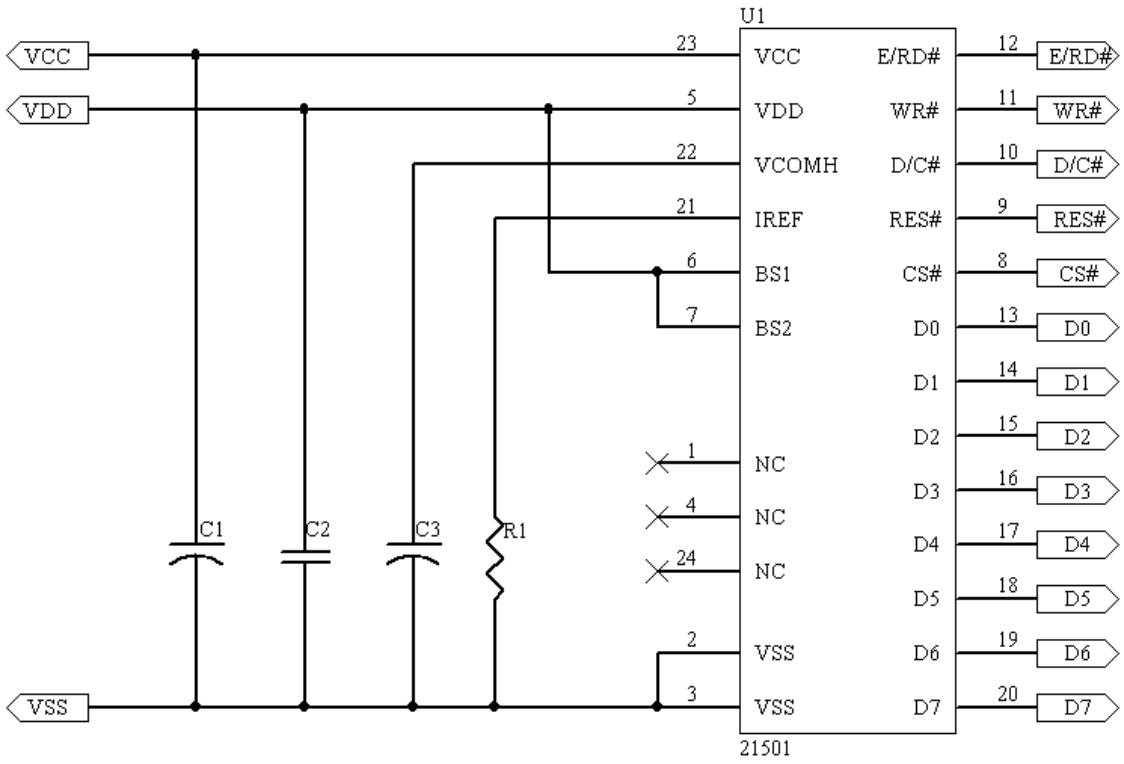


Note:

(1) Since an ESD protection circuit is connected between V_{DD}, V_{DDIO} and V_{CC}, V_{CC} becomes lower than V_{DD} whenever V_{DD}, V_{DDIO} is ON and V_{CC} is OFF as shown in the dotted line of V_{CC} in above figures.

(2) V_{CC} should be disabled when it is OFF.

8.2 APPLICATION CIRCUIT



Component :

C1, C3: 4.7uF/25V (Tantalum type), or solid tantalum 4.7uF/ 25V/ A Case (Vishay 572D)

C2: 4.7uF /16V (0805)

R1: 2M ohm /1% (0603)

This circuit is for 8080 interface.

8.3 COMMAND TABLE

Refer to IC Spec.: SSD1305

9. RELIABILITY TEST CONDITIONS

No.	Items	Specification	Quantity
1	High temp. (Non-operation)	85°C, 240hrs	5
2	High temp. (Operation)	70°C, 120hrs	5
3	Low temp. (Operation)	-40°C, 120hrs	5
4	High temp. / High humidity (Operation)	65°C, 90%RH, 120hrs	5
5	Thermal shock (Non-operation)	-40°C ~85°C (-40°C /30min; transit /3min; 85°C /30min; transit /3min) 1cycle: 66min, 100 cycles	5
6	Vibration	Frequency : 5~50HZ, 0.5G Scan rate : 1 oct/min Time : 2 hrs/axis Test axis : X, Y, Z	1 Carton
7	Drop	Height: 120cm Sequence : 1 angle、3 edges and 6 faces Cycles: 1	1 Carton
8	ESD (Non-operation)	Air discharge model, ±8kV, 10 times	5

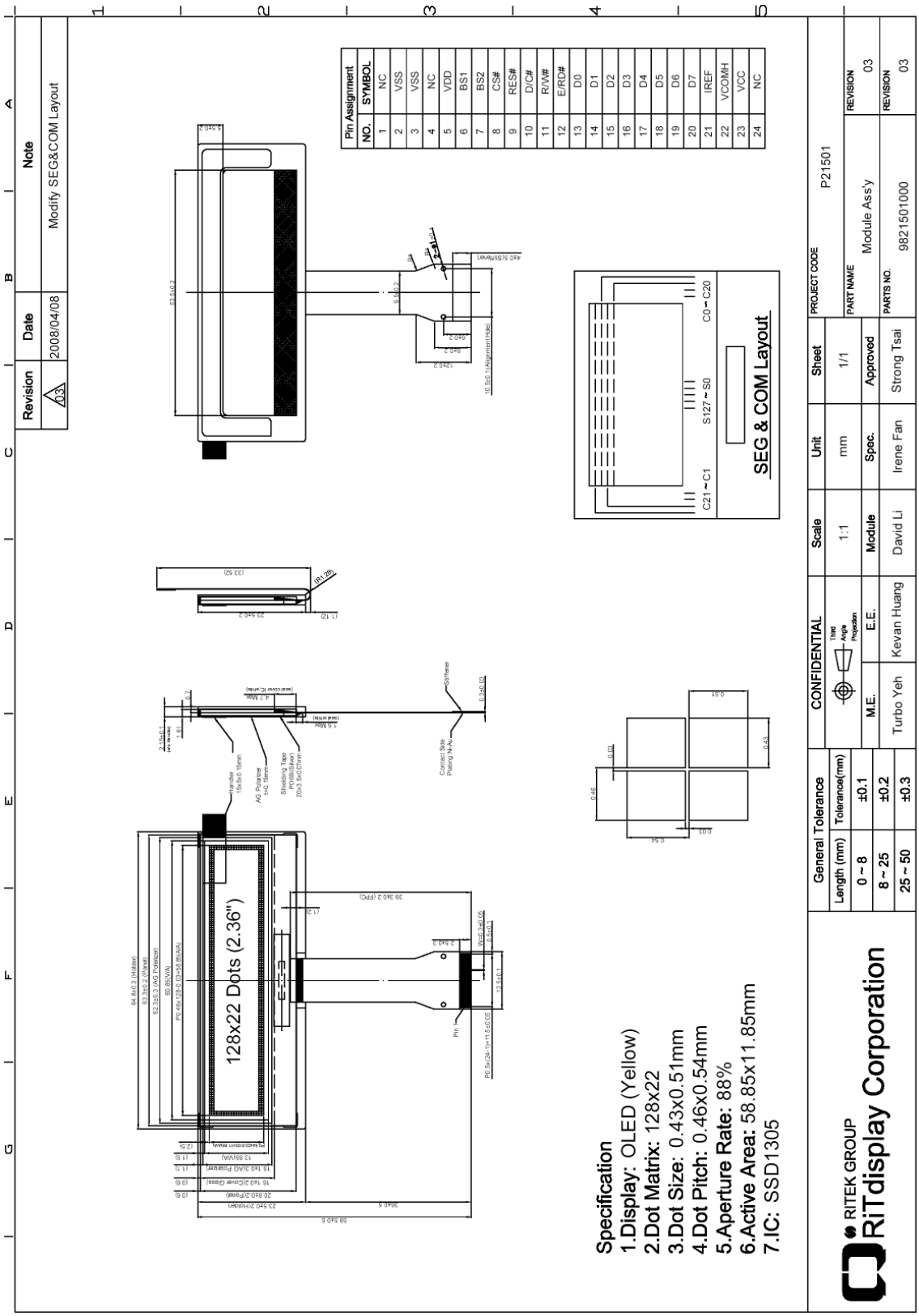
Test and measurement conditions

1. All measurements shall not be started until the specimens attain to temperature stability.
2. All-pixels-on is used as operation test pattern.
3. The degradation of Polarizer are ignored for item 1, 4 & 5.

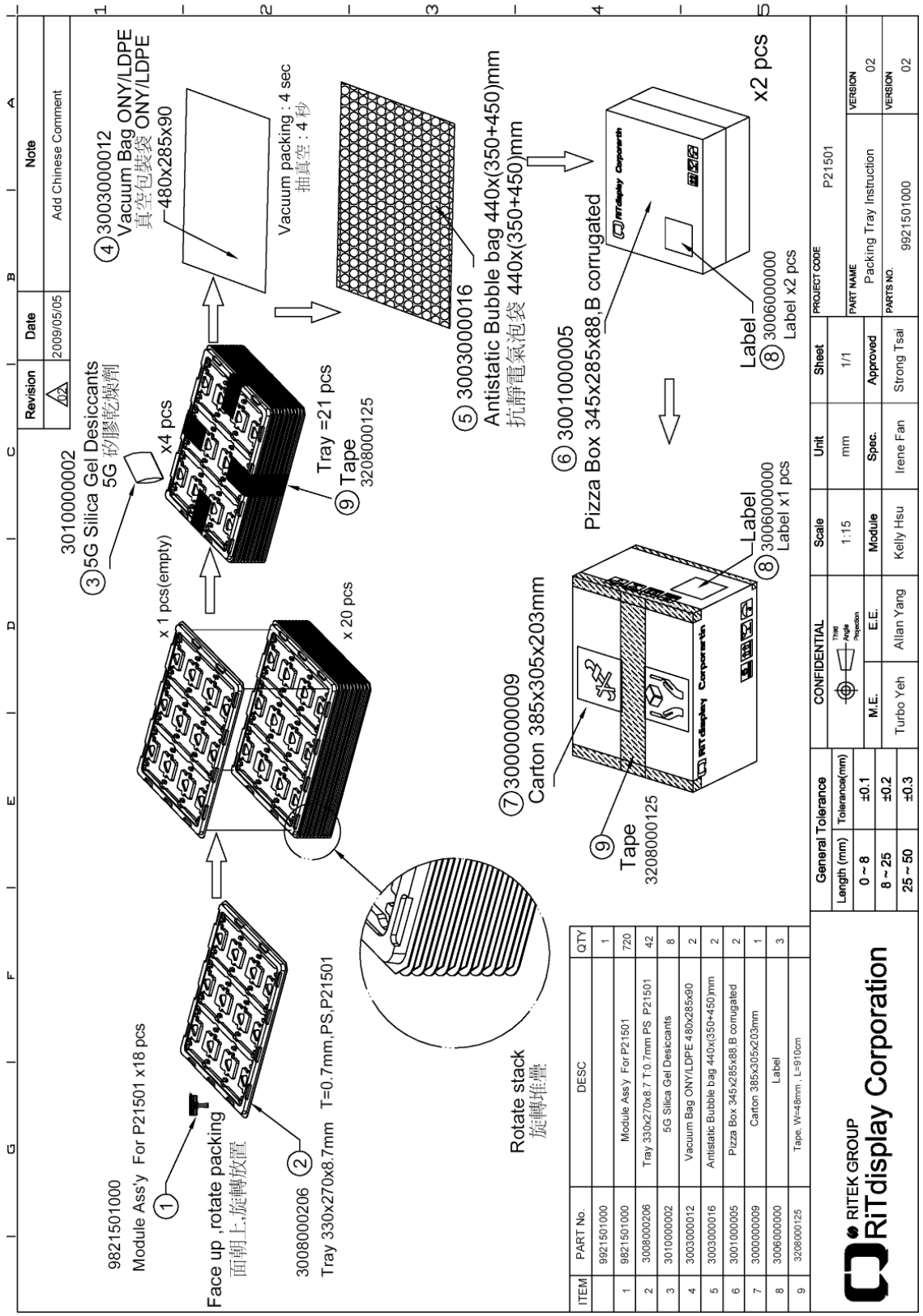
Evaluation criteria

1. The function test is OK.
2. No observable defects.
3. Luminance: > 50% of initial value.
4. Current consumption: within ± 50% of initial value.

10. EXTERNAL DIMENSION



11. PACKING SPECIFICATION



12. APPENDIXES

APPENDIX 1: DEFINITIONS

A. DEFINITION OF CHROMATICITY COORDINATE

The chromaticity coordinate is defined as the coordinate value on the CIE 1931 color chart for R, G, B, W.

B. DEFINITION OF CONTRAST RATIO

The contrast ratio is defined as the following formula:

$$\text{Contrast Ratio} = \frac{\text{Luminance of all pixels on measurement}}{\text{Luminance of all pixels off measurement}}$$

C. DEFINITION OF RESPONSE TIME

The definition of turn-on response time Tr is the time interval between a pixel reaching 10% of steady state luminance and 90% of steady state luminance. The definition of turn-off response time Tf is the time interval between a pixel reaching 90% of steady state luminance and 10% of steady state luminance. It is shown in Figure 2.

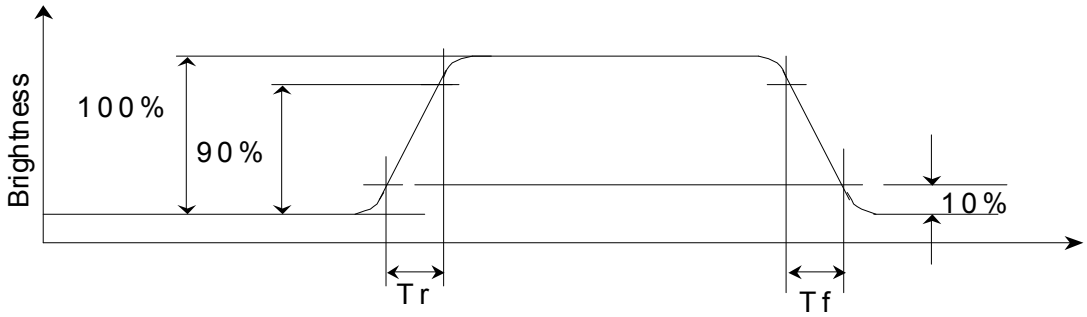


Figure 2 Response time

D. DEFINITION OF VIEWING ANGLE

The viewing angle is defined as Figure 3. Horizontal and vertical (H & V) angles are determined for viewing directions where luminance varies by 50% of the perpendicular value.

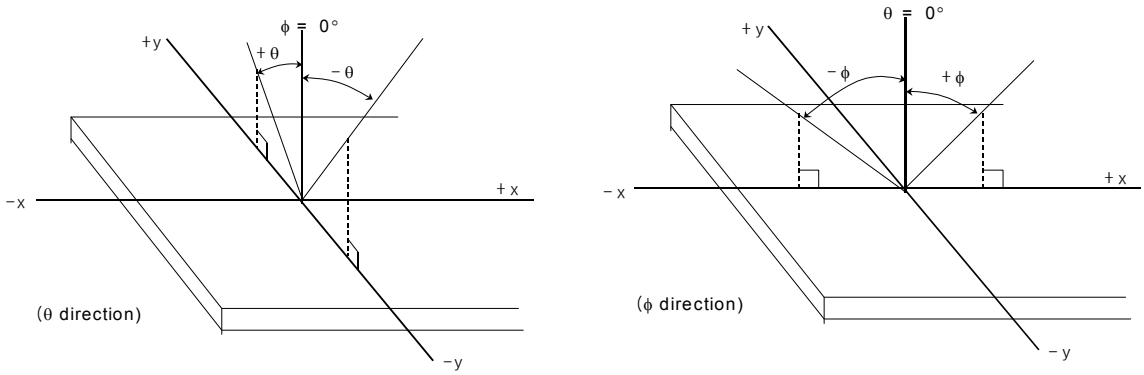


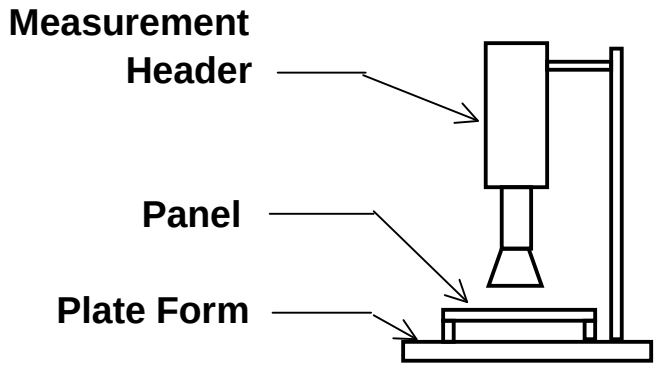
Figure 3 Viewing angle

REV.: A01 2009/05/05

APPENDIX 2: MEASUREMENT APPARATUS

A. LUMINANCE/COLOR COORDINATE

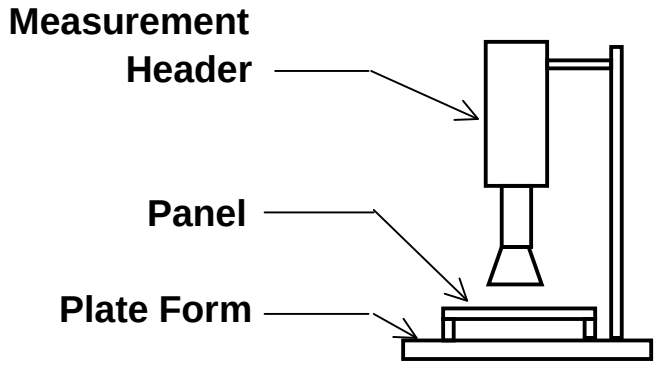
PHOTO RESEARCH PR-705, MINOLTA CS-100



**PR-705 /
MINOLTA CS-100
Color Analyzer**

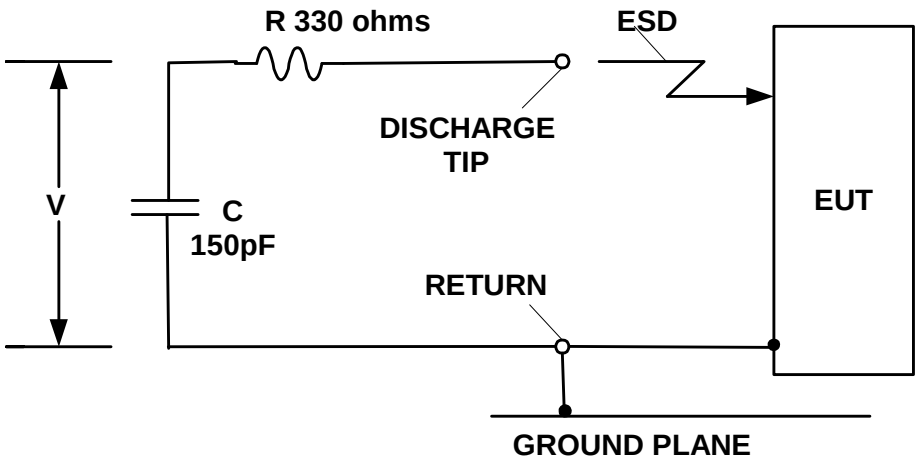
B. CONTRAST / RESPONSE TIME / VIEWING ANGLE

WESTAR CORPORATION FPM-510



**Westar FPM-510
Display Contrast /
Response time /
View angle Analyzer**

C. ESD ON AIR DISCHARGE MODE



APPENDIX 3: PRECAUTIONS

A. RESIDUE IMAGE

Because the pixels are lighted in different time, the luminance of active pixels may reduce or differ from inactive pixels. Therefore, the residue image will occur. To avoid the residue image, every pixel needs to be lighted up uniformly.