US Micro Products
ENGINEERED DISPLAY SOLUTIONS

PMOLED SPECIFICATION

Part Number	USMP-P19605
Size	1.1"
Resolution	96 x 64
Color	Yellow
Panel Size	29 (W) x 21 (H)
Active Area	23.49 (W) x 15.65 (H)
IC	SSD1325T2R1
Interface	Parallel, SPI

FOR ADDITIONAL INFORMATION
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Issue Date	Approved by (customer use)	Checked by	Prepared by

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REVISION RECORD

REV.	REVISION DESCRIPTION	REV. DATE	REMARK
A01	INITIAL RELEASE	2011. 06. 02	
A02	Modify double sides tape position	2011. 09. 30	Page 21
A03	Add printing line on FPC	2011. 12. 27	Page 21

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1. SCOPE

This specification is to define the general provisions and quality requirements that apply to the supply of display cells manufactured by US Micro Products. This document, together with the Module Ass'y Drawing, is the highest-level specification for this product.

2. WARRANTY

US Micro Products warrants that the products delivered pursuant to this specification (or order) will conform to the agreed specifications for twelve (12) months from the shipping date ("Warranty Period"). US Micro Products is obligated to repair or replace the products which are found to be defective or inconsistent with the specifications during the Warranty Period without charge, on condition that the products are stored or used as the conditions specified in the specifications. Nevertheless, US Micro Products is not obligated to repair or replace the products without charge if the defects or inconsistency are caused by the force majeure or the reckless behaviors of the customer.
After the Warranty Period, all repairs or replacements of the products are subject to charge.

3. FEATURES

- Small molecular organic light emitting diode.
- Color : Yellow.
- Panel matrix : 96*64.
- Driver IC : SSD1325.
- Excellent quick response time.
- Extremely thin thickness for best mechanism design : 1.61mm.
- High contrast : 2000:1.
- Wide viewing angle : 160°.
- 8-bit 6800-series parallel interface, 8-bit 8080-series parallel interface, serial peripheral interface.
- Wide range of operating temperature : -40 to 70 ℃.
- Anti-glare polarizer.

4. MECHANICAL DATA

NO	ITEM	SPECIFICATION	UNIT
1	Dot Matrix	96 (W) x 64 (H)	dot
2	Dot Size	0.215 (W) x 0.215 (H)	mm^2
3	Dot Pitch	0.245 (W) x 0.245 (H)	mm^2
4	Aperture Rate	77	%
5	Active Area	23.49 (W) x 15.65 (H)	mm^2
6	Panel Size	29 (W) x 21 (H)	mm^2
7*	Panel Thickness	1.42 ± 0.1	mm
8	Module Size	29 (W) x 67.7 (H) x 2.41 (D)	mm^3
9	Diagonal A/A size	1.1	inch
10	Module Weight	2.36 ± 10%	gram

* Panel thickness includes substrate glass, cover glass and UV glue thickness.

5. MAXIMUM RATINGS

ITEM	MIN	MAX	UNIT	Condition	Remark
Supply Voltage (V_{DD})	-0.3	3.5	V	Ta = 25℃	IC maximum rating
Supply Voltage (Vcc)	8	16	V	Ta = 25℃	IC maximum rating
Operating Temp.	-40	70	℃		
Storage Temp	-40	85	℃		
Humidity	-	85	%		
Life Time	33,000	-	Hrs	120 cd/m^2, 50% checkerboard	Note (1)
Life Time	40,000	-	Hrs	100 cd/m^2, 50% checkerboard	Note (2)
Life Time	50,000	-	Hrs	80 cd/m^2, 50% checkerboard	Note (3)

Note:

(A) Under Vcc = 12V, Ta = 25℃, 50% RH.

(B) Life time is defined the amount of time when the luminance has decayed to less than 50% of the initial measured luminance.

(1) Setting of 120 cd/m^2 :

- Contrast setting : 0x6D
- Frame rate : 105Hz
- Duty setting : 1/64

(2) Setting of 100 cd/m^2 :

- Contrast setting : 0x51
- Frame rate : 105Hz
- Duty setting : 1/64

(3) Setting of 80 cd/m^2 :

- Contrast setting : 0x40
- Frame rate : 105Hz
- Duty setting : 1/64

6. ELECTRICAL CHARACTERISTICS

6.1 D.C ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETERS	TEST CONDITION	MIN	TYP	MAX	UNIT
V_{CC}	Analog power supply (for OLED panel)	Ta=-20 °C to +70°C	11.5	12	12.5	V
V_{DD}	Digital power supply	Ta=-20 °C to +70°C	2.4	2.7	3.5	V
I_{DD}	Operating current for V_{DD} V_{DD} = 2.7V, V_{CC} = 12V, IREF = 10uA No panel attached, All Display ON	Contrast=7F	-	-	650	uA
I_{CC}	Operating current for V_{CC} V_{DD} = 2.7V, V_{CC} = 12V, IREF = 10uA No panel attached, All Display ON	Contrast=7F	-	700	-	uA
V_{IH}	Hi logic input level		0.8* V_{DD}	-	V_{DD}	V
V_{IL}	Low logic input level		0	-	0.2* V_{DD}	V
V_{OH}	Hi logic output level		0.9* V_{DD}	-	V_{DD}	V
V_{OL}	Low logic output level		0	-	0.1* V_{DD}	V
I_{SEG}	Segment on output current V_{DD}=2.7V, V_{CC}=12V, IREF=10uA, Display on.	Contrast=7F	270	300	370	uA
		Contrast=5F	-	225	-	uA
		Contrast=3F	-	150	-	uA
		Contrast=1F	-	75	-	uA

Note 1: V_{DD}=2.7V；V_{CC}=12V；Frame rate=105Hz；No panel attached.

Note 2: The Vcc input must keep in a stable value; ripple and noise are not allowed.

6.2 ELECTRO-OPTICAL CHARATERISTICS

PANEL ELECTRICAL SPECIFICATIONS

PARAMETER	MIN	TYP.	MAX	UNITS	COMMENTS
Normal mode current		10	12	mA	All pixels on (1)
Standby mode current		1	2	mA	Standby mode 10% pixels on (2)
Normal mode power consumption		120	144	mW	All pixels on (1)
Standby mode power consumption		12	24	mW	Standby mode 10% pixels on (2)
Normal Luminance	80	100		cd/m^2	Display Average
Standby Luminance		20		cd/m^2	Display Average
CIEx (Yellow)	0.43	0.47	0.51		x, y (CIE 1931)
CIEy (Yellow)	0.45	0.49	0.53		
Dark Room Contrast	2000:1				
Viewing Angle	160			degree	
Response Time		10		µs	

(1) Normal mode condition :

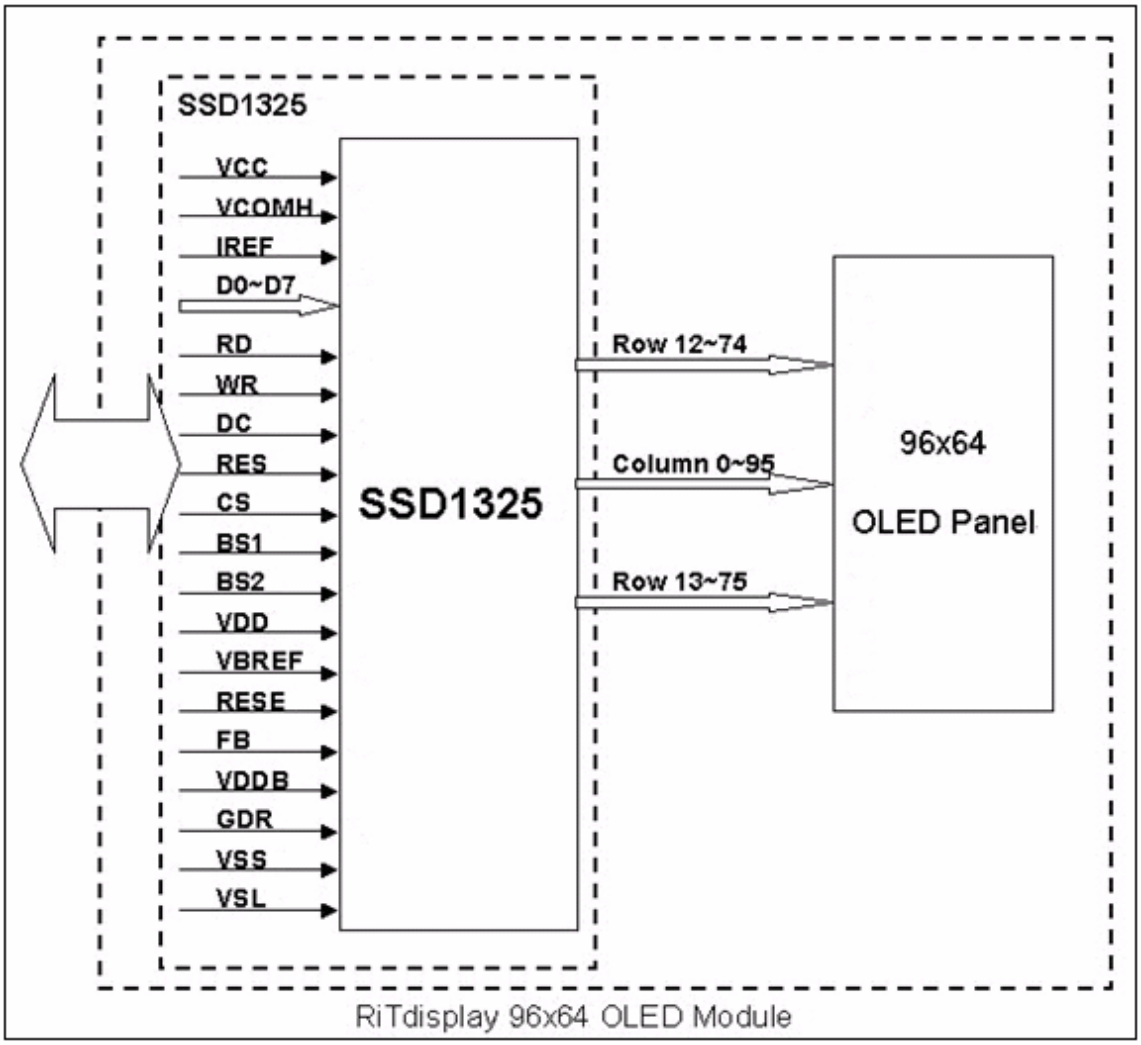
- Driving Voltage : 12V
- Contrast setting : 0x51
- Frame rate : 105Hz
- Duty setting : 1/64

(2) Standby mode condition :

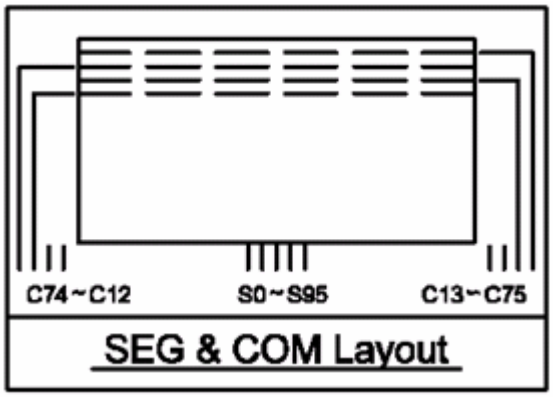
- Driving Voltage : 12V
- Contrast setting : 0x0F
- Frame rate : 105Hz
- Duty setting : 1/64

7. INTERFACE

7.1 FUNCTION BLOCK DIAGRAM



7.2 PANEL LAYOUT DIAGRAM



7.3 PIN ASSIGNMENTS

Pin No.	Pin Name	TYPE	Description
1	NC	-	No connection.
2	VCC	I	Voltage source input for OLED operating.
3	VCOMH	O	A capacitor should be connected between this pin and VSS.
4	IREF	I	A resistor should be connected between this pin and VSS.
5	D7	I/O	Bi-direction data singal.
6	D6		
7	D5		
8	D4		
9	D3		
10	D2		
11	D1		
12	D0		
13	RD	I	Data read operation is initiated when it's pull low.
14	WR	I	Data write operation is initiated when it's pull low.
15	D/C	I	This is Data/Command Control pin. H:Data Input、L:Command Input.
16	RES	I	When the pin is LOW, initialization of the chip is executed.
17	CS	I	This pin is the chip select input.
18	NC	-	No connection.
19	BS2	I	MCU interface selection input.
20	BS1		
21	VDD	I	Voltage Power supply for logic.
22	NC	-	No connection.
23	NC	-	No connection.
24	VBREF	I	This is an internal voltage reference pin. It should be kept NC and left open.
25	RESE	I	This is a reserved pin. It should be kept NC.
26	FB	I	This is a reserved pin. It should be kept NC.
27	VDDB	I	This is a reserved pin. Voltage source input for logic circuit.
28	GDR	I	This is a reserved pin. It should be kept NC.
39	VSS	I	This is a ground pin.
30	VSL	I	This pin can be kept NC or connected with a capacitor to VSS for stability.

7.4 GRAPHIC DISPLAY DATA RAM ADDRESS MAP

The GDDRAM is a bit mapped static RAM holding the bit pattern to be displayed. The size of the RAM is 128x80x4 bits.

Table 11 shows the GDDRAM map under the following condition:

- Command "Set Re-map" A0h is set to:
  - Disable Column Address Re-map (A[0]=0)
  - Disable Nibble Re-map (A[1]=0)
  - Enable Horizontal Address Increment (A[2]=0)
  - Disable COM Re-map (A[4]=0)
- Display Start Line=00h
- Data byte sequence: D0, D1, D2 … D5119

Table 11 : GDDRAM address map 1

		SEG0	SEG1	SEG2	SEG3		SEG124	SEG125	SEG126	SEG127
		00		01			3E		3F	
COM0	00	D0[3:0]	D0[7:4]	D1[3:0]	D1[7:4]		D62[3:0]	D62[7:4]	D63[3:0]	D63[7:4]
COM1	01	D64[3:0]	D64[7:4]	D65[3:0]	D65[7:4]		D126[3:0]	D126[7:4]	D127[3:0]	D127[7:4]
⋮	⋮									
COM78	4E	D4992[3:0]	D4992[7:4]	D4993[3:0]	D4993[7:4]		D5054[3:0]	D5054[7:4]	D5055[3:0]	D5055[7:4]
COM79	4F	D5056[3:0]	D5056[7:4]	D5057[3:0]	D5057[7:4]		D5118[3:0]	D5118[7:4]	D5119[3:0]	D5119[7:4]

SEG Outputs
Column Address
(HEX)

COM Outputs
Row Address (HEX)
(Display Startline=0)

Nibble re-map A[1]=0

Table 12 shows the GDDRAM map under the following condition:

- Command "Set Re-map" A0h is set to:
  - Disable Column Address Re-map (A[0]=0)
  - Disable Nibble Re-map (A[1]=0)
  - Enable Vertical Address Increment (A[2]=1)
  - Disable COM Re-map (A[4]=0)
- Display Start Line=00h
- Data byte sequence: D0, D1, D2 … D5119

Table 12 : GDDRAM address map 2

		SEG0	SEG1	SEG2	SEG3		SEG124	SEG125	SEG126	SEG127
		00		01			3E		3F	
COM0	00	D0[3:0]	D0[7:4]	D80[3:0]	D80[7:4]		D4960[3:0]	D4960[7:4]	D5040[3:0]	D5040[7:4]
COM1	01	D1[3:0]	D1[7:4]	D81[3:0]	D81[7:4]		D4961[3:0]	D4961[7:4]	D5041[3:0]	D5041[7:4]
⋮	⋮									
COM78	4E	D78[3:0]	D78[7:4]	D158[3:0]	D158[7:4]		D5038[3:0]	D5038[7:4]	D5118[3:0]	D5118[7:4]
COM79	4F	D79[3:0]	D79[7:4]	D159[3:0]	D159[7:4]		D5039[3:0]	D5039[7:4]	D5119[3:0]	D5119[7:4]

SEG Outputs
Column Address
(HEX)

COM Outputs
Row Address (HEX)
(Display Startline=0)

Nibble re-map A[1]=0

Table 13 shows the GDDRAM map under the following condition:

- Command "Set Re-map" A0h is set to:
  - Enable Column Address Re-map (A[0]=1)
  - Enable Nibble Re-map (A[1]=1)
  - Enable Horizontal Address Increment (A[2]=0)
  - Disable COM Re-map (A[4]=0)
- Display Start Line=00h
- Data byte sequence: D0, D1, D2 … D5119

Table 13 : GDDRAM address map 3

		SEG0	SEG1	SEG2	SEG3		SEG124	SEG125	SEG126	SEG127
		3F		3E			01		00	
COM0	00	D63[7:4]	D63[3:0]	D62[7:4]	D62[3:0]		D1[7:4]	D1[3:0]	D0[7:4]	D0[3:0]
COM1	01	D127[7:4]	D127[3:0]	D126[7:4]	D126[3:0]		D65[7:4]	D65[3:0]	D64[7:4]	D64[3:0]
⋮	⋮									
COM78	4E	D5055[7:4]	D5055[3:0]	D5054[7:4]	D5054[3:0]		D4993[7:4]	D4993[3:0]	D4992[7:4]	D4992[3:0]
COM79	4F	D5119[7:4]	D5119[3:0]	D5118[7:4]	D5118[3:0]		D5057[7:4]	D5057[3:0]	D5056[7:4]	D5056[3:0]

SEG Outputs Column Address (HEX)

COM Outputs | Row Address (HEX)

(Display Startline=0)

Nibble re-map A[1]=1

For vertical scrolling of the display, an internal register storing display start line can be set to control the portion of the RAM data to be mapped to the display.

Table 14 shows the example in which the display start line register is set to 10h with the following condition:

- Command "Set Re-map" A0h is set to:
  - Disable Column Address Re-map (A[0]=0)
  - Disable Nibble Re-map (A[1]=0)
  - Enable Horizontal Address Increment (A[2]=0)
  - Enable COM Re-map (A[4]=1)
- Display Start Line=10h (corresponds to COM15)
- Data byte sequence: D0, D1, D2 … D5119

Table 14 : GDDRAM address map 4

		SEG0	SEG1	SEG2	SEG3		SEG124	SEG125	SEG126	SEG127
		00		01			3E		3F	
COM15	0F	D0[3:0]	D0[7:4]	D1[3:0]	D1[7:4]		D62[3:0]	D62[7:4]	D63[3:0]	D63[7:4]
COM14	0E	D64[3:0]	D64[7:4]	D65[3:0]	D65[7:4]		D126[3:0]	D126[7:4]	D127[3:0]	D127[7:4]
⋮	⋮									
COM17	11	D4992[3:0]	D4992[7:4]	D4993[3:0]	D4993[7:4]		D5054[3:0]	D5054[7:4]	D5055[3:0]	D5055[7:4]
COM16	10	D5056[3:0]	D5056[7:4]	D5057[3:0]	D5057[7:4]		D5118[3:0]	D5118[7:4]	D5119[3:0]	D5119[7:4]

SEG Output Column Addre (HEX)

COM Outputs | Row Address (HEX)

(Display Startline=10H)

Nibble re-map A[1]=0

Table 15 shows the GDDRAM map under the following condition:

- Command "Set Re-map" A0h is set to:
  - Disable Column Address Re-map (A[0]=0)
  - Disable Nibble Re-map (A[1]=0)
  - Enable Horizontal Address Increment (A[2]=0)
  - Disable COM Re-map (A[4]=0)
- Display Start Line=00h
- Column Start Address=01h
- Column End Address=3Eh
- Row Start Address=01h
- Row End Address=4Eh
- Data byte sequence: D0, D1, D2 … D4835

Table 15 : GDDRAM address map 5

		SEG0	SEG1	SEG2	SEG3		SEG124	SEG125	SEG126	SEG127	SEG Ou
		00		01			3E		3F		Column A
COM0	00										(HE)
COM1	01			D0[3:0]	D0[7:4]		D61[3:0]	D61[7:4]			
⋮	⋮										
COM78	4E			D4774[3:0]	D4774[7:4]		D4835[3:0]	D4835[7:4]			
COM79	4F										
COM Outputs (Display Startline=0)	Row Address (HEX)										

Nibble re-map A[1]=0

Note

(1) Please refer to Table 18 for the details of setting command "Set Re-map"A0h.

(2) The "Display Start Line" is set by the command "Set Display Start Line" A1h and please refer to Table 18 for the setting details

(3) The "Column Start/End Address" is set by the command "Set Column Address" 15h and please refer to Table 18 for the setting details

(4) The "Row Start/End Address" is set by the command "Set Row Address" 75h and please refer to Table 18 for the setting detail

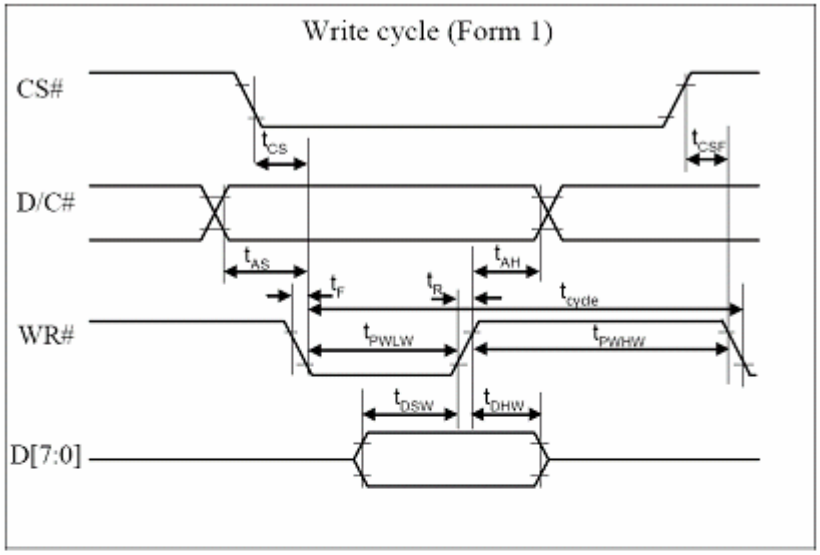
7.5 INTERFACE TIMING CHART

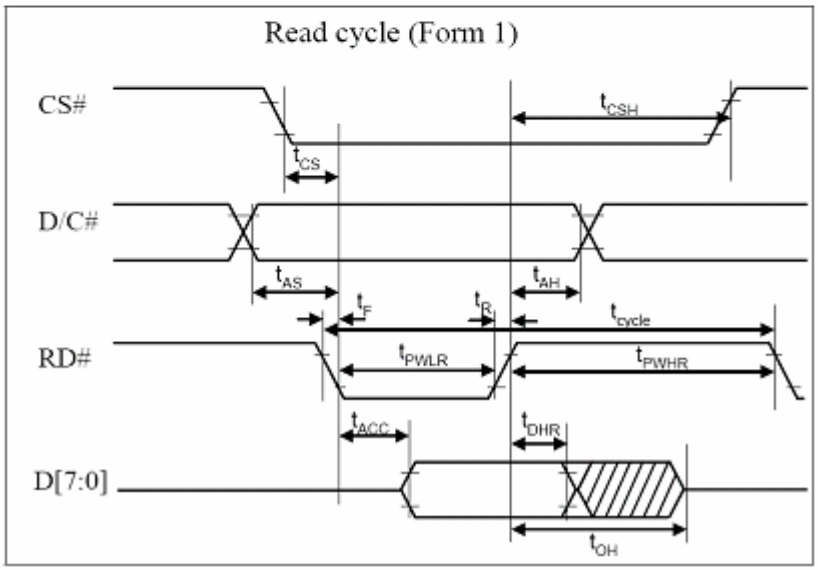
8080-Series MPU Parallel Interface Timing Characteristics

(V_{DD} - V_{SS} = 2.4 to 3.5V, T_A = 25°C)

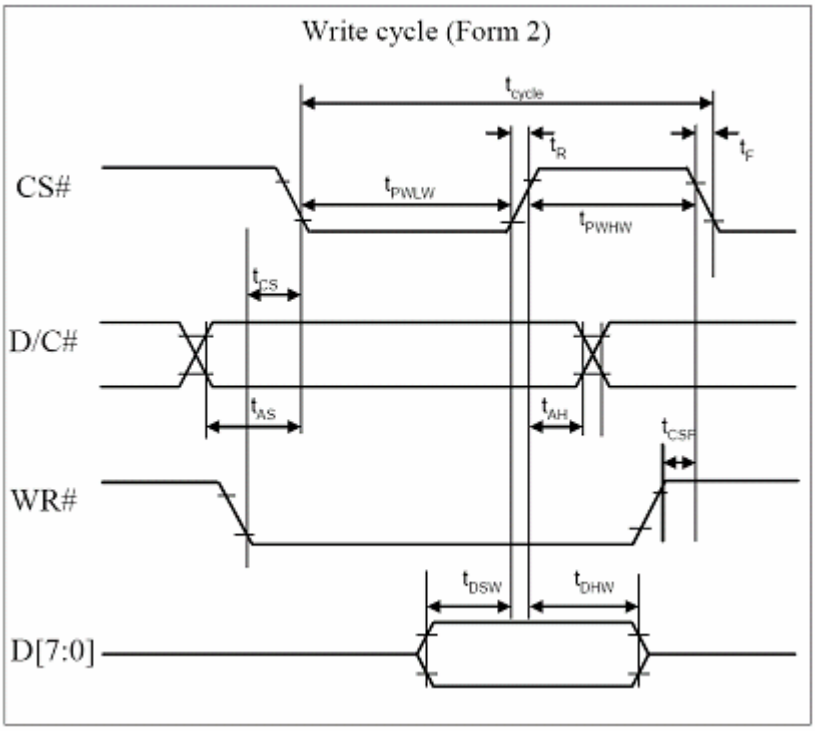
Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time	300	-	-	ns
t_{AS}	Address Setup Time	10	-	-	ns
t_{AH}	Address Hold Time	0	-	-	ns
t_{DSW}	Write Data Setup Time	40	-	-	ns
t_{DHW}	Write Data Hold Time	15	-	-	ns
t_{DHR}	Read Data Hold Time	20	-	-	ns
t_{OH}	Output Disable Time	-	-	70	ns
t_{ACC}	Access Time	-	-	140	ns
t_{PWLR}	Read Low Time	120	-	-	ns
t_{PWLW}	Write Low Time	60	-	-	ns
t_{PWHR}	Read High Time	60	-	-	ns
t_{PWHW}	Write High Time	60	-	-	ns
t_R	Rise Time	-	-	15	ns
t_F	Fall Time	-	-	15	ns
t_{CS}	Chip select setup time	0	-	-	ns
t_{CSH}	Chip select hold time to read signal	0	-	-	ns
t_{CSF}	Chip select hold time	20	-	-	ns

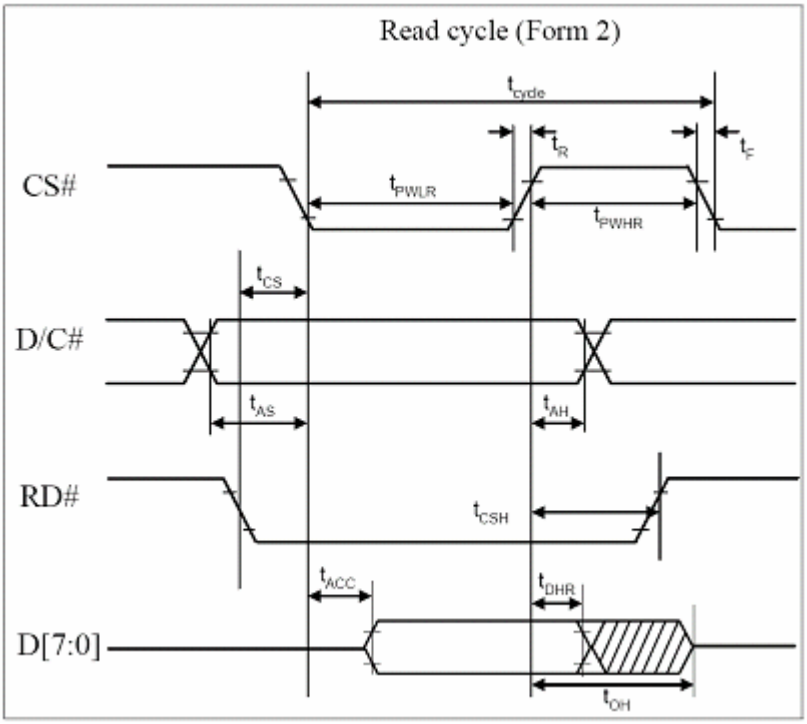
8080-series parallel interface characteristics (Form 1)





8080-series parallel interface characteristics (Form2)



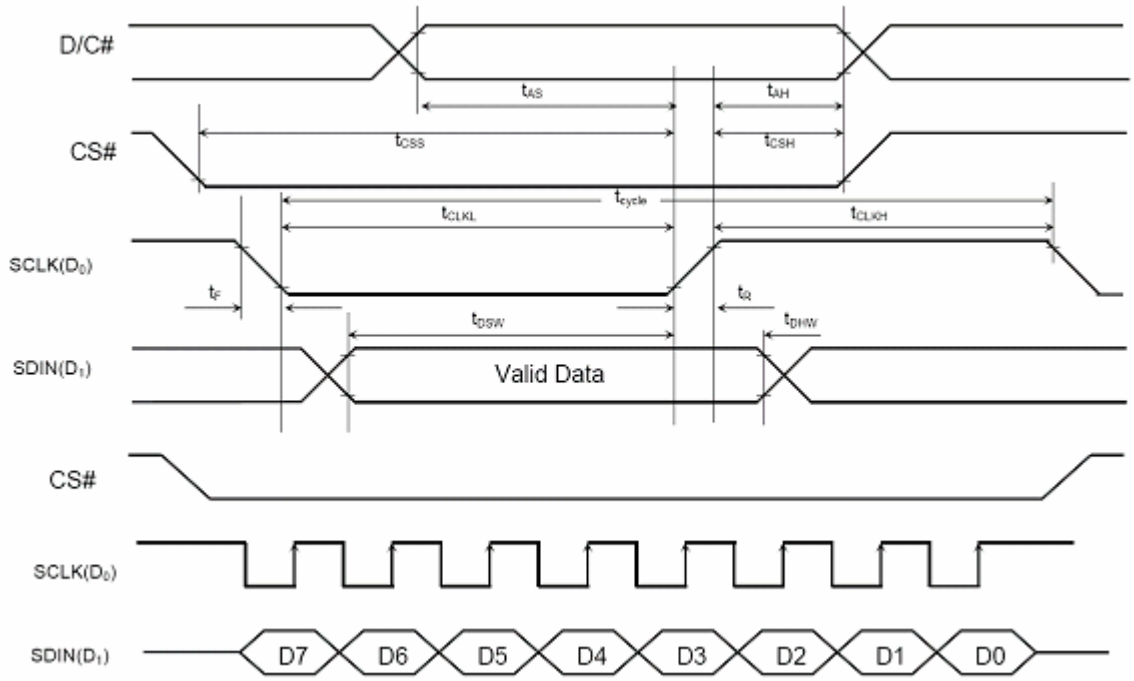


Serial Interface Timing Characteristics

(V_{DD} - V_{SS} = 2.4 to 3.5V, T_A = 25°C)

Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time	250	-	-	ns
t_{AS}	Address Setup Time	150	-	-	ns
t_{AH}	Address Hold Time	150	-	-	ns
t_{CSS}	Chip Select Setup Time	120	-	-	ns
t_{CSH}	Chip Select Hold Time	60	-	-	ns
t_{DSW}	Write Data Setup Time	100	-	-	ns
t_{DHW}	Write Data Hold Time	100	-	-	ns
t_{CLKL}	Clock Low Time	100	-	-	ns
t_{CLKH}	Clock High Time	100	-	-	ns
t_R	Rise Time	-	-	15	ns
t_F	Fall Time	-	-	15	ns

Serial Interface Characteristics

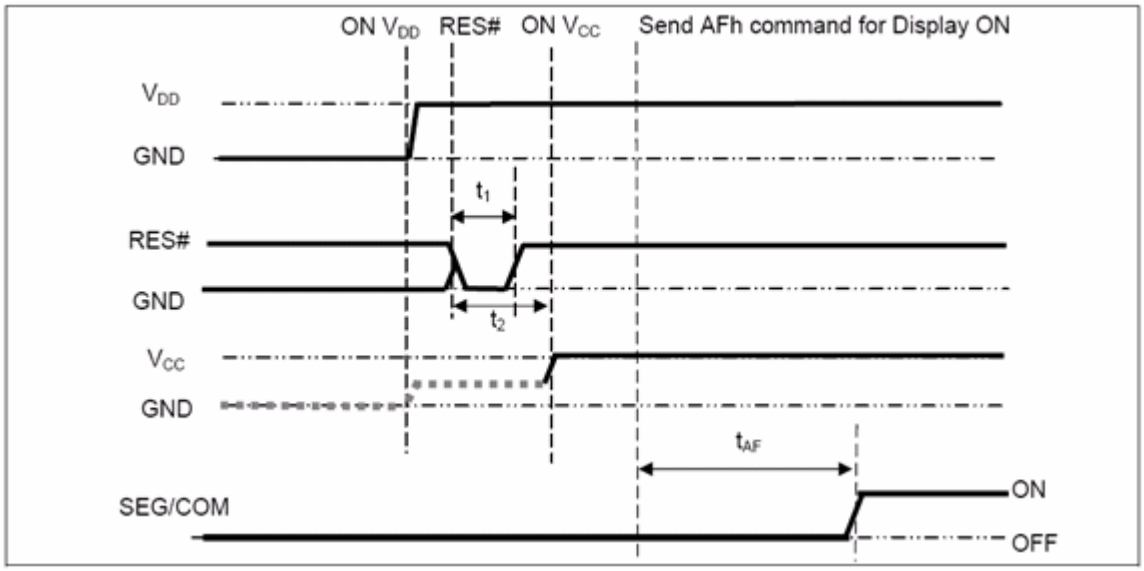


8. POWER ON / OFF SEQUENCE & APPLICATION CIRCUIT

8.1 POWER ON / OFF SEQUENCE

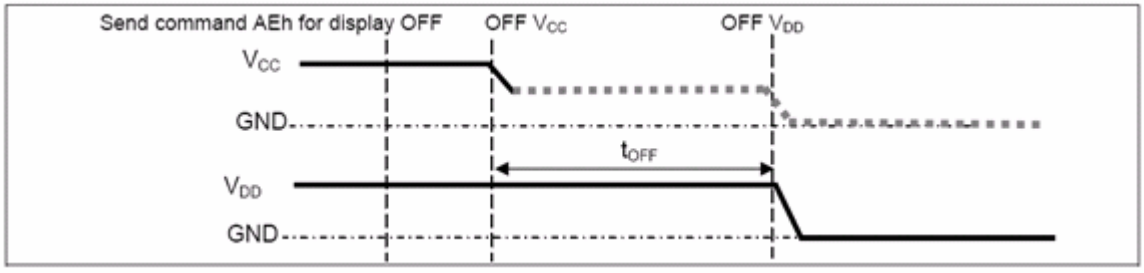
***Power ON sequence**:*

1. Power ON V_{DD}.
2. After V_{DD} become stable, set RES# pin LOW (logic low) for at least 3us(t_1) and then HIGH (logic high).
3. After set RES# pin LOW (logic low), wait for at least 3us(t_2).Then power ON V_{CC}.(1)
4. After V_{CC} become stable, send command AFh for display ON. SEG/COM will be ON after 100ms(t_{AF}).



Power OFF sequence:

1. Send command AEh for display OFF.
2. Wait until panel discharges completely.
3. Power OFF V_{CC}. (1), (2)
4. Wait for t_{OFF}. power OFF V_{DD}. (where minimum t_{OFF}=80ms, typical t_{OFF}=100ms)

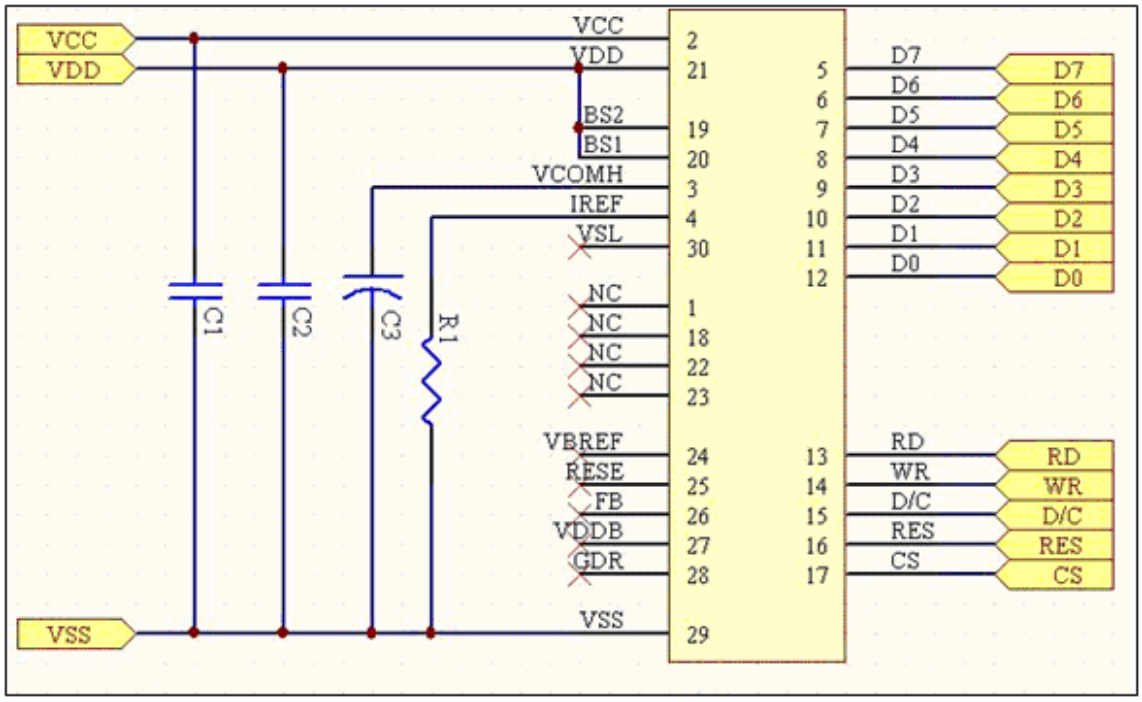


Note:

(1) Since an ESD protection circuit is connected between V_{DD} and V_{CC}, V_{CC} becomes lower than V_{DD} whenever V_{DD} is ON and V_{CC} is OFF as shown in the dotted line of V_{CC} in above figures.

(2) V_{CC} should be disabled when it is OFF.

8.2 APPLICATION CIRCUIT



Recommend components:

C1: 4.7uF/16V (0805).

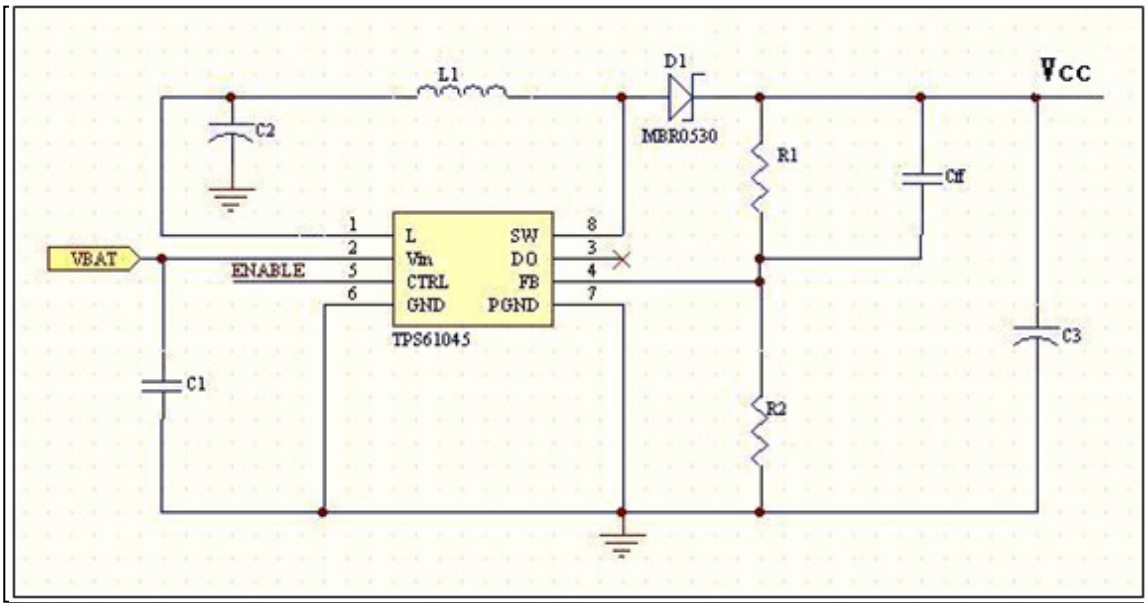
C2: 0.1uF/16V (0603).

C3: 4.7uF/25V (Tantalum type),or Solid Tantalum 4.7uF/ 25V/ A Case (Vishay 572D).

R1: 1M ohm(0603) ,1%.

This circuit is designed for 8080 8-bits interface.

EXTERNAL DC-DC APPLICATION CIRCUIT



Recommended components

C1: 100nF(0603) / 25V, C2 : 4.7uF (Tantalum type) /25V.

C3 : 4.7uF (Tantalum type) / 25V.

Cff : 22pF(0603) / 16V.

D1: Schotty Diode.

L1: 10uH.

R1: 2M ohm (0603),1%, R2: 232K ohm (0603),1%.

VBAT = 1.8V ~ 6.0V(The detail application, please refer the IC data sheet).

8.3 COMMAND TABLE

Refer to SSD1325 IC Spec.

9. RELIABILITY TEST CONDITIONS

No.	Items	Specification	Quantity
1	High temp. (Non-operation)	85℃, 240hrs	5
2	High temp. (Operation)	70℃, 120hrs	5
3	Low temp. (Operation)	-40℃, 120hrs	5
4	High temp. / High humidity (Operation)	65℃, 90%RH, 120hrs	5
5	Thermal shock (Non-operation)	-40℃ ~85℃ (-40℃ /30min; transit /3min; 85℃ /30min; transit /3min) 1cycle: 66min, 100 cycles	5
6	Vibration	Frequency : 5~50HZ, 0.5G Scan rate : 1 oct/min Time : 2 hrs/axis Test axis : X, Y, Z	1 Carton
7	Drop	Height: 120cm Sequence : 1 angle、3 edges and 6 faces Cycles: 1	1 Carton
8	ESD (Non-operation)	Air discharge model, ±8kV, 10 times	5

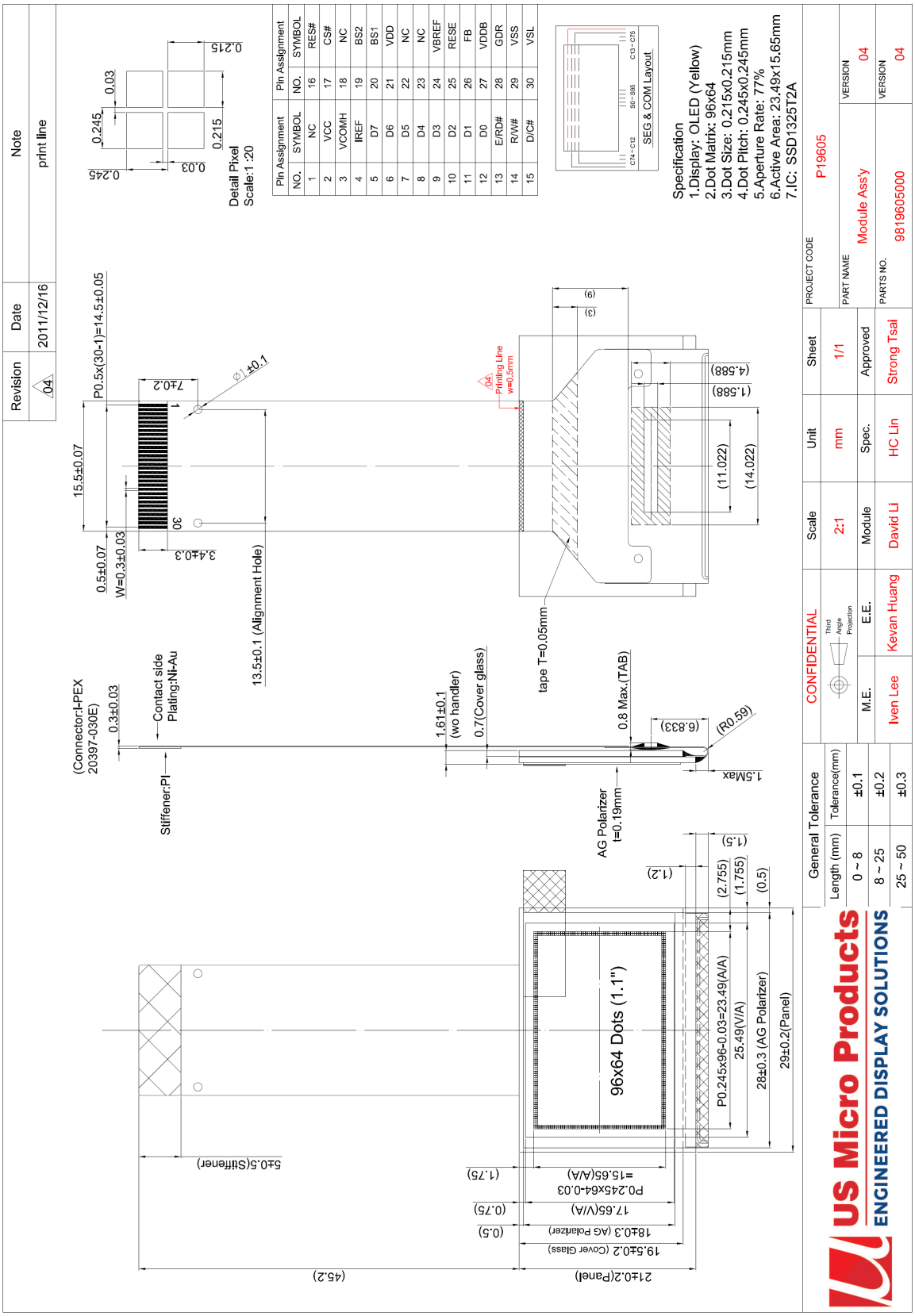
Test and measurement conditions

1. All measurements shall not be started until the specimens attain to temperature stability.
2. All-pixels-on is used as operation test pattern.
3. The degradation of Polarizer are ignored for item 1, 4 & 5.

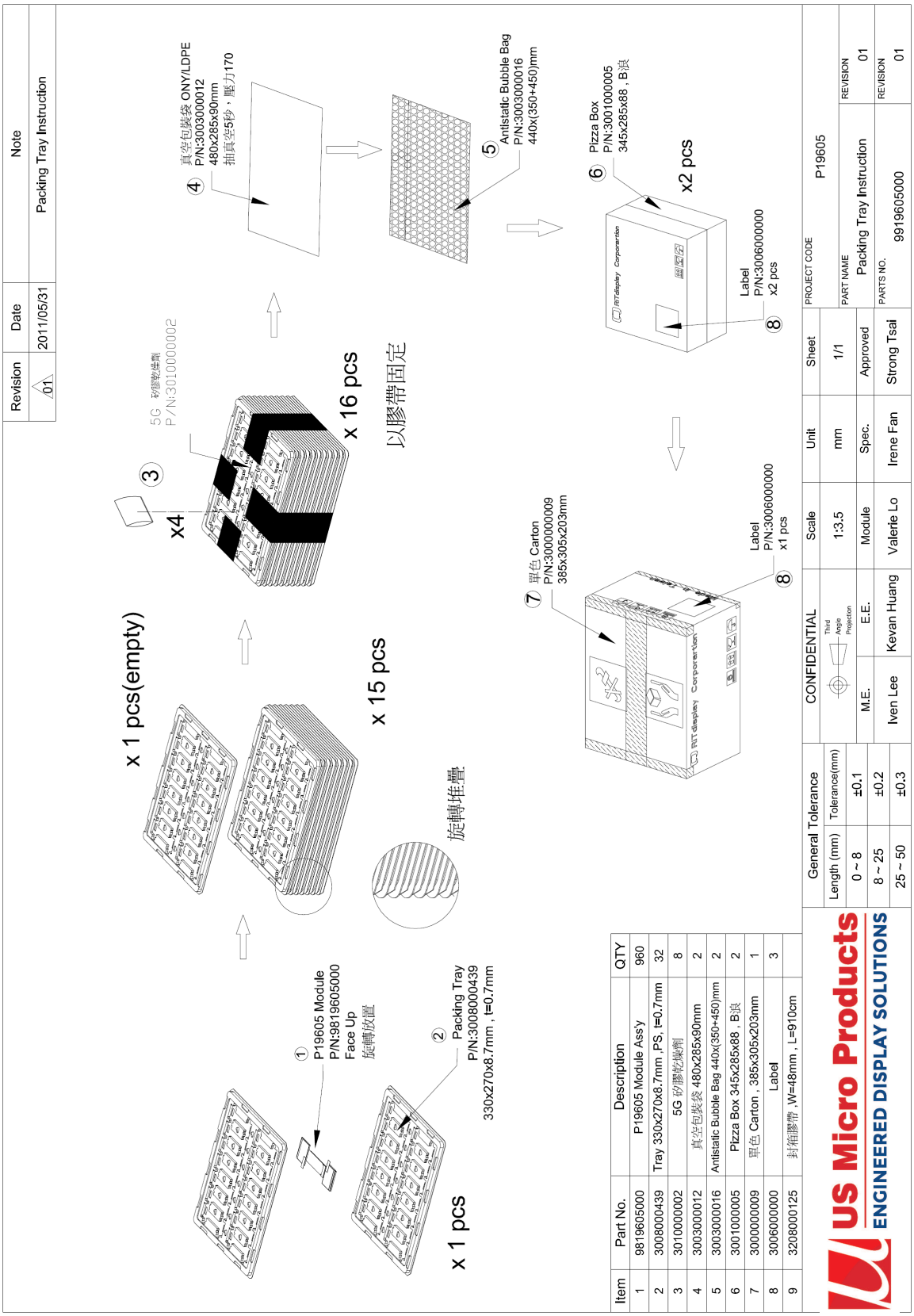
Evaluation criteria

1. The function test is OK.
2. No observable defects.
3. Luminance: > 50% of initial value.
4. Current consumption: within ± 50% of initial value.

10. EXTERNAL DIMENSION



11. PACKING SPECIFICATION



Item	Part No.	Description	QTY
1	9819605000	P19605 Module Ass'y	960
2	3008000439	Tray 330x270x8.7mm ,PS, t=0.7mm	32
3	3010000002	5G 矽膠乾燥劑	8
4	3003000012	真空包裝袋 480x285x90mm	2
5	3003000016	Antistatic Bubble Bag 440x(350+450)mm	2
6	3001000005	Pizza Box 345x285x88 , B浪	2
7	3000000009	單色 Carton , 385x305x203mm	1
8	3006000000	Label	3
9	3208000125	封箱膠帶 ,W=48mm , L=910cm	

12. APPENDIXES

APPENDIX 1: DEFINITIONS

A. DEFINITION OF CHROMATICITY COORDINATE

The chromaticity coordinate is defined as the coordinate value on the CIE 1931 color chart for R, G, B, W.

B. DEFINITION OF CONTRAST RATIO

The contrast ratio is defined as the following formula:

$$\text{Contrast Ratio} = \frac{\text{Luminance of all pixels on measurement}}{\text{Luminance of all pixels off measurement}}$$

C. DEFINITION OF RESPONSE TIME

The definition of turn-on response time Tr is the time interval between a pixel reaching 10% of steady state luminance and 90% of steady state luminance. The definition of turn-off response time Tf is the time interval between a pixel reaching 90% of steady state luminance and 10% of steady state luminance. It is shown in Figure 2.

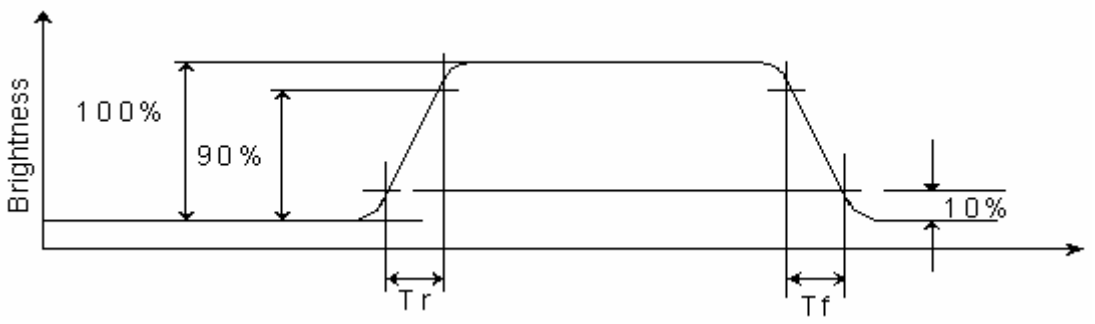


Figure 2: Response time

D. DEFINITION OF VIEWING ANGLE

The viewing angle is defined as Figure 3. Horizontal and vertical (H & V) angles are determined for viewing directions where luminance varies by 50% of the perpendicular value.

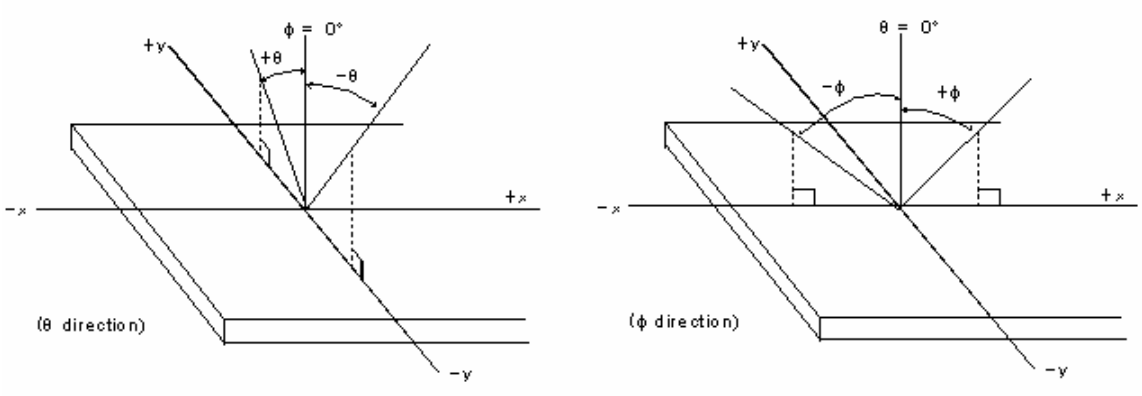
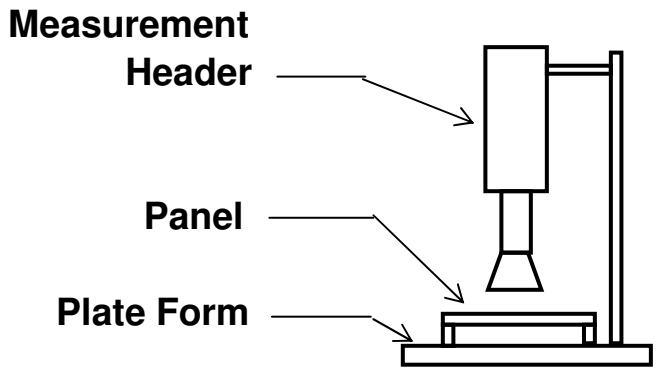


Figure 3: Viewing Angle

APPENDIX 2: MEASUREMENT APPARATUS

A. LUMINANCE/COLOR COORDINATE

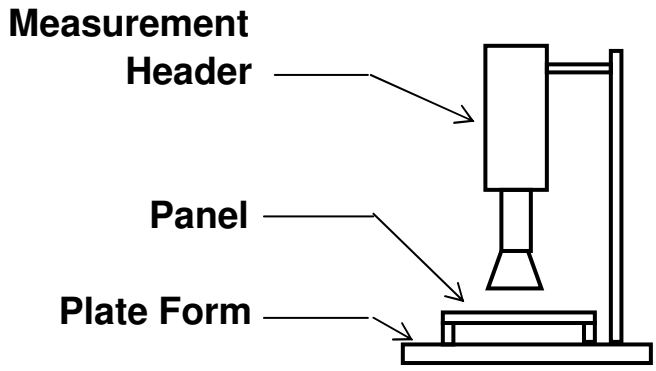
PHOTO RESEARCH PR-705, MINOLTA CS-100



**PR-705 /
MINOLTA CS-100
Color Analyzer**

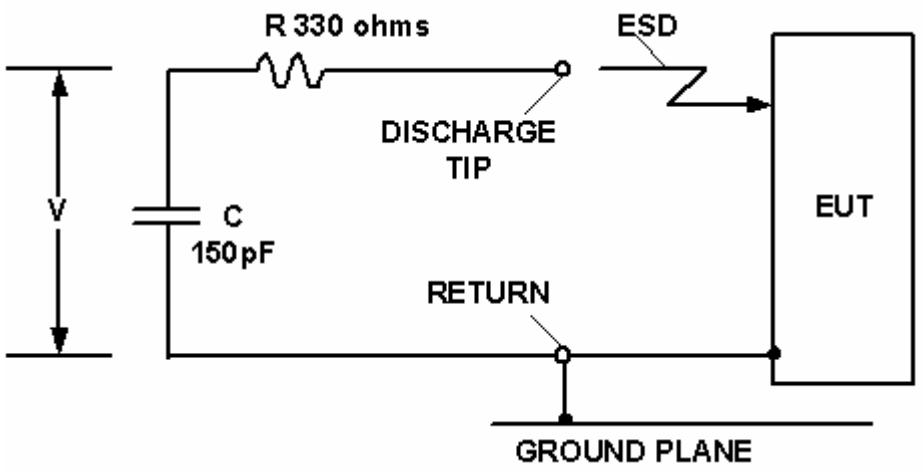
B. CONTRAST / RESPONSE TIME / VIEW ANGLE

WESTAR CORPORATION FPM-510



**Westar FPM-510
Display Contrast /
Response time /
View angle Analyzer**

C. ESD ON AIR DISCHARGE MODE



APPENDIX 3: PRECAUTIONS

A. RESIDUE IMAGE

Because the pixels are lighted in different time, the luminance of active pixels may reduce or differ from inactive pixels. Therefore, the residue image will occur. To avoid the residue image, every pixel needs to be lighted up uniformly.