US Micro Products
ENGINEERED DISPLAY SOLUTIONS

PMOLED SPECIFICATION

Part Number	USMP-P008-096032WBI-A0
Size	0.8"
Resolution	96x32
Color	White
Panel Size	28.5 (W) x 11.5 (H)
Active Area	19.18 (W) x 6.38 (H)
IC	SSD1307
Interface	SPI, I^2C

FOR ADDITIONAL INFORMATION
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Issue Date	Approved by (customer use)	Checked by	Prepared by

REVISION RECORD

REV.	REVISION DESCRIPTION	REV. DATE	REMARK
X01	INITIAL RELEASE	2009. 02. 09	
A01	■ Transfer from X version ■ Modify definition of panel thickness ■ Modify shielding tape ■ Add the packing specification	2009. 04. 02	Page 5, 18 & 19
A02	■ Add module bending diagram	2009. 11. 06	Page 18

CONTENTS

1. SCOPE

The purpose of this specification is to define the general provisions and quality requirements that apply to the supply of display cells manufactured by USMP. This document, together with the Module Assembly Drawing, is the highest-level specification for this product. It describes the product, identifies supporting documents and contains specifications, which are either not addressed, or are exceptions to the supporting documents.

2. WARRANTY

USMP warrants that the products delivered pursuant to this specification (or order) will conform to the agreed specifications for twelve (12) months from the shipping date ("Warranty Period"). USMP is obligated to repair or replace the products which are found to be defective or inconsistent with the specifications during the Warranty Period without charge, on condition that the products are stored or used as the conditions specified in the specifications. Nevertheless, USMP is not obligated to repair or replace the products without charge if the defects or inconsistency are caused by the force majeure or the reckless behaviors of the customer.

After the Warranty Period, all repairs or replacements of the products are subject to charge.

3. FEATURES

- Small molecular organic light emitting diode.
- Color : White
- Panel matrix : 96*32
- Driver IC : SSD1307
- Excellent Quick response time : 10μs
- Extremely thin thickness for best mechanism design : 1.41 mm
- High contrast : 2000:1
- Wide viewing angle : 160°
- SPI (Serial Peripheral Interface), I^2C Interface.
- Strong environmental resistance.
- Wide range of operating temperature : -40 to 70℃
- Anti-glare polarizer.

4. MECHANICAL DATA

NO	ITEM	SPECIFICATION	UNIT
1	Dot Matrix	96 (W) x 32 (H)	dot
2	Dot Size	0.18 (W) x 0.18 (H)	mm^2
3	Dot Pitch	0.20 (W) x 0.20 (H)	mm^2
4	Aperture Rate	81	%
5	Active Area	19.18 (W) x 6.38 (H)	mm^2
6	Panel Size	28.5 (W) x 11.5 (H)	mm^2
7*	Panel Thickness	1.22 ± 0.1	mm
8	Module Size	49.4 (W) x 11.8 (H) x 1.41 (D)	mm^3
9	Diagonal A/A size	0.8	inch
10	Module Weight	0.95 ± 10%	gram

* Panel thickness includes substrate glass, cover glass and UV glue thickness.

5. MAXIMUM RATINGS

ITEM	MIN	MAX	UNIT	Condition	Remark
Supply Voltage (V_{DD})	-0.3	+4	V	Ta = 25 ℃	IC maximum rating
Supply Voltage (Vcc)	7	16	V	Ta = 25 ℃	IC maximum rating
Operating Temp.	-40	70	℃		
Storage Temp	-40	85	℃		
Humidity		85	%		
Life Time	21,000	-	Hrs	140 cd/m^2, 50% checkerboard	Note (1)
Life Time	25,000	-	Hrs	120 cd/m^2, 50% checkerboard	Note (2)
Life Time	30,000	-	Hrs	100 cd/m^2, 50% checkerboard	Note (3)

Note:

(A) Under VCC = 12, Ta = 25℃, 50% RH.

(B) Life time is defined the amount of time when the luminance has decayed to less than 50% of the initial measured luminance.

(1) Setting of 140 cd/m^2 :

- Contrast setting : 0x40
- Frame rate : 105Hz
- Duty setting : 1/32

(2) Setting of 120 cd/m^2 :

- Contrast setting : 0x36
- Frame rate : 105Hz
- Duty setting : 1/32

(3) Setting of 100 cd/m^2 :

- Contrast setting : 0x2C
- Frame rate : 105Hz
- Duty setting : 1/32

6. ELECTRICAL CHARACTERISTICS

6.1 D.C ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETERS	TEST CONDITION	MIN	TYP	MAX	UNIT
V_{CC}	Analog power supply (for OLED panel)	Ta=-20 °C to +70°C	11.5	12	12.5	V
V_{DD}	Digital power supply	Ta=-20 °C to +70°C	1.65	2.8	3.3	V
I_{DD}	Operating current for V_{DD} VDD = 2.8V, VCC = 12V, IREF = 10uA No Panel attached, All Display ON	Contrast=FF	-	23	30	uA
I_{CC}	Operating current for V_{CC} VDD = 2.8V, VCC = 12V, IREF = 10uA No panel attached, All Display ON	Contrast=FF	-	455	590	uA
V_{IH}	High logic input level		0.8* V_{DD}	-	-	V
V_{IL}	Low logic input level		-	-	0.2* V_{DD}	V
V_{OH}	High logic output level	I_{OUT} = 100uA, 3.3MHz	0.9* V_{DD}	-	-	V
V_{OL}	Low logic output level	I_{OUT} = 100uA, 3.3MHz	-	-	0.1* V_{DD}	V
I_{SEG}	Segment on output current V_{DD}=2.8V, V_{CC}=12V, IREF=10uA, Display on,	Contrast=FF	285	316	345	uA
		Contrast=AF	-	217	-	uA
		Contrast=7F	-	158	-	uA
		Contrast=3F	-	78	-	uA
		Contrast=0F	-	19	-	uA

Note : The Vcc input must keep in a stable value; ripple and noise are not allowed.

6.2 ELECTRO-OPTICAL CHARACTERISTICS

PANEL ELECTRICAL SPECIFICATIONS

PARAMETER	MIN	TYP.	MAX	UNITS	COMMENTS
Normal mode current		5	6	mA	All pixels on (1)
Standby mode current		1	1.5	mA	Standby mode 10% pixels on (2)
Normal mode power consumption		60	72	mW	All pixels on (1)
Standby mode power consumption		12	18	mW	Standby mode 10% pixels on (2)
Normal mode Luminance	100	120		cd/m^2	Display Average
Standby mode Luminance		20		cd/m^2	
CIEx (White)	0.24	0.28	0.32		x, y (CIE 1931)
CIEy (White)	0.28	0.32	0.36		
Dark Room Contrast	2000:1				
Viewing Angle	160			degree	
Response Time		10		μs	

(1) Normal mode condition :

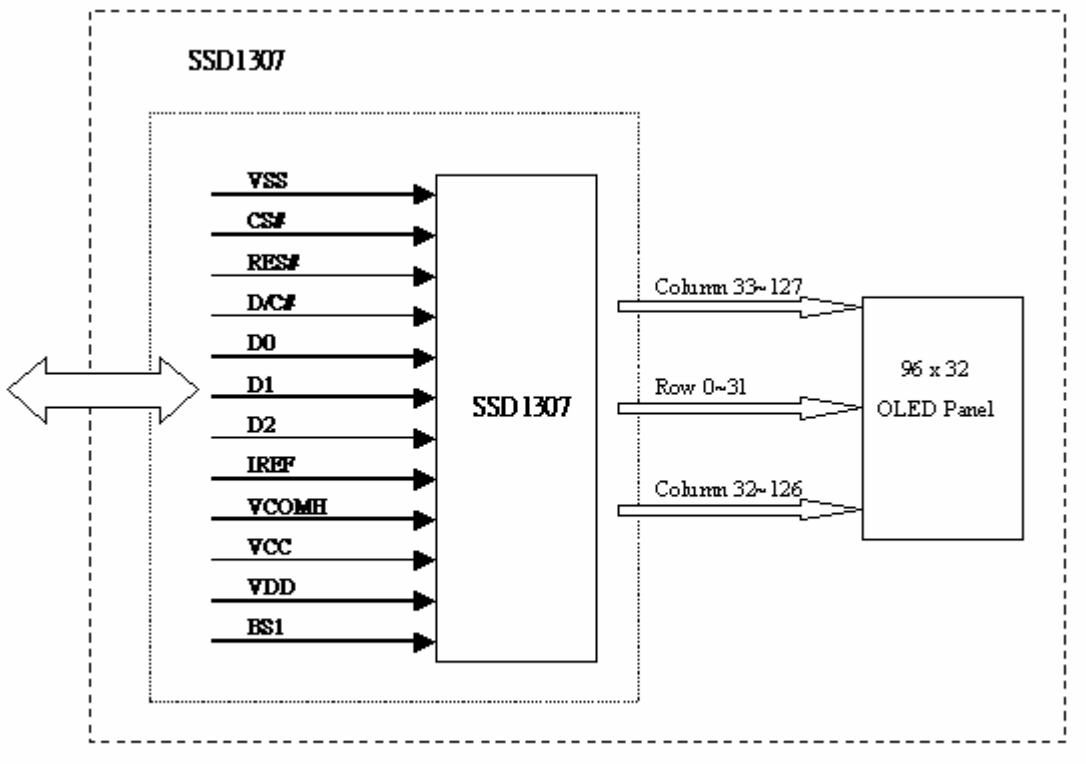
- Driving Voltage : 12
- Contrast setting : 0x36
- Frame rate : 105Hz
- Duty setting : 1/32

(2) Standby mode condition :

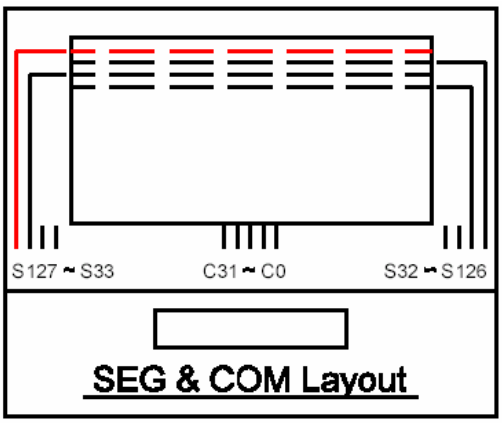
- Driving Voltage : 12
- Contrast setting : 0x00
- Frame rate : 105Hz
- Duty setting : 1/32

7. INTERFACE

7.1 FUNCTION BLOCK DIAGRAM



7.2 PANEL LAYOUT DIAGRAM



7.3 PIN ASSIGNMENTS

Pin No.	Pin Name	Description
1	VSS	This is a ground pin.
2	CS#	This pin is the chip select input.
3	RES#	Hardware reset signal
4	D/C#	In 4-wire Serial mode, this is Data/Command control pin. In I^2C mode, this pin acts as SA0 for slave address selection.
5	D0	4-wire SPI: SCLK I^2C: SCL
6	D1	4-wire SPI: SDIN I^2C: SDAIN
7	D2	4-wire SPI: NC I^2C: SDAOUT
8	IREF	The current reference input pin, this pin should be connected to ground through a resistor.
9	VCOMH	The COM voltage reference pin, this pin should be connected to ground through a capacitor.
10	VCC	Positive OLED high voltage power supply
11	VDD	Power supply for logic circuit
12	BS1	MCU Bus Interface Pin Selection 0: 4-wire Serial Interface 1: I^2C Interface

7.4 GRAPHIC DISPLAY DATA RAM ADDRESS MAP

The GDDRAM is a bit mapped static RAM holding the bit pattern to be displayed. The size of the RAM is 128 x 39 bits and the RAM is divided into five pages, from PAGE0 to PAGE4, which are used for monochrome 128x39 dot matrix display, as shown in below figures.

When one data byte is written into GDDRAM, all the rows image data of the same page of the current column are filled (i.e. the whole column (8 bits) pointed by the column address pointer is filled.). Data bit D0 is written into the top row, while data bit D7 is written into bottom row. For PAGE4, bit D7 is treated as don't care bit.

For mechanical flexibility, re-mapping on both Segment and Common outputs can be selected by software. For vertical shifting of the display, an internal register storing the display start line can be set to control the portion of the RAM data to be mapped to the display (command D3h).

GDDRAM pages structure of SSD1307

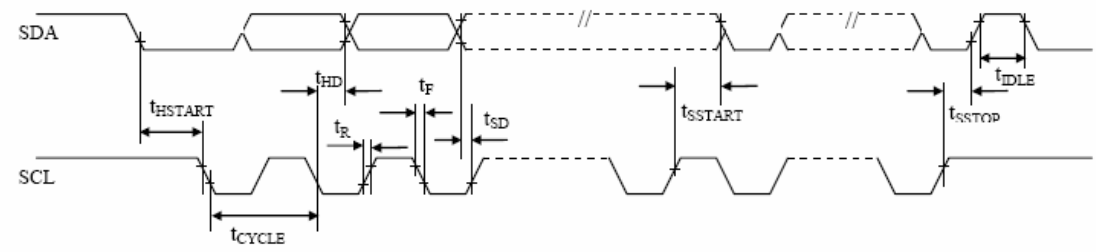
Segment re-mapping (command A1h)		SEG127	SEG126	SEG125	SEG124	.....	SEG4	SEG3	SEG2	SEG1	SEG0		
Segment re-mapping (command A0h [RESET])		SEG0	SEG1	SEG2	SEG3	.....	SEG123	SEG124	SEG125	SEG126	SEG127		
Page	Data	COL0	COL1	COL2	COL3	.....	COL123	COL124	COL125	COL126	COL127	COM Output Scan Direction (command C0h [RESET])	COM Output Scan Direction (command C8h)
0	D0					.....						COM0	COM38
	D1											COM1	COM37
	D2											COM2	COM36
	D3											COM3	COM35
	D4											COM4	COM34
	D5											COM5	COM33
	D6											COM6	COM32
	D7											COM7	COM31
1	D0					.....						COM8	COM30
	D1											COM9	COM29
	D2											COM10	COM28
	D3											COM11	COM27
	D4											COM12	COM26
	D5											COM13	COM25
	D6											COM14	COM24
	D7											COM15	COM23
2	D0					.....						COM16	COM22
	D1											COM17	COM21
	D2											COM18	COM20
	D3											COM19	COM19
	D4											COM20	COM18
	D5											COM21	COM17
	D6											COM22	COM16
	D7											COM23	COM15
3	D0					.....						COM24	COM14
	D1											COM25	COM13
	D2											COM26	COM12
	D3											COM27	COM11
	D4											COM28	COM10
	D5											COM29	COM9
	D6											COM30	COM8
	D7											COM31	COM7
4	D0					.....						COM32	COM6
	D1											COM33	COM5
	D2											COM34	COM4
	D3											COM35	COM3
	D4											COM36	COM2
	D5											COM37	COM1
	D6											COM38	COM0
	D7	Don't care bit											

Each box represents one bit of image data

7.5 INTERFACE TIMING CHART

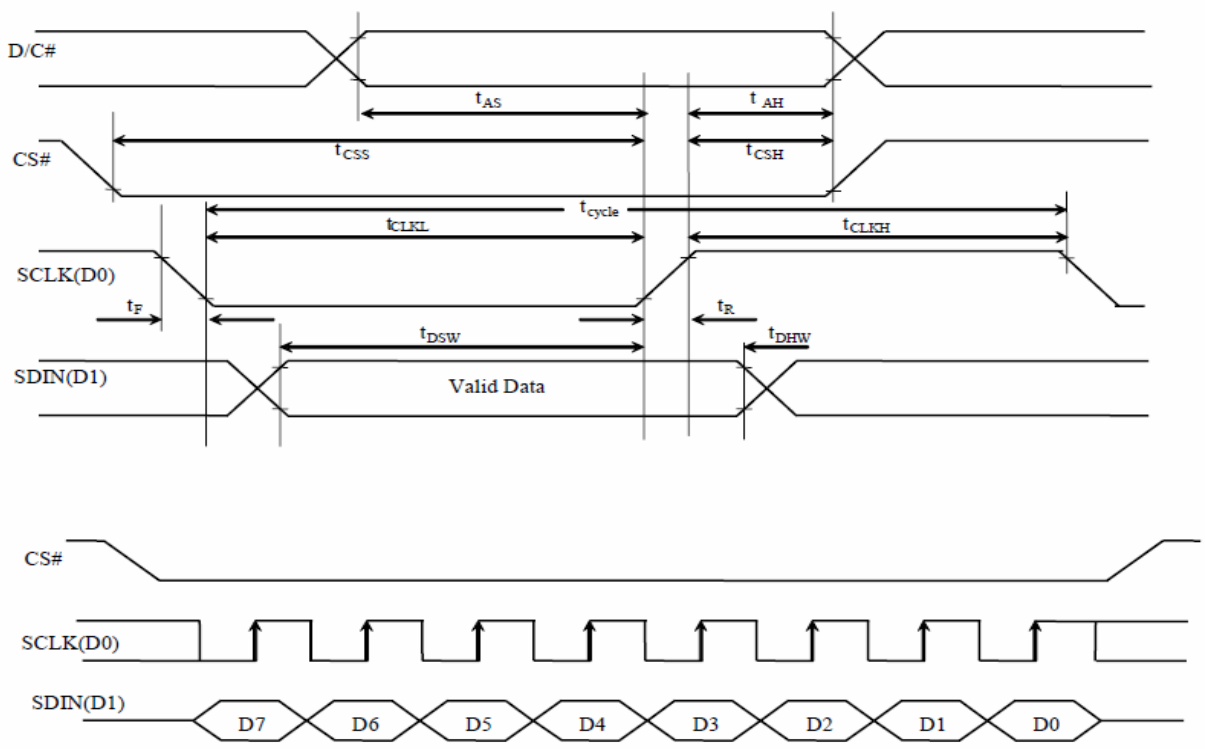
I²C Interface Timing Characteristics

Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time	2.5	-	-	us
t_{HSTART}	Start condition Hold Time	0.6	-	-	us
t_{HD}	Data Hold Time (for "SDA_{OUT}" pin)	0	-	-	ns
	Data Hold Time (for "SDA_{IN}" pin)	300	-	-	ns
t_{SD}	Data Setup Time	100	-	-	ns
t_{SSTART}	Start condition Setup Time (Only relevant for a repeated Start condition)	0.6	-	-	us
t_{SSTOP}	Stop condition Setup Time	0.6	-	-	us
t_R	Rise Time for data and clock pin	-	-	300	ns
t_F	Fall Time for data and clock pin	-	-	300	ns
t_{IDLE}	Idle Time before a new transmission can start	1.3	-	-	us



Serial Interface Timing Characteristics (4-wire SPI)

Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time	100	-	-	ns
t_{AS}	Address Setup Time	15	-	-	ns
t_{AH}	Address Hold Time	15	-	-	ns
t_{CSS}	Chip Select Setup Time	20	-	-	ns
t_{CSH}	Chip Select Hold Time	10	-	-	ns
t_{DSW}	Write Data Setup Time	15	-	-	ns
t_{DHW}	Write Data Hold Time	15	-	-	ns
t_{CLKL}	Clock Low Time	20	-	-	ns
t_{CLKH}	Clock High Time	20	-	-	ns
t_R	Rise Time	-	-	40	ns
t_F	Fall Time	-	-	40	ns



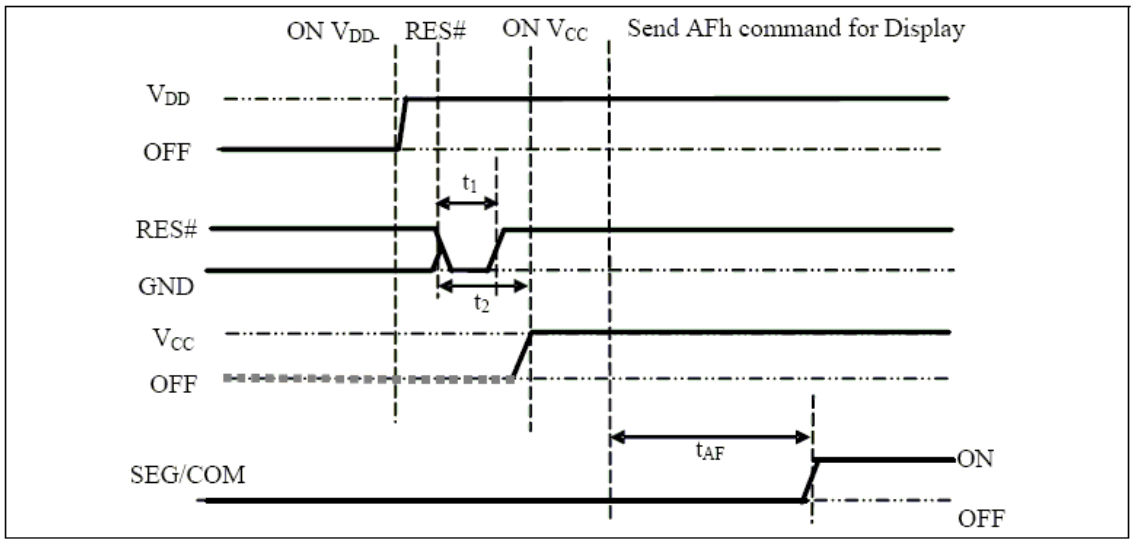
8. POWER ON / OFF SEQUENCE & APPLICATION CIRCUIT

8.1 POWER ON / OFF SEQUENCE

***Power ON sequence*:**

1. Power ON V_{DD}
2. After V_{DD} become stable, set RES# pin LOW (logic low) for at least 3us (t_1) [3] and then HIGH (logic high).
3. After set RES# pin LOW (logic low), wait for at least 3us (t_2). Then Power ON V_{CC}. [1]
4. After V_{CC} become stable, send command AFh for display ON. SEG/COM will be ON after 100ms (t_{AF}).

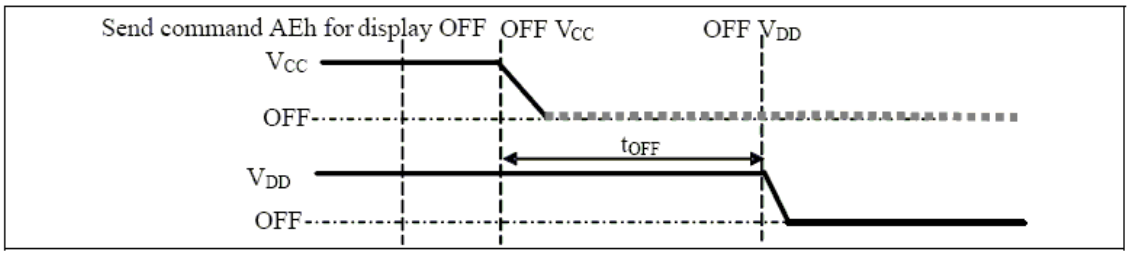
The Power ON sequence



***Power OFF sequence*:**

1. Send command AEh for display OFF.
2. Power OFF V_{CC} [1], [2]
3. Power OFF V_{DD} after t_{OFF}.[4] (where Minimum t_{OFF}=80ms, Typical t_{OFF}=100ms)

The Power OFF sequence



Note:

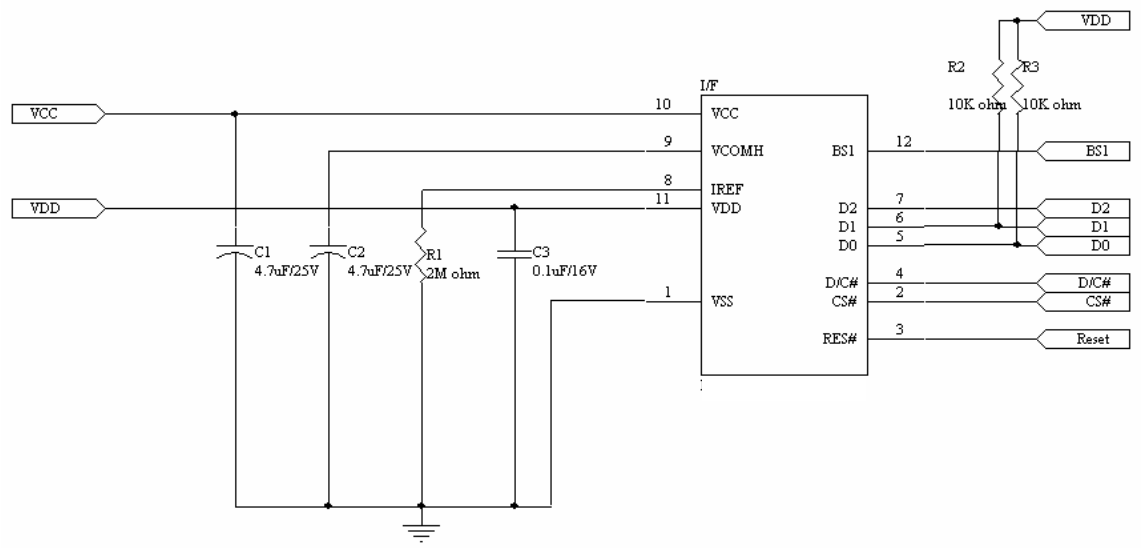
[1] V_{CC} should be disabled when it is OFF.

[2] Power Pins (V_{DD}, V_{CC}) can never be pulled to ground under any circumstance.

[3] The register values are reset after t_1.

[4] V_{DD} should not be Power OFF before V_{CC} Power OFF.

8.2 APPLICATION CIRCUIT



Component：

C1、C2：4.7uF/16V(0805)

C3：0.1uF/16V(0603)

R1：2M ohm 1%(0603)

R2、R3：10K ohm (0603)

This circuit is for I^2C Interface

8.3 COMMAND TABLE

Refer to SSD1307 IC Spec.

9. RELIABILITY TEST CONDITIONS

No.	Items	Specification	Quantity
1	High temp. (Non-operation)	85℃, 240hrs	5
2	High temp. (Operation)	70℃, 120hrs	5
3	Low temp. (Operation)	-40℃, 120hrs	5
4	High temp. / High humidity (Operation)	65℃, 90%RH, 120hrs	5
5	Thermal shock (Non-operation)	-40℃ ~85℃ (-40℃ /30min; transit /3min; 85℃ /30min; transit /3min) 1cycle: 66min, 100 cycles	5
6	Vibration	Frequency : 5~50HZ, 0.5G Scan rate : 1 oct/min Time : 2 hrs/axis Test axis : X, Y, Z	1 Carton
7	Drop	Height: 120cm Sequence : 1 angle、3 edges and 6 faces Cycles: 1	1 Carton
8	ESD (Non-operation)	Air discharge model, ±8kV, 10 times	5

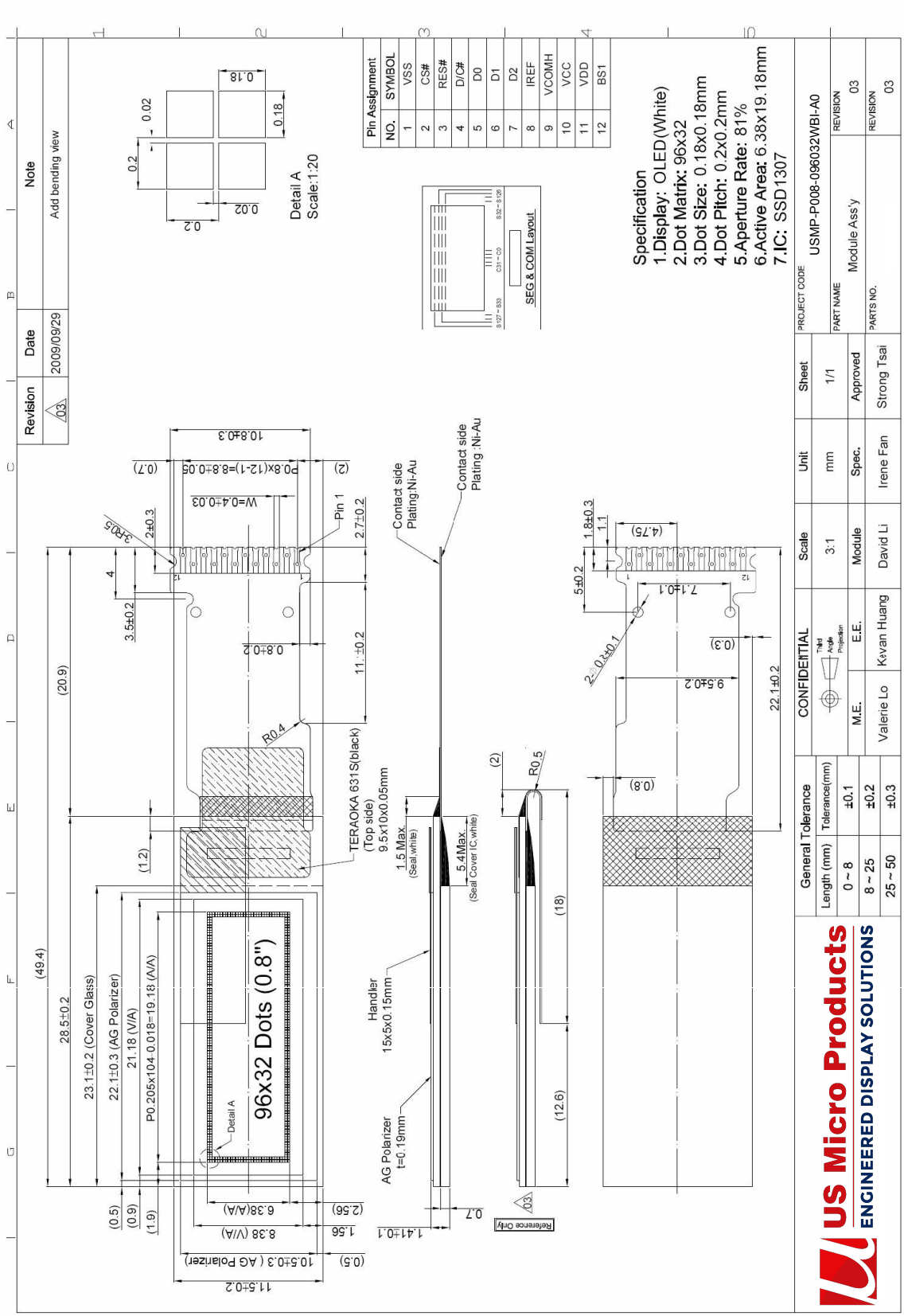
Test and measurement conditions

1. All measurements shall not be started until the specimens attain to temperature stability.
2. All-pixels-on is used as operation test pattern.
3. The degradation of Polarizer are ignored for item 1, 4 & 5.

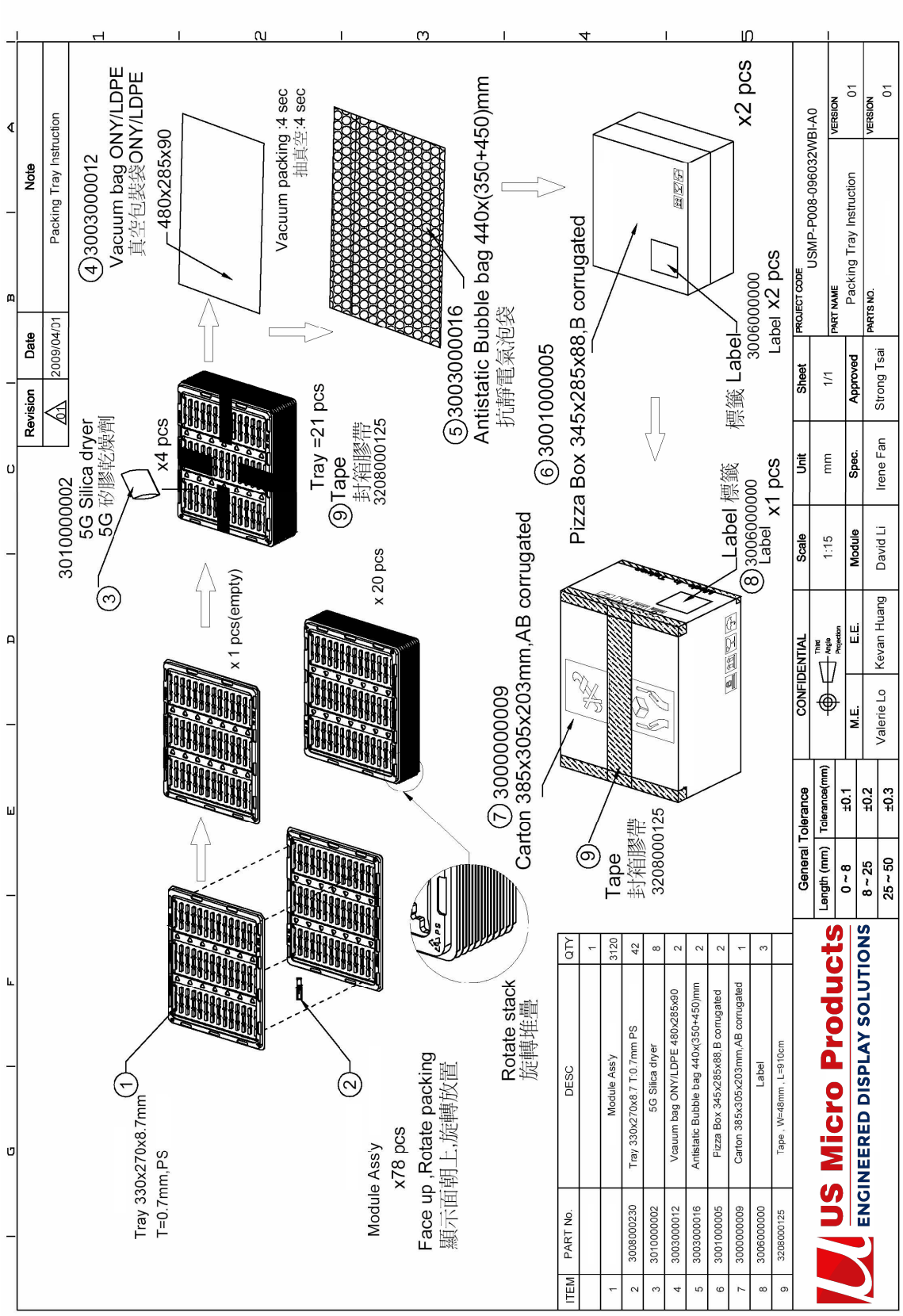
Evaluation criteria

1. The function test is OK.
2. No observable defects.
3. Luminance: > 50% of initial value.
4. Current consumption: within ± 50% of initial value.

10. EXTERNAL DIMENSION



11. PACKING SPECIFICATION



12. APPENDIXES

APPENDIX 1: DEFINITIONS

A. DEFINITION OF CHROMATICITY COORDINATE

The chromaticity coordinate is defined as the coordinate value on the CIE 1931 color chart for R, G, B, W.

B. DEFINITION OF CONTRAST RATIO

The contrast ratio is defined as the following formula:

$$\text{Contrast Ratio} = \frac{\text{Luminance of all pixels on measurement}}{\text{Luminance of all pixels off measurement}}$$

C. DEFINITION OF RESPONSE TIME

The definition of turn-on response time Tr is the time interval between a pixel reaching 10% of steady state luminance and 90% of steady state luminance. The definition of turn-off response time Tf is the time interval between a pixel reaching 90% of steady state luminance and 10% of steady state luminance. It is shown in Figure 2.

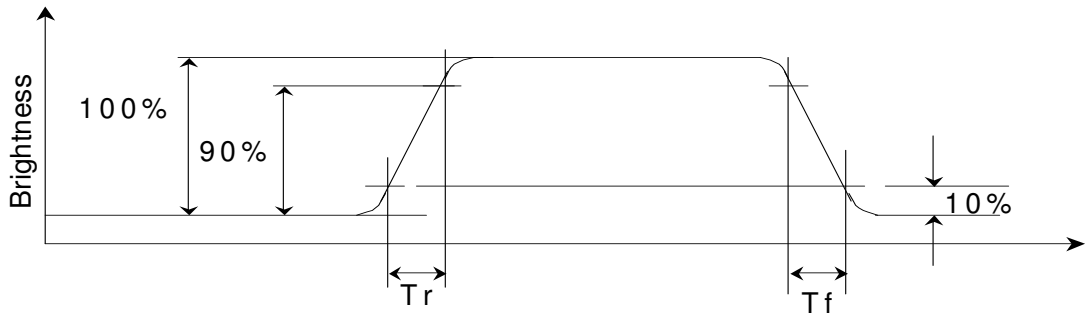
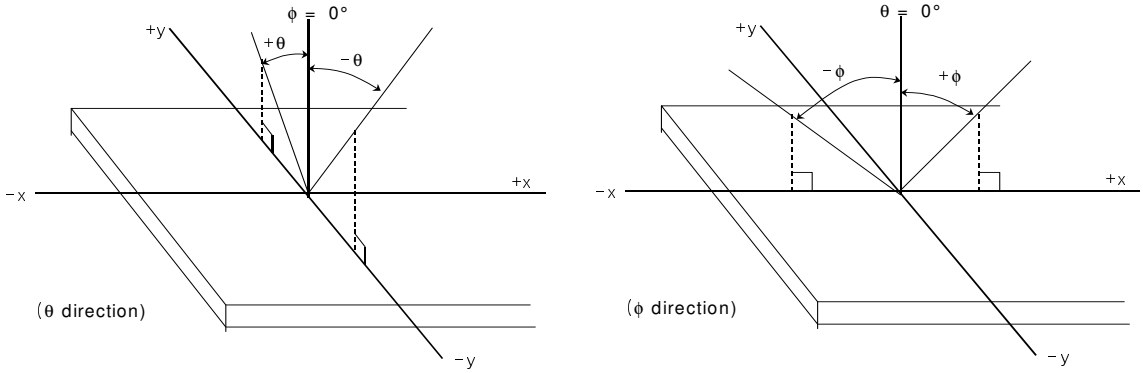


Figure 2 Response time

D. DEFINITION OF VIEWING ANGLE

The viewing angle is defined as Figure 3. Horizontal and vertical (H & V) angles are determined for viewing directions where luminance varies by 50% of the perpendicular value.



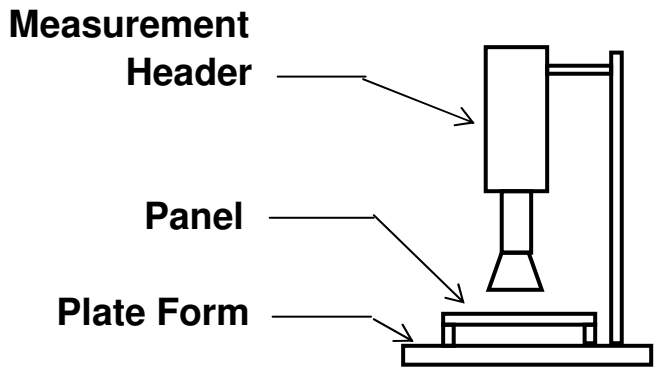
Vertical angles **Horizontal angles**

Figure 3 Viewing Angle

APPENDIX 2: MEASUREMENT APPARATUS

A. LUMINANCE/COLOR COORDINATE

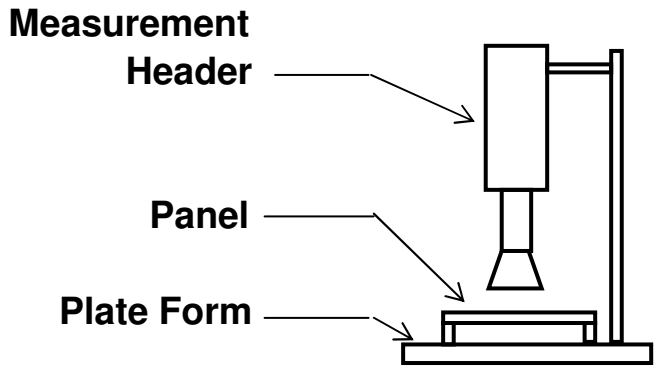
PHOTO RESEARCH PR-705, MINOLTA CS-100



**PR-705 /
MINOLTA CS-100
Color Analyzer**

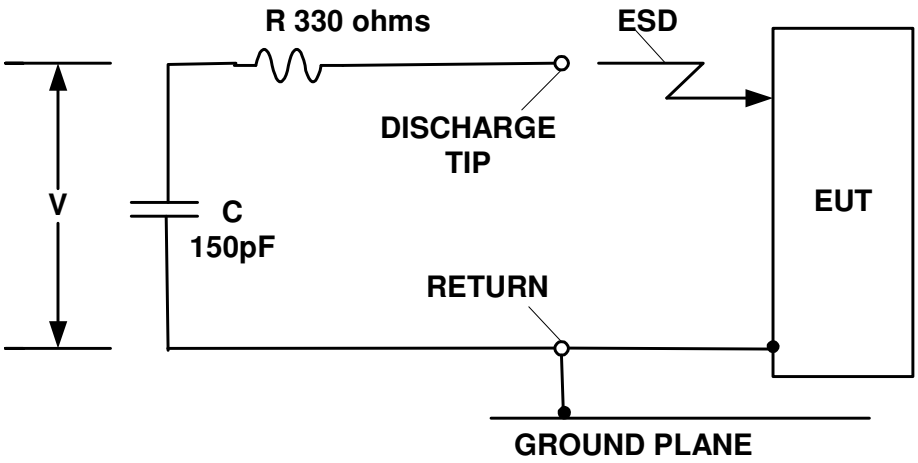
B. CONTRAST / RESPONSE TIME / VIEWING ANGLE

WESTAR CORPORATION FPM-510



**Westar FPM-510
Display Contrast /
Response time /
View angle Analyzer**

C. ESD ON AIR DISCHARGE MODE



APPENDIX 3: PRECAUTIONS

A. RESIDUE IMAGE

Because the pixels are lighted in different time, the luminance of active pixels may reduce or differ from inactive pixels. Therefore, the residue image will occur. To avoid the residue image, every pixel needs to be lighted up uniformly.