US Micro Products
ENGINEERED DISPLAY SOLUTIONS

PMOLED SPECIFICATION

Part Number	USMP-P007-096016WBI-A0
Size	0.7"
Resolution	96 x 16
Color	White
IC	LD7054
Brightness	1300 cd/m^2
Contrast	2000:1
Operating temp.	-40 ~ 70℃

FOR ADDITIONAL INFORMATION
PLEASE CONTACT:
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Issue Date	Approved by (customer use)	Checked by	Prepared by

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REVISION RECORD

REV.	REVISION DESCRIPTION	REV. DATE	REMARK
X01	■ INITIAL RELEASE	2015. 12. 29	
X02	■ Add the information of module weight ■ Add the panel electrical specifications ■ Add the application circuit	2016. 04. 21	Page 5, 6, 7, 8 & 15
X03	■ Modify luminance specifications	2016. 07. 26	Page 7 & 8

CONTENTS

1. SCOPE

The purpose of this specification is to define the general provisions and quality requirements that apply to the supply of display cells manufactured by USMP. This document, together with the Module Assembly Drawing, is the highest-level specification for this product. It describes the product, identifies supporting documents and contains specifications.

2. WARRANTY

USMP warrants that the products delivered pursuant to this specification (or order) will conform to the agreed specifications for twelve (12) months from the shipping date ("Warranty Period"). USMP is obligated to repair or replace the products which are found to be defective or inconsistent with the specifications during the Warranty Period without charge, on condition that the products are stored in the original packages at 25°C±5°C, 55%±10%RH or used as the conditions specified in the specifications.

Nevertheless, USMP is not obligated to repair or replace the products without charge if the defects or inconsistency are caused by the force majeure or the reckless behaviors of the customer.

After the Warranty Period, all repairs or replacements of the products are subject to charge.

3. FEATURES

- Small molecular organic light emitting diode.
- Color : White
- Panel resolution : 96x16
- Driver IC : LD7054
- Excellent Quick response time : 10μs
- Extremely thin thickness for best mechanism design : 1.02 mm
- High contrast : 2000:1
- Wide viewing angle : 160°
- 4wire Serial Peripheral Interface, I^2C Serial Interface.
- Wide range of operating temperature : -40 to 70℃

4. MECHANICAL DATA

NO	ITEM	SPECIFICATION	UNIT
1	Dot Matrix	96 x 16	dot
2	Dot Size	0.185 (W) x 0.164 (H)	mm^2
3	Dot Pitch	0.205 (W) x 0.184 (H)	mm^2
4	Aperture Rate	80	%
5	Active Area	17.644 (W) x 3.26 (H)	mm^2
6	Panel Size	24 (W) x 7.44 (H)	mm^2
7*	Panel Thickness	1.02	mm
8	Module Size	34 (W) x 7.44 (H) x 1.02 (T)	mm^3
9	Diagonal A/A size	0.7	inch
10	Module Weight	0.42 ± 10%	gram

* Panel thickness includes substrate glass, cover glass and UV glue thickness.

5. MAXIMUM RATINGS

ITEM	MIN	MAX	UNIT	Condition	Remark
Supply Voltage (VDD)	-0.3	6	V	Ta = 25℃	IC maximum rating
Supply Voltage (VCC-C)	8	19.5	V	Ta = 25℃	IC maximum rating
Operating Temp.	-40	70	℃	-	-
Storage Temp	-40	85	℃	-	-

Note:

(1) Maximum ratings are those values beyond which damages to the OLED module may occur. The OLED functional operation should be restricted to the limits in the section 6. Electrical Characteristics tables.

6. ELECTRICAL CHARACTERISTICS

6.1 D.C ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETERS	TEST CONDITION	MIN	TYP	MAX	UNIT
VCC-C	Driver power supply (for OLED panel)	Ta = 25℃	11.5	12	12.5	V
VDD	Logic Power 1 (Table 6.1)	Ta = 25℃	1.65	-	3.5	V
VDDL	Logic Power 2 (Table 6.1)	Ta = 25℃	1.65	-	2.0	V
V_{OH}	High logic output level	Iout=100 uA	0.9* V_{DD}	-	V_{DD}	V
V_{OL}	Low logic output level	Iout=100uA	0	-	0.1* V_{DD}	V
V_{IH}	High logic input level	-	0.7* V_{DD}	-	V_{DD}	V
V_{IL}	Low logic input level	-	0	-	0.3* V_{DD}	V

Table 6.1

VDD	VDDL	Remark
1.65 V ~ 2.0V	VDDL= VDD	VDD Reg. OFF(PSEL=GND)
2.5V ~ 3.5V	Internal Regulator	VDD Reg. ON(PSEL=VDD)

6.2 ELECTRO-OPTICAL CHARACTERISTICS

PANEL ELECTRICAL SPECIFICATIONS

PARAMETER	MIN	TYP.	MAX	UNITS	COMMENTS
Normal mode current consumption (ICC-C)	-	10	10.5	mA	All pixels on (1)
	-	3.5	4	mA	20% pixels on (1)
Standby mode current consumption (ICC-C)	-	1	2	mA	Standby mode 10% pixels on (2)
Normal mode power consumption	-	120	126	mW	All pixels on (1)
	-	42	48	mW	20% pixels on (1)
Standby mode power consumption	-	12	24	mW	Standby mode 10% pixels on (2)
IDD sleep mode current	-	-	30	uA	Sleep mode Current (3)
ICC-C sleep mode current	-	-	5	uA	Sleep mode Current (3)
Pixel Luminance	1200	1300		cd/m^2	Display Average
Standby Luminance		20		cd/m^2	
CIEx (White)	0.26	0.30	0.34		CIE1931
CIEy (White)	0.29	0.33	0.37		CIE1931
Dark Room Contrast	2000:1				
Viewing Angle	160			degree	
Response Time		10		μs	

(1) Normal mode condition : (without polarizer)

- Driving Voltage : 12V
- Contrast setting : 0xaf
- Frame rate : 225Hz
- Duty setting : 1/16

(2) Standby mode condition : (without polarizer)

- Driving Voltage : 12V
- Contrast setting : 0x09
- Frame rate : 225Hz
- Duty setting : 1/16

(3) Sleep mode condition :

When send (0x14)→(0x01), (0x02)→(0x00) command OLED will display off.

(4) Wake up condition :

When send (0x14)→(0x00), (0x02)→(0x01) command OLED will be turned on.

7. LIFETIME SPECIFICATION

ITEM	MIN	UNIT	Condition	Remark
Life Time	6,500	Hrs	1400 cd/m^2, 50% checkerboard	Note (1)
Life Time	7,500	Hrs	1300 cd/m^2, 50% checkerboard	Note (2)
Life Time	8,800	Hrs	1200 cd/m^2, 50% checkerboard	Note (3)

Note:

(A) Under Vcc = 12V, Ta = 25℃, 50% RH.

(B) Life time is defined the amount of time when the luminance has decayed to less than 50% of the initial measured luminance.

(1) Setting of 1400 cd/m^2 : (without polarizer)

- Contrast setting : 0xc0
- Frame rate : 225Hz
- Duty setting : 1/16

(2) Setting of 1300 cd/m^2 : (without polarizer)

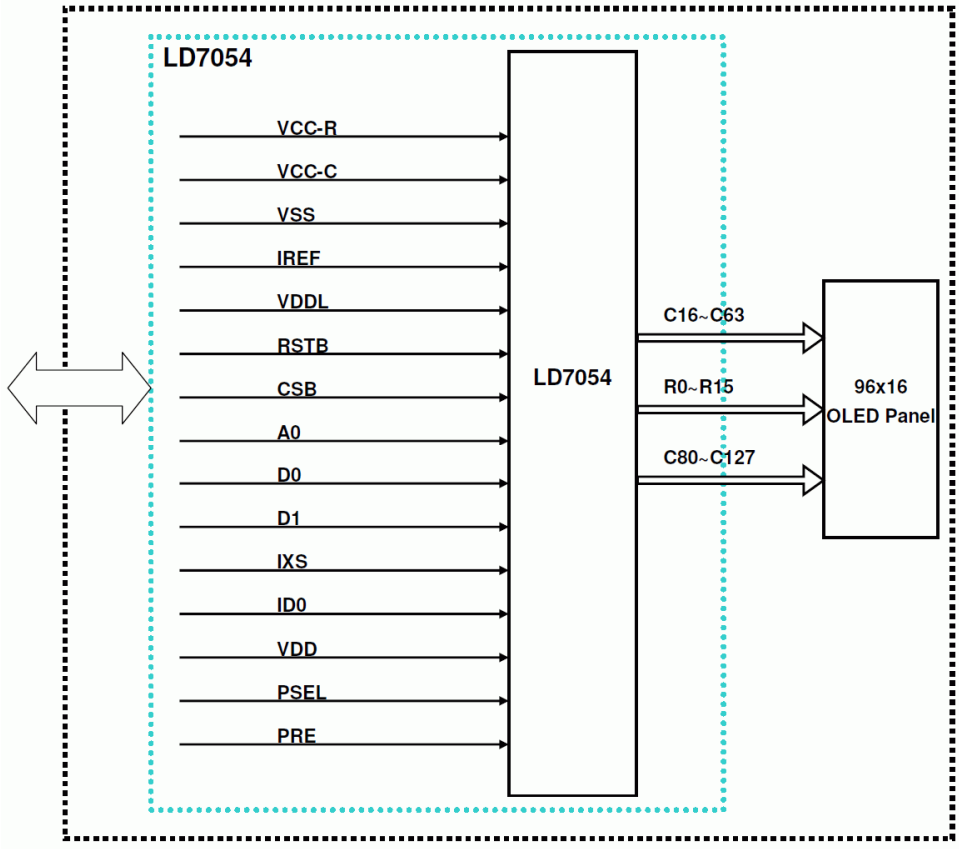
- Contrast setting : 0xaf
- Frame rate : 225Hz
- Duty setting : 1/16

(3) Setting of 1200 cd/m^2 : (without polarizer)

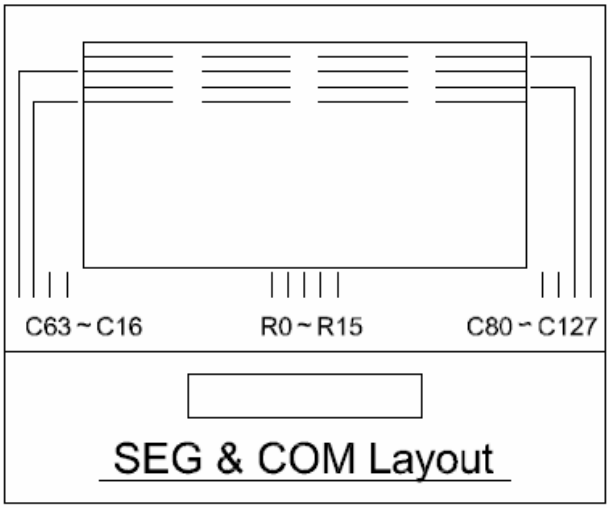
- Contrast setting : 0xa1
- Frame rate : 225Hz
- Duty setting : 1/16

8. INTERFACE

8.1 FUNCTION BLOCK DIAGRAM



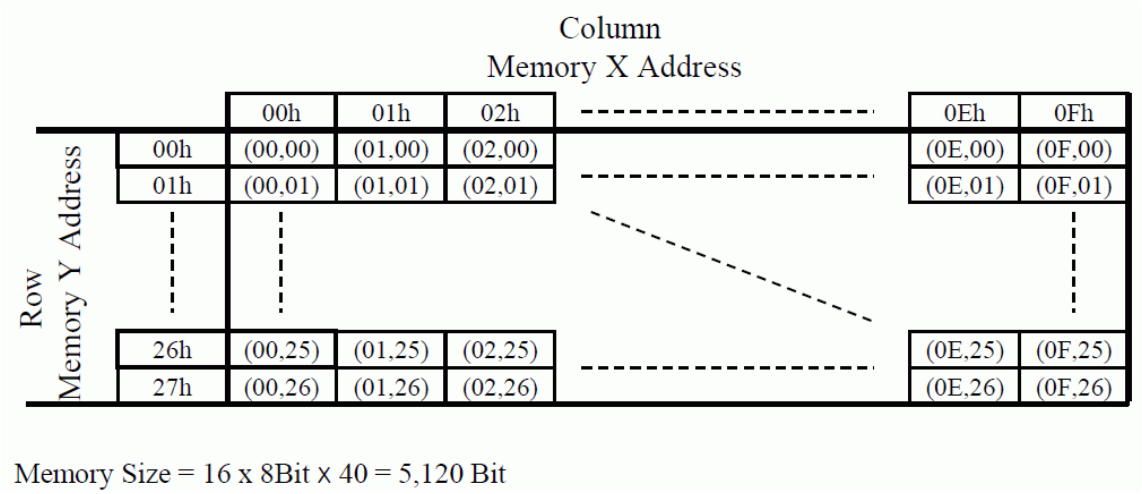
8.2 PANEL LAYOUT DIAGRAM



8.3 PIN ASSIGNMENTS

PIN NAME	PIN NO.	DESCRIPTION
VCC-R	1	OLED Dot Matrix Power Supply for Scan Driver Regulator Enable : connect ceramic capacitor 4.7uF between VCC-R and VSS.
VCC-C	2	OLED Dot Matrix Power Supply for Column Driver and Scan Driver.
VSS	3	Ground pin.
IREF	4	This pin is the dot output current reference pin. A resister should be connected between this pin and VSS.
VDDL	5	Internal Logic Power. Capacitor is connected between VDDL and VSS.
RSTB	6	Reset (Active Low).
CSB	7	Chip Select (Active Low).
A0	8	Address (L: command, H: Parameter).
D0	9	When I^2C interface mode is selected, D1 will be the I^2C data input (SDA) and D0 will be the I^2C bus clock input (SCL). When serial interface mode is selected, D1 will be the serial data input (SDIN), D0 will be the serial clock input (SCLK).
D1	10	
IXS	11	H : I^2C is selected, L : I^2C is not selected.
ID0	12	This pin configure I^2C interface address.Using this pin, I^2C Address can be selected.
VDD	13	Interface Block Power, Logic & Analog Power.
PSEL	14	This pin enable/disable internal logic power regulator. When this pin is tied with VDD pin, it is the internal logic power regulator enabled.
PRE	15	Column Driver Low Power.

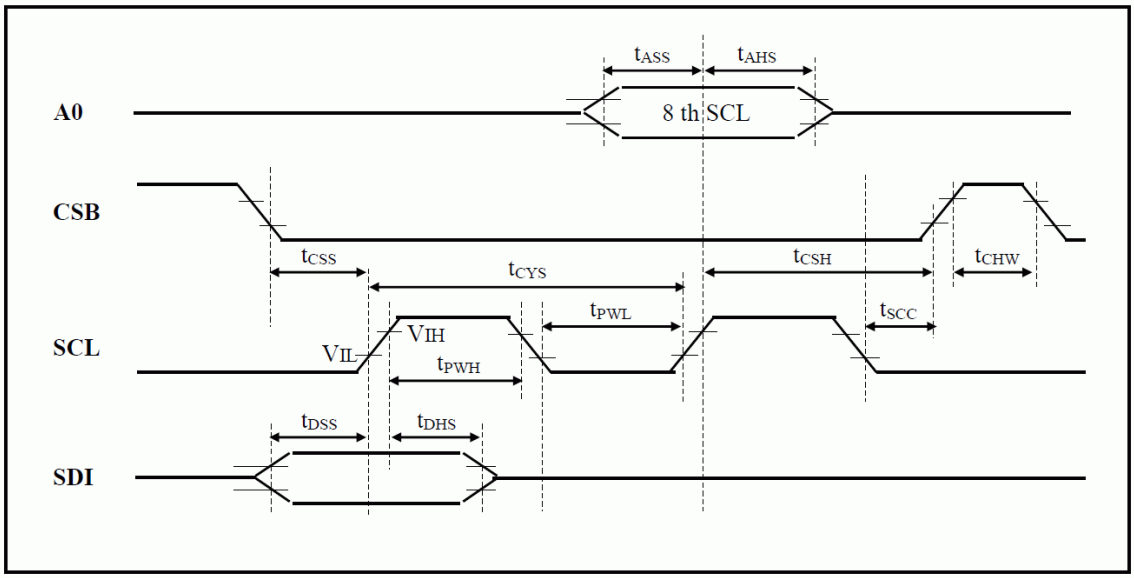
8.4 GRAPHIC DISPLAY DATA RAM ADDRESS MAP



Memory Size = 16 x 8Bit x 40 = 5,120 Bit

8.5 INTERFACE TIMING CHART

Serial Interface1

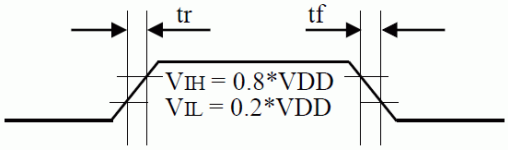


(VSS = 0V, VDD= 2.6V~3.5V, Ta = 25℃)

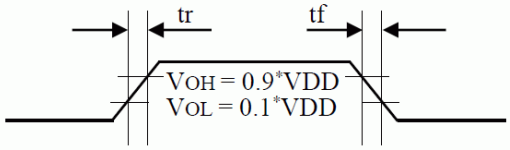
Symbol	Parameter	Conditions	Related Pins	MIN	TYP	MAX	Unit
t_{CYS} t_{PWH} t_{PWL}	Serial clock cycle High pulse Width Low pulse width	-	SCL	66 20 20	- -	- -	ns
t_{ASS} t_{AHS}	A0 setup time A0 hold time		A0	15 25	- -	- -	ns
t_{DSS} t_{DHS}	Data setup time Data hold time		SDI	20 20	- -	- -	ns
t_{CSS} t_{CSH} t_{CSW}	Chip select setup time Chip select hold time Chip select high pulse width	-	CSB	20 50 50	- - -	- - -	ns
t_{SCC}	SCL to Chip select	-	SCL, CSB	15	-	-	ns

NOTE : The input signal rise time and fall time (tr, tf) is specified at 15 ns or less.

Input Signal Slope



Output Signal Slope



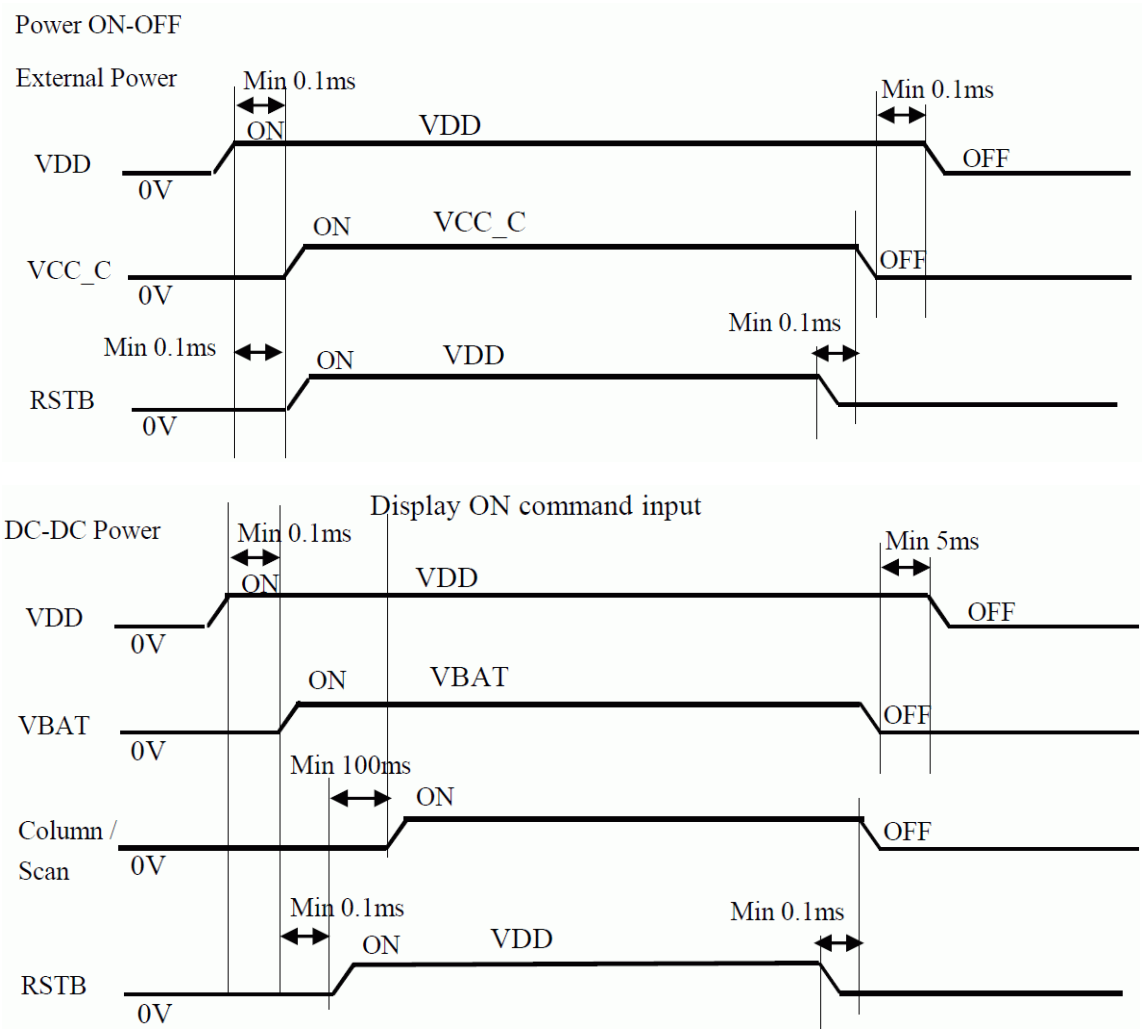
Serial Interface2

(VSS = 0V, VDD= 1.65V~3.5V, Ta = 25℃)

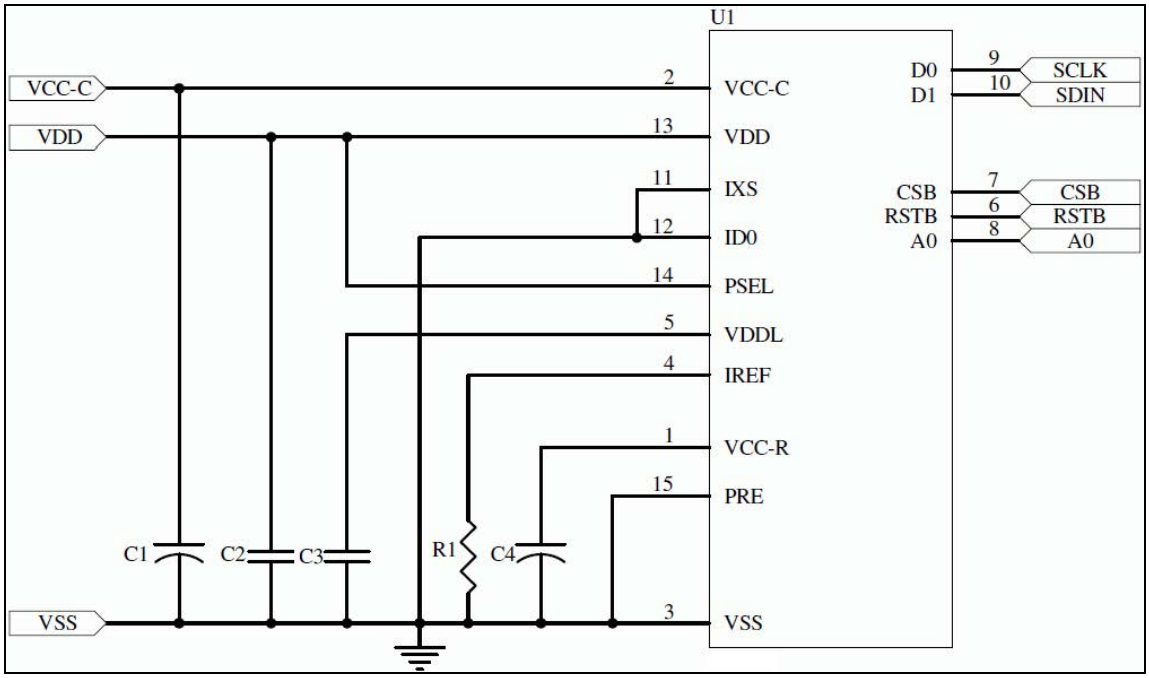
Symbol	Parameter	Conditions	Related Pins	MIN	TYP	MAX	Unit
t_{CYS} t_{PWH} t_{PWL}	Serial clock cycle High pulse Width Low pulse width	-	SCL	150 60 60	- -	- -	ns
t_{ASS} t_{AHS}	A0 setup time A0 hold time		A0	50 60	- -	- -	ns
t_{DSS} t_{DHS}	Data setup time Data hold time		SDI	60 60	- -	- -	ns
t_{CSS} t_{CSH} t_{CSW}	Chip select setup time Chip select hold time Chip select high pulse width	-	CSB	60 100 100	- - -	- - -	ns
t_{SCC}	SCL to Chip select	-	SCL, CSB	40	-	-	ns

9. POWER ON / OFF SEQUENCE & APPLICATION CIRCUIT

9.1 POWER ON / OFF SEQUENCE



9.2 APPLICATION CIRCUIT



Recommend components:

C1: 2.2uF/16V(0805)

C4: 4.7uF/16V(0805)

C2, C3: 1uF/6.3V(0603)

R1: 68K ohm 1%(0603)

This circuit is for SPI interface.

9.3 COMMAND TABLE

Refer to IC Spec.: LD7054

10. RELIABILITY TEST CONDITIONS

No.	Items	Specification	Quantity
1	High temp. (Non-operation)	85℃, 240hrs	5
2	High temp. (Operation)	70℃, 120hrs	5
3	Low temp. (Operation)	-40℃, 120hrs	5
4	High temp. / High humidity (Operation)	65℃, 90%RH, 120hrs	5
5	Thermal shock (Non-operation)	-40℃ ~85℃ (-40℃ /30min; transit /3min; 85℃ /30min; transit /3min) 1cycle: 66min, 100 cycles	5
6	Vibration	Frequency : 5~50HZ, 0.5G Scan rate : 1 oct/min Time : 2 hrs/axis Test axis : X, Y, Z	1 Carton
7	Drop	Height: 120cm Sequence : 1 angle、3 edges and 6 faces Cycles: 1	1 Carton
8	ESD (Non-operation)	Air discharge model, ±8kV, 10 times	5

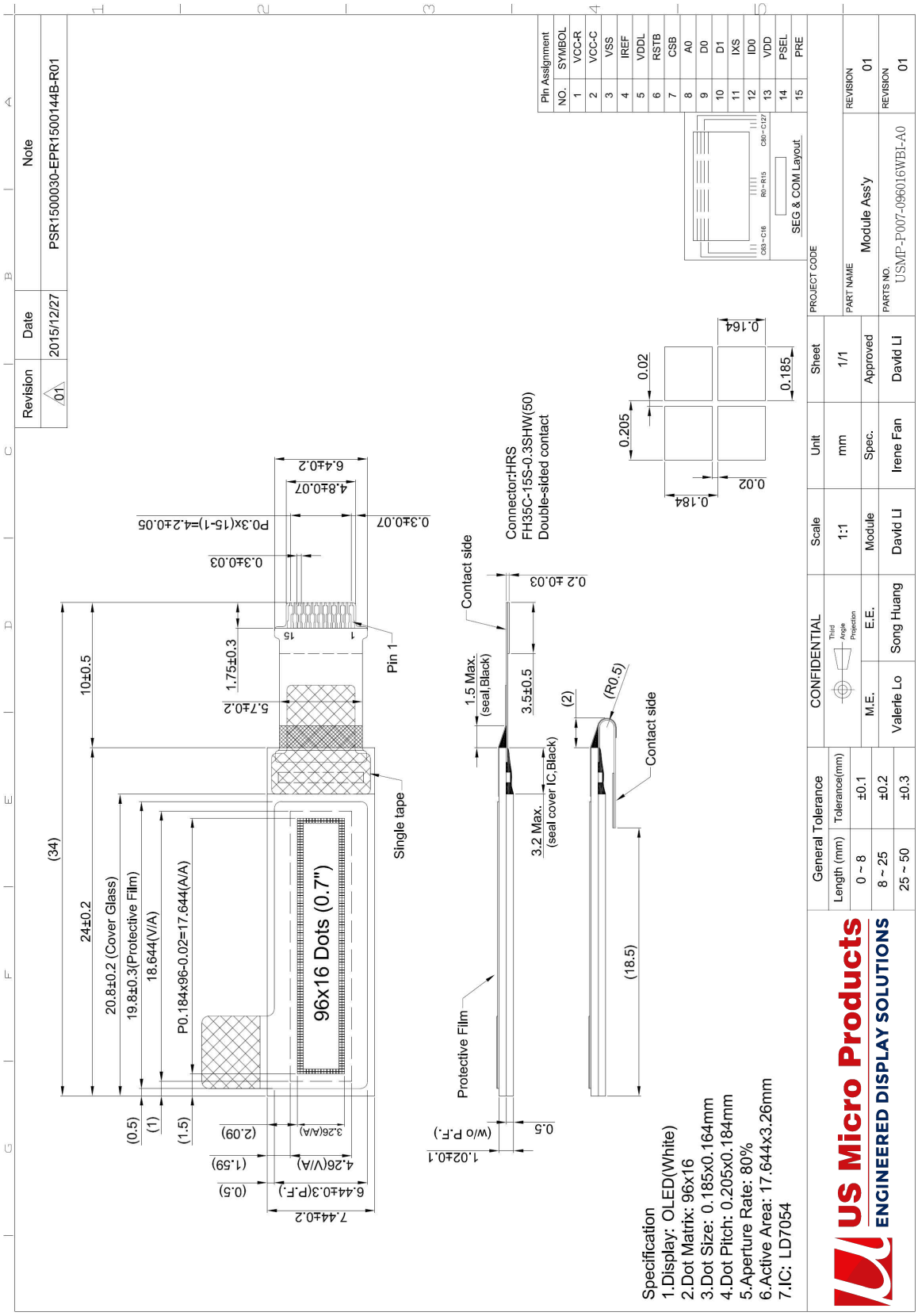
Test and measurement conditions

1. All measurements shall not be started until the specimens attain to temperature stability.
2. All-pixels-on is used as operation test pattern.

Evaluation criteria

1. The function test is OK.
2. No observable defects.
3. Luminance: > 50% of initial value.
4. Current consumption: within ± 50% of initial value.

11. EXTERNAL DIMENSION



12. PACKING SPECIFICATION

TBD

13. APPENDIXES

APPENDIX 1: DEFINITIONS

A. DEFINITION OF CHROMATICITY COORDINATE

The chromaticity coordinate is defined as the coordinate value on the CIE 1931 color chart for R, G, B, W.

B. DEFINITION OF CONTRAST RATIO

The contrast ratio is defined as the following formula:

$$\text{Contrast Ratio} = \frac{\text{Luminance of all pixels on measurement}}{\text{Luminance of all pixels off measurement}}$$

C. DEFINITION OF RESPONSE TIME

The definition of turn-on response time Tr is the time interval between a pixel reaching 10% of steady state luminance and 90% of steady state luminance. The definition of turn-off response time Tf is the time interval between a pixel reaching 90% of steady state luminance and 10% of steady state luminance. It is shown in Figure 2.

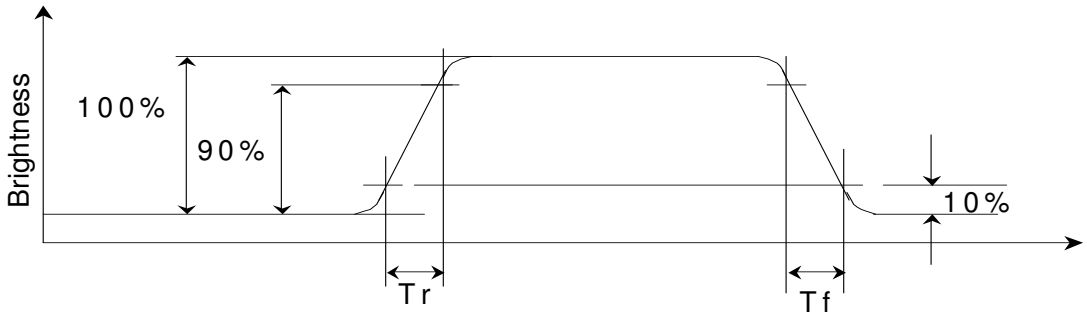


Figure 2 Response time

D. DEFINITION OF VIEWING ANGLE

The viewing angle is defined as Figure 3. Horizontal and vertical (H & V) angles are determined for viewing directions where luminance varies by 50% of the perpendicular value.

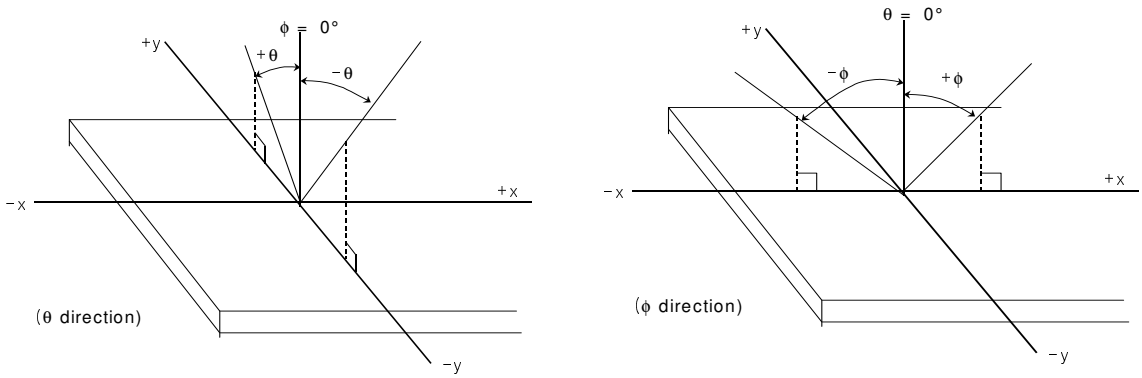
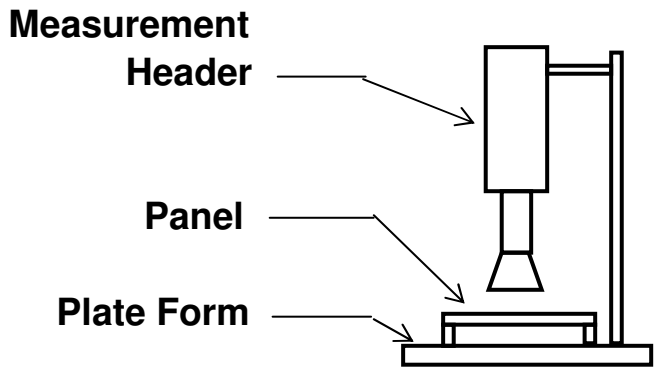


Figure 3 Viewing angle

APPENDIX 2: MEASUREMENT APPARATUS

A. LUMINANCE/COLOR COORDINATE

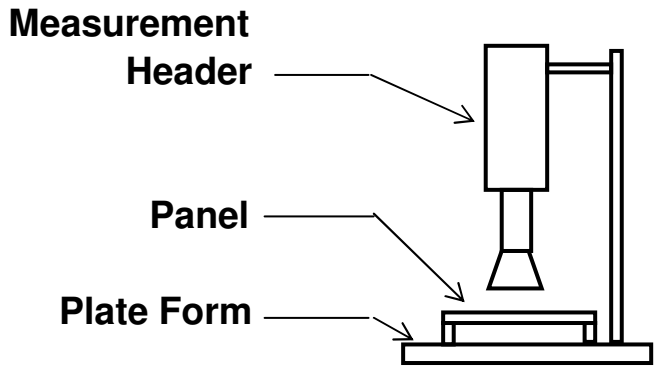
PHOTO RESEARCH PR-705, MINOLTA CS-100



**PR-705 /
MINOLTA CS-100
Color Analyzer**

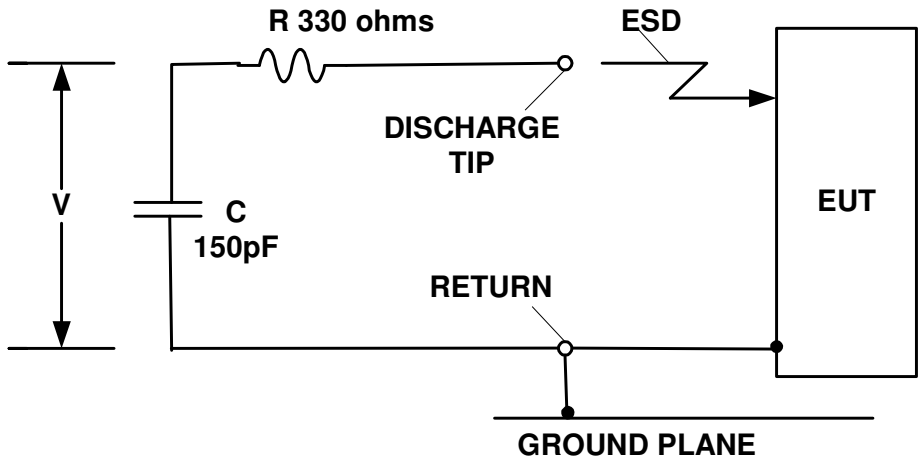
B. CONTRAST / RESPONSE TIME / VIEWING ANGLE

WESTAR CORPORATION FPM-510



**Westar FPM-510
Display Contrast /
Response time /
View angle Analyzer**

C. ESD ON AIR DISCHARGE MODE



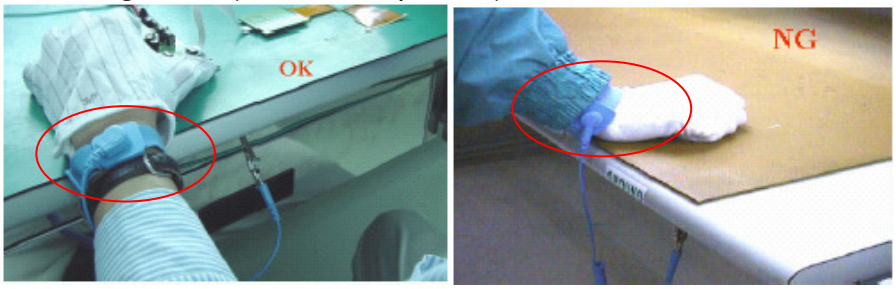
APPENDIX 3: PRECAUTIONS FOR USING THE OLED MODULE

Precautions for Handling

1. When handling the module, wear powder-free antistatic rubber finger cots, and be careful not to bend and twist it.

2. The OLED module is consisted of glass and film, and it should avoid pressure, strong impact, or being dropped from a high position.

3. The OLED module is an electronic component and is subject to damage caused by Electro Static Discharge (ESD). And hence normal ESD precautions must be taken when handling it. Also, appropriate ESD protective environment must be administered and maintained in the production line. When handling and assembling the panel, wear an antistatic wrist strap with the alligator clip attached to the ground to prevent ESD damage on the panel. Antistatic wrist strap should touch human body directly instead of gloves. (See below photos).



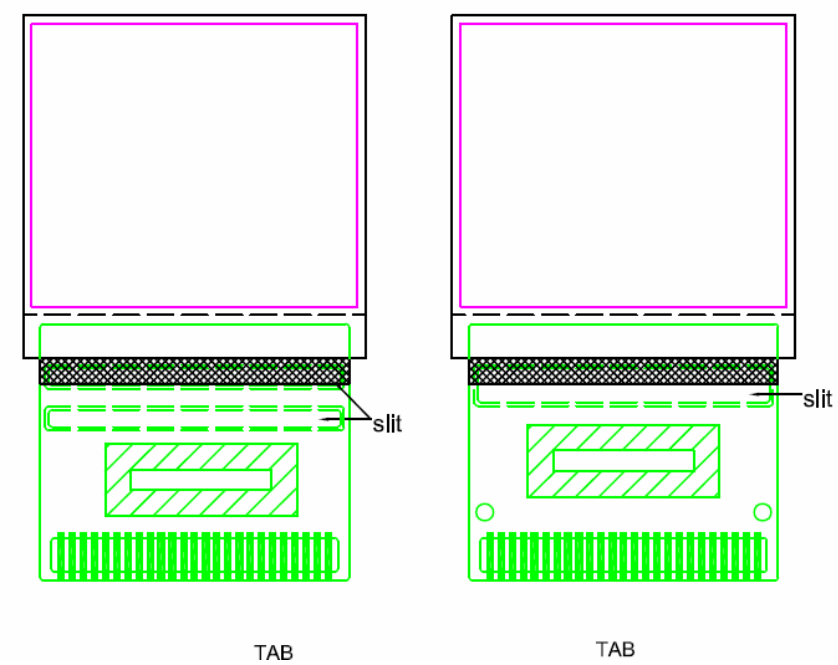
4. Take out the panel one by one from the holding trays for assembly, and never put the panel on top of another one to avoid the scratch.

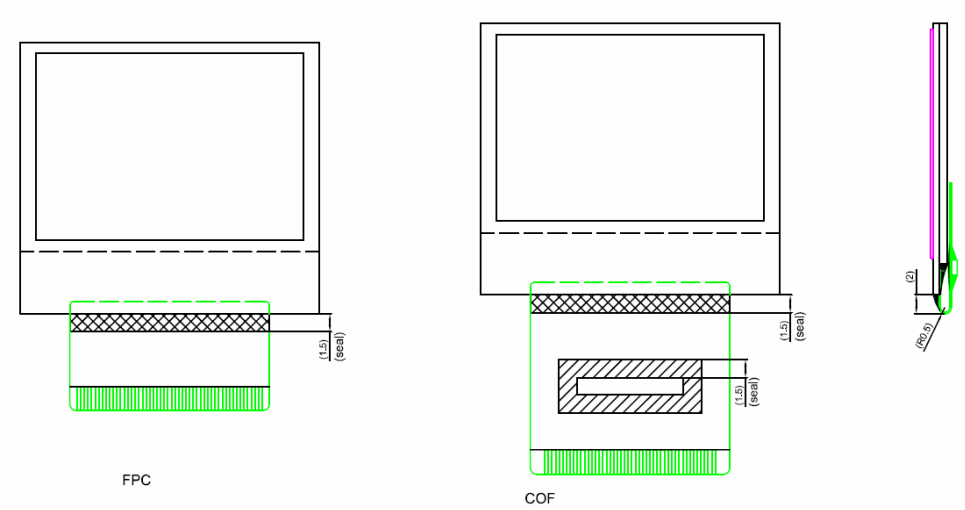
5. Avoid jerk and excessive bend on TAB/FPC/COF, and be careful not to let foreign matter or bezel damage the film.

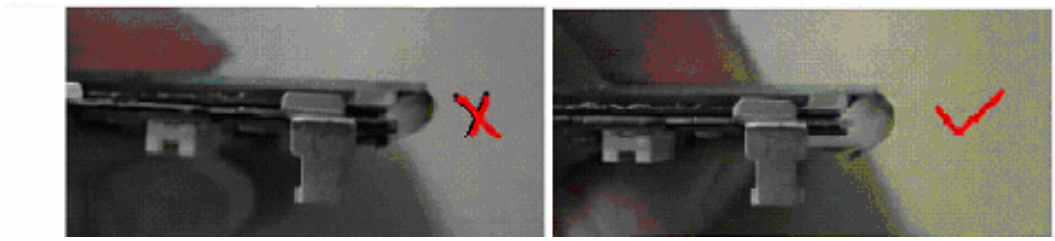
6. When handling and assembling the module (panel + IC), grab the panel, not the TAB/FPC/COF.

7. Use the tweezers to open the clicks on the connector of PCB before the insertion of FPC/COF, and click them back in. Once the FPC/COF sits properly in the connector, use the tweezers to avoid the damages.

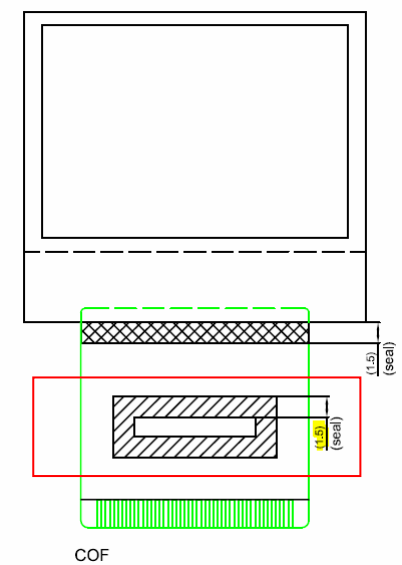
8. Please do not bend the film near the substrate glass. It could cause film peeling and TAB/FPC/COF damage. For TAB, It should bend the slit area as actual OLED it is. For FPC or COF, it is suggested to follow below pictures for instruction (distance between substrate glass and bending area >1.5mm; R>0.5mm).

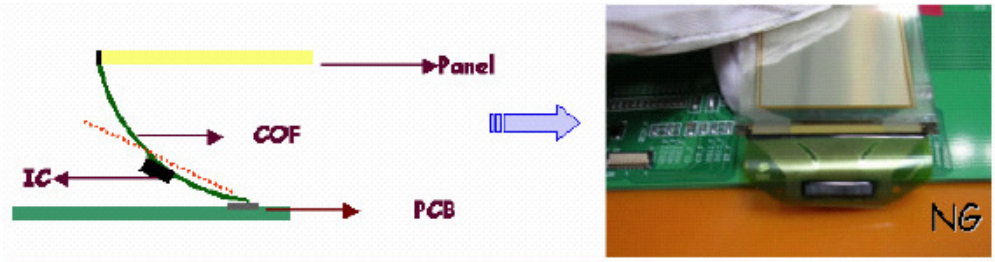




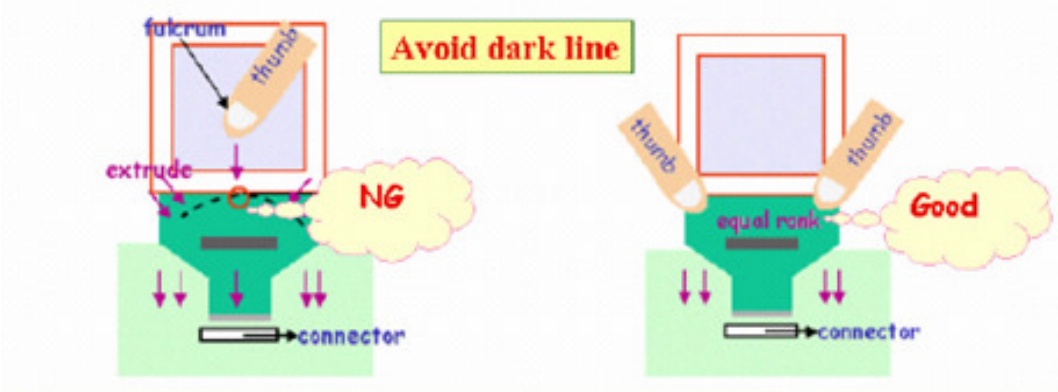


9. Avoid bending the film at IC bonding area. It could damage the IC ILB bonding. It should avoid bending the IC seal area. Please keep the bending distance >1.5mm.





10. Use both thumbs to insert COF into the connector when assembling the panel. Please refer to the photo.



11. Do not wipe the pin of film and polarizer with the dry or hard materials that will damage the surface. When cleaning the display surface, use the soft cloth with solvent, IPA or alcohol, to clean.

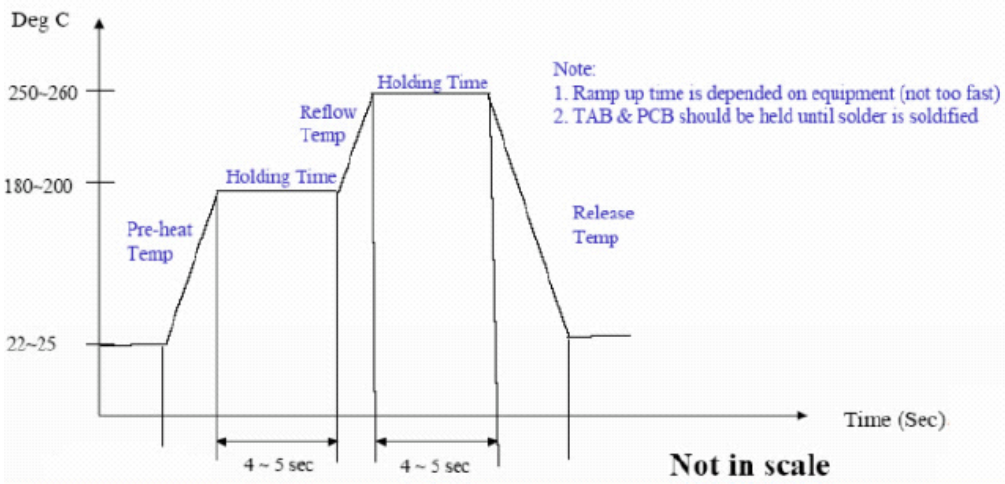
12. Protection film is applied to the surface of OLED panel to avoid the scratch. Please remove the protective film before assembling it. If the OLED panel has been stored for a long time, the residue adhesive material of the protective film may remain on the display surface after remove the protective film. Please use the soft cloth with solvent, IPA or alcohol, to clean.

13. When hand or hot-bar soldering TAB/FPC onto PCB, make sure the temperature and timing profiles to meet the requirements of soldering specification (the specification depends on the application or optimized by customer) to prevent the damage of IC pins by inappropriate soldering.

14. Solder residues arise from soldering process have to be cleaned up thoroughly before the module assembly.

15. Use the voltage and current settings listed in the specification to do the function test after the module assembly.

16. Suggestion for soldering process:
    i. TAB Lead- free soldering hot bar process
        1. Use pulse heated bonding tool equipment
        2. Material: Sn/Ag/Cu lead-free solder paste with typical 25um thickness on PCB pad. The TAB pin size and shape may be different, please base on the production line to adjust the thickness of PCB pad and temperature.
        3. Bonding Force:--4kg per centimeter square as the starting point.
        4. Suggested bonding tool temperature & time profile is as below for reference. Since there are differences in TAB soldering pins, soldering technicians' skills, mechanism…etc., the soldering conditions must be adequately tuned.



ii. TAB Lead- free soldering wire process
In case of manual soldering (Lead- free solder wire)
1. Solder wire contact iron directly: 280±5℃ at 3-5secs
2. Solder wire contact TAB lead directly (near iron but not contact): 380±5℃, 3-5secs
3. Since there are differences in TAB soldering pins, soldering technicians' skills, mechanism…etc., the soldering conditions must be adequately tuned.

iii. High temperature will result in rapid heat conduction to IC and might cause damage to IC, so please keep the temperature below 380℃. Also, avoid damaging the polyimide and solder resist which might take place at high temperatures. Refold cycles base on the de-soldering status, if the plating of pin was damaged, it can not be used again.

Precautions for Electrical

1. Design using the settings in the specification

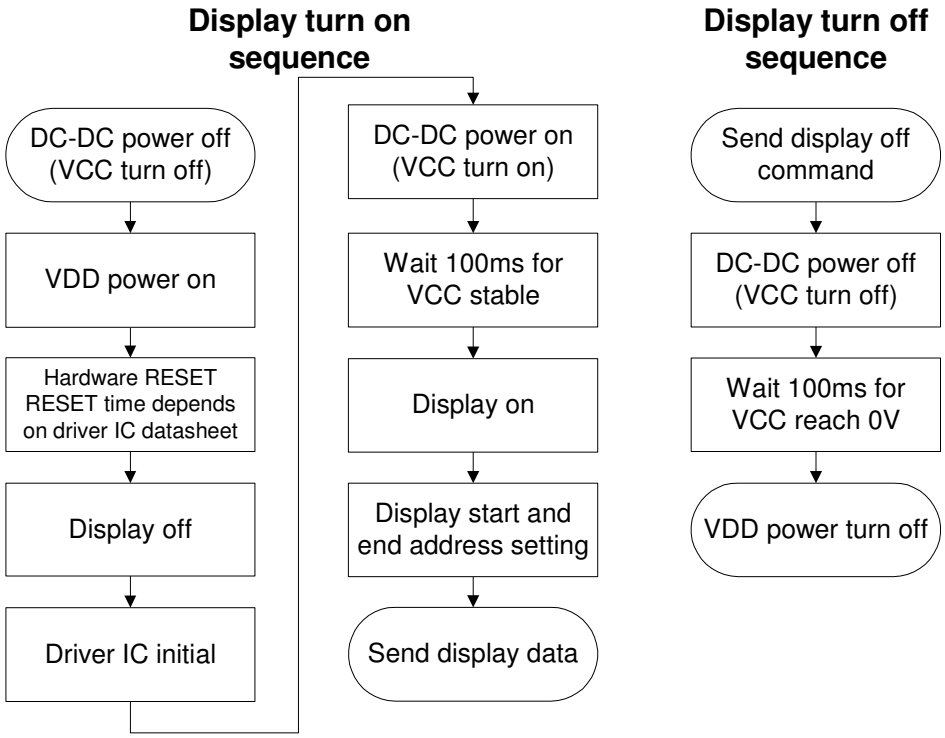
It is very important to design and operate the panel using the settings listed in the specification. It includes voltage, current, frame rate and duty cycle... etc. Operation the OLED outside the range of the specification should be entirely avoided to ensure proper operation of the OLED.

2. Maximum Ratings

To ensure the proper operation of the panel, never design the panel with parameters running over the maximum ratings listed in the specification. Also the logic voltages such as VIL and VIH have to be within the specified range in the specification to prevent any improper operation of the panel.

3. Power on/off procedure

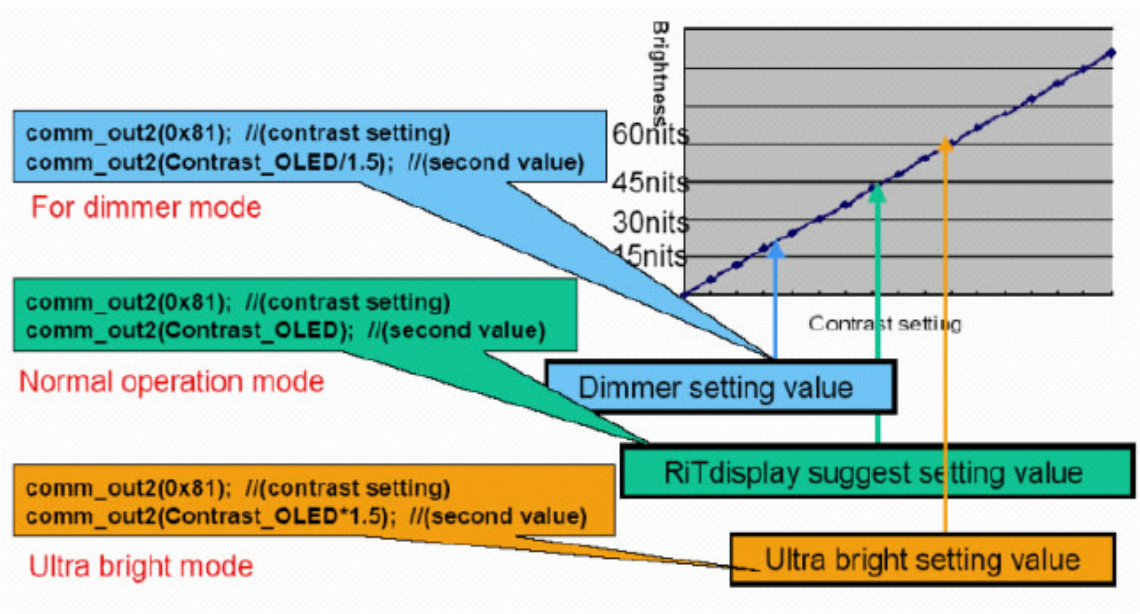
To avoid any inadvertent effects resulting from inappropriate power on/off operations, please follow the directions of power on/off procedure on page 6. Any operation that does not comply with the procedure could cause permanent damage of the IC and should be avoided. When the logic power is not on, do not activate any input signal. Abrupt shutdown of power to the module, while the OLED panel is on, would cause OLED panel malfunction.



4. Power savings

To save power consumption of the OLED, please use partial display or sleep mode when the panel is not fully activated. Also, if possible, make the black background to save power.

The OLED is a self-luminous device and a particular pixel cluster or image can be lit on via software control. So power savings can be achieved by partial display or dimming down the luminance. Depending on the application, the user can choose among Ultra Bright Mode, Normal Operation Mode, and Sleeping Mode. The power consumption is almost in directly proportion to the brightness of the panel, and also in directly proportion to the number of pixels lit on the panel. The customer can save the power by the use of black background and sleeping mode. One benefit from using these design schemes is the extension of the OLED lifetime.



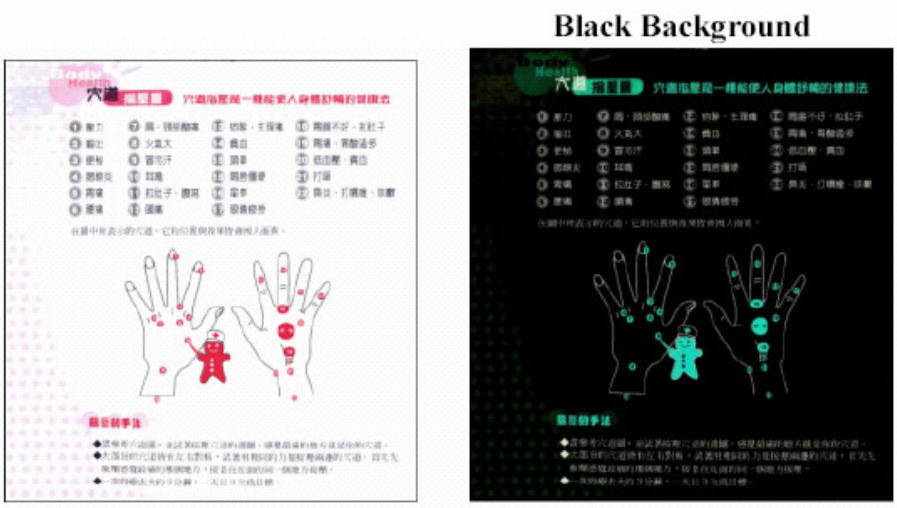
5. Adjusting the luminance of the panel

Although there are a couple of ways to adjust the luminance of the panel, it is strongly recommended that the customer change the contrast setting to adjust the luminance of the panel. Adjusting voltages to achieve desired luminance is not allowed. Be aware that the adjustment of luminance would accompany the change of lifetime of the panel and its power consumption as well.

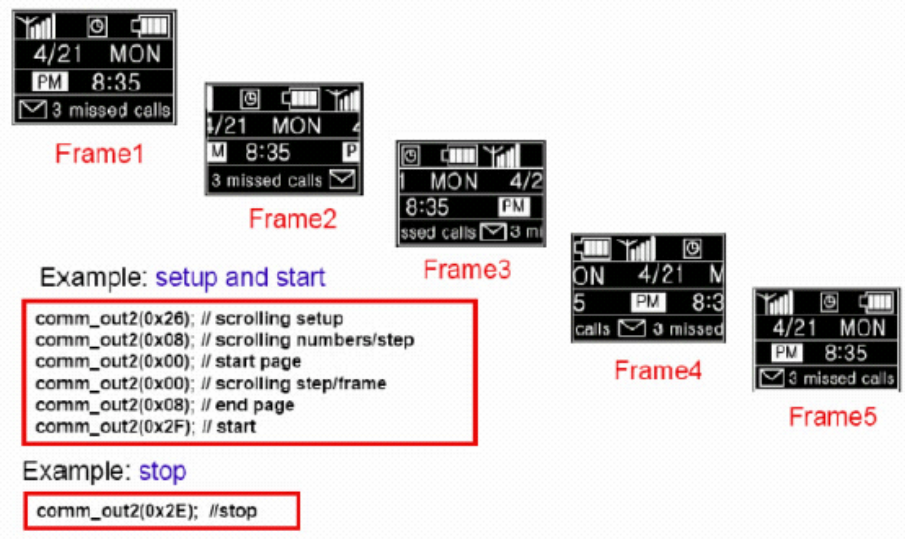
6. Residual Image (Image Sticking)

The OLED is a self-emissive device. As with other self-emissive device or displays consisting of self-emissive pixels, when a static image frozen for a long period of time is changed to another one with all-pixels-on background, residual image or image sticking is noticed by the human eye. Image sticking is due to the luminance difference or contrast between the pixels that were previously turned on and the pixels that are newly turned on. Image sticking depends on the luminance decay curve of the display. The slower the decay, the less prominent the image sticking is. It is strongly recommended that the user employ the following four strategies to minimize image sticking.

1. Employ image scrolling or animation to even out the lit-on time of each and every pixel on the display, also could use sleeping mode for reduced the residual image and extend the power capacity.
2. Minimize the use of all-pixels-on or full white background in their application because when the panel is turned on full white, the image sticking from previously shown patterns is the most revealing. Black background is the best for power savings, greatest visibility, eye appealing, and dazzling displays.
3. Avoid displaying the characters or menu with high brightness level in a fix position for a long time or repeatedly. If necessary, using the auto fadeout technology.
4. If a static logo is used in the reliability test, change the pattern into its inverse (i.e., turn off the while pixels and turn on the previously unlit pixels) and freeze the inverse pattern as long as the original logo is used, so every pixel on the panel can be lit on for about the same time to minimize image sticking, caused by the differential turn-on time between the original and its reverse patterns.



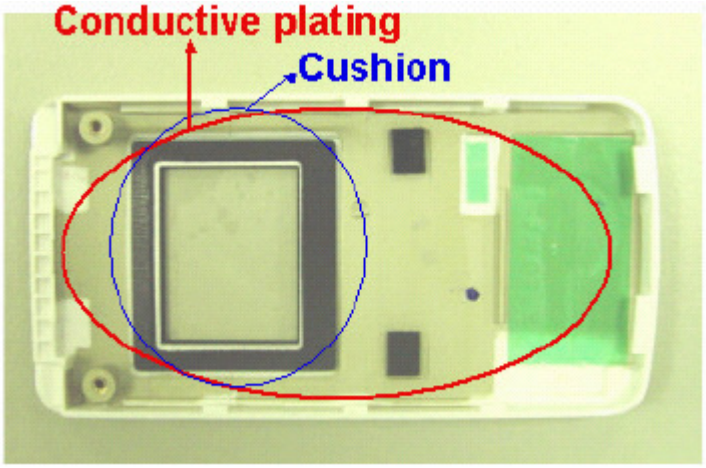
Scrolling example



Precautions for Mechanical

1. Cushion or Buffer tape on the cover glass

It is strongly recommended to have a cushion or buffer tape to apply on the panel backside and front side when assembling OLED panel into module to protect it from damage due to excessive extraneous forces.



It is recommended that a plating conductive layer be used in the housing for EMI/EMC protection. And, the enough space should be reserved for the IC placement if the IC thickness is thicker than the TAB film when customer design the PCB.

2. Avoid excessive bending of film when handling or designing the panel into the product

The bending of TAB/COF/FPC has to follow the precautions indicated in the specification, extra bending or excessive extraneous forces should be avoided to minimize the chances of film damage. If bending the film is necessary, please bend the designated bending area only. Please refer to items 8 and 9 of Precautions for Handling for more information.

Precautions for Storage and Reliability Test

1. Storage

Store the packed cartons or packages at 25℃±5℃, 55%±10%RH. Do not store the OLED module under direct sunlight or UV light. For best panel performance, unpack the cartons and start the production of the panels within six months after the reception of them.

2. Reliability Test

USMP only guarantees the reliability of the OLEDs under the test conditions and durations listed in the specification.