

# TFT SPECIFICATION

Part Number	USMP-T500-384216NBQ-A0
Size	50"
Resolution	4K2K (3840 x 2160)
Brightness	500 nits
Contrast	4000:1
Viewing Angle	89/89/89/89
Operating Temp.	0 ~ 50°C

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Issue Date	Approved by (customer use)	Checked by	Prepared by

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### REVISION HISTORY

Version	Date	Page(New)	Section	Description
Ver. 2.0	Jul.20.2015	All	All	The Approval specification was been released.
Ver. 2.1	Aug.25.2015	1		Revision
Ver. 2.2	Sep.11.2015	1		Revision
Ver. 2.3	Sep.16.2015	44	11	MECHANICAL CHARACTERISTIC
Ver. 2.4	Dec.09.2015	44	11	MECHANICAL CHARACTERISTIC
Ver. 2.5	Jan.15.2016	1,34	7.1	Modify Module Brightness

## 1. GENERAL DESCRIPTION

### 1.1 OVERVIEW

USMP-T500-384216NBQ-A0 is a 50" TFT Liquid Crystal Display PID module with LED Backlight unit and 8Lane V-by-one interface. This module supports 3840 x 2160 Quad HD TV format and can display true 1.07G colors (8-bit+FRC /color). The driving board module for backlight is built-in.

### 1.2 FEATURES

- High brightness (500 nits)
- High contrast ratio (4000:1)
- Fast response time (Gray to gray average 9.5 ms)
- High color saturation (NTSC 88%)
- Quad Full HDTV (3840 x 2160 pixels) resolution, true Quad Full HDTV format
- DE (Data Enable) only mode
- V-by-one interface
- Optimized response time for 50 Hz /60Hz frame rate
- Ultra wide viewing angle : Super MVA technology
- Viewing Angle : 178(H)/178(V) (CR ≥ 10) VA Technology
- RoHs compliance
- T-con input frame rate : FHD 50/60Hz, FHD 100/120Hz, QFHD 24/30Hz or QFHD 50/60Hz,  
Output frame rate: QFHD 50/60Hz

\*: The detail setting such as I2C command or timing requirement in FHD/QFHD is specified in USMP application note. It's important and necessary to follow the specification either in product SPEC or application note, otherwise it may lead to abnormal or no display. USMP application note would be provided by USMP in the design-in stage.

### 1.3 APPLICATION

- Standard Living Room TVs
- Public Display Application
- Home Theater Application
- MFM Application

### 1.4 GENERAL SPECIFICATIONS

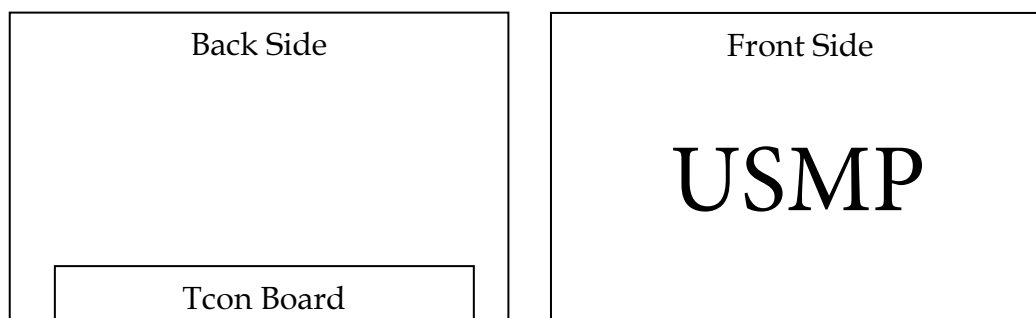
Item	Specification	Unit	Note
Active Area	1095.84(H) x 616.41(V) (50" diagonal)	mm	(1)
Bezel Opening Area	1103.04(H) x 622.41(V)	mm	
Driver Element	a-si TFT active matrix	-	-
Pixel Number	3840 x R.G.B. x 2160	pixel	-
Pixel Pitch(Sub Pixel)	0.0951(H)x0.2854(V)	mm	-
Pixel Arrangement	RGB vertical stripe	-	-
Display Colors	1.07G colors (8-bit+FRC)	color	
Display Operation Mode	Transmissive mode / Normally Black	-	-

Surface Treatment	Anti-Glare coating (Haze 1%)	-	(2)
Rotation Function	Unachievable		(3)
Display Orientation	Signal input with "USMP"		(3)

Note (1) Please refer to the attached drawings in chapter 9 for more information about the front and back outlines.

Note (2) The spec. of the surface treatment is temporarily for this phase. USMP reserves the rights to change this

feature. Note (3)



## 1.5 MECHANICAL SPECIFICATIONS

Item		Min.	Typ.	Max.	Unit	Note
Module Size	Horizontal (H)	1113.84	1115.04	1116.24	mm	(1)
	Vertical (V)	637.21	638.41	639.61	mm	(1)
	Depth (D)	(24.2)	(25.2)	(26.2)	mm	(2)
	Depth (D)	(28.9)	(29.9)	(30.9)	mm	(3)
Weight		11400	12000	12600	g	-

Note (1) Please refer to the attached drawings for more information of front and back outline dimensions.

Note (2) Module Depth is between bezel to T-CON cover.

Note (3) Module Depth is between bezel to Converter cover

## 2. ABSOLUTE MAXIMUM RATINGS

### 2.1 ABSOLUTE RATINGS OF ENVIRONMENT

Item	Symbol	Value		Unit	Note
		Min.	Max.		
Storage Temperature	TST	-20	+60	°C	(1)
Operating Ambient Temperature	TOP	0	50	°C	(1), (2)
Shock (Non-Operating)	SNOP	-	35	G	(3), (5)
Vibration (Non-Operating)	VNOP	-	1.0	G	(4), (5)

Note (1) Temperature and relative humidity range is shown in the figure below.

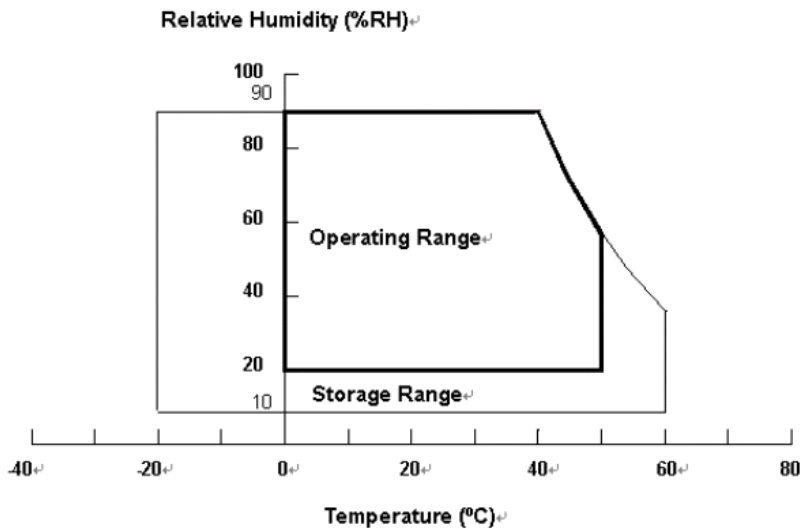
- (a) 90 %RH Max. ( $T_a \leq 40\text{ }^\circ\text{C}$ )
- (b) Wet-bulb temperature should be  $39\text{ }^\circ\text{C}$  Max.
- (c) No condensation.

Note (2) Thermal management should be considered in final product design to prevent the surface temperature of display area from being over  $65\text{ }^\circ\text{C}$ . The range of operating temperature may degrade in case of improper thermal management in final product design.

Note (3) 11 ms, half sine wave, 1 time for  $\pm X$ ,  $\pm Y$ ,  $\pm Z$ .

Note (4) 10 ~ 200 Hz, 30 min, 1 time each X, Y, Z.

Note (5) At testing Vibration and Shock, the fixture in holding the module has to be hard and rigid enough so that the module would not be twisted or bent by the fixture.



## 2.2 PACKAGE STORAGE

When storing modules as spares for a long time, the following precaution is necessary.

- (a) Do not leave the module in high temperature, and high humidity for a long time, It is highly recommended to store the module with temperature from 0 to 35 °C at normal humidity without condensation.
- (b) The module shall be stored in dark place. Do not store the TFT-LCD module in direct sunlight or fluorescent light.

## 2.3 ELECTRICAL ABSOLUTE RATINGS

### 2.3.1 TFT LCD MODULE

Item	Symbol	Value		Unit	Note
		Min.	Max.		
Power Supply Voltage	VCC	-0.3	13.5	V	(1)
Logic Input Voltage	VIN	-0.3	3.6	V	

### 2.3.2 BACKLIGHT CONVERTER UNIT

Item	Symbol	Value		Unit	Note
		Min.	Max.		
Light Bar Voltage	VW	—	65	VRMS	2D Mode
Converter Input Voltage	VBL	0	30	V	(1)
Control Signal Level	—	-0.3	6	V	(1), (3)

Note (1) Permanent damage to the device may occur if maximum values are exceeded. Functional operation should be restricted to the conditions described under normal operating conditions.

Note (2) No moisture condensation or freezing.

Note (3) The control signals include On/Off Control and External PWM Control.



### 3. ELECTRICAL CHARACTERISTICS

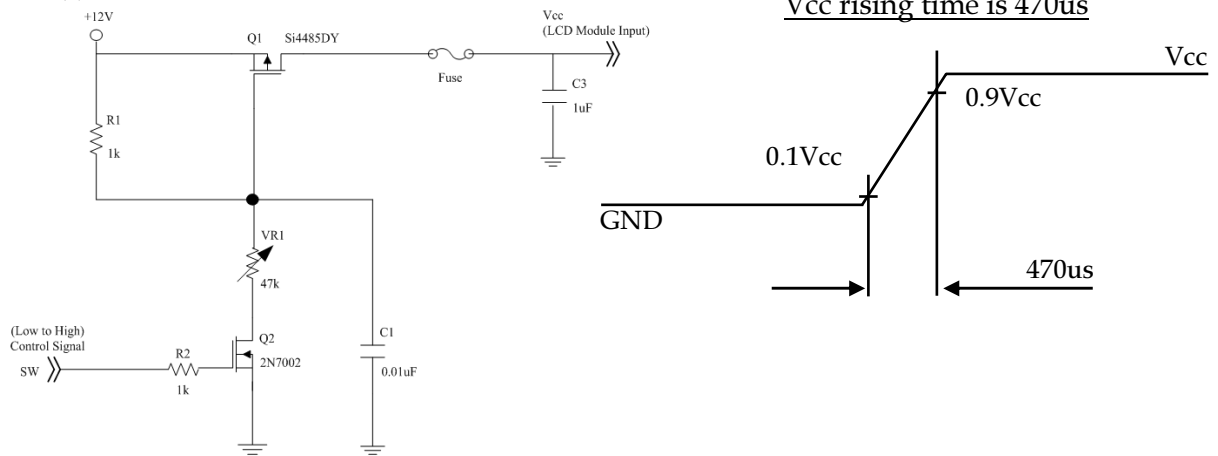
#### 3.1 TFT LCD MODULE

(Ta = 25 ± 2 °C)

Parameter		Symbol	Value			Unit	Note
			Min.	Typ.	Max.		
Power Supply Voltage		V <sub>CC</sub>	10.8	12	13.2	V	(1)
Rush Current		I <sub>RUSH</sub>	—	—	3.88	A	(2)
QFHD 120Hz Output Power Consumption	White Pattern	P <sub>T</sub>	—	14.352	15.787	W	(3)
	Horizontal Stripe	P <sub>T</sub>	—	29.946	32.94	W	
	Black Pattern	P <sub>T</sub>	—	13.938	15.33	W	
QFHD 120Hz Output Power Supply Current	White Pattern	—	—	1.196	1.312	A	
	Horizontal Stripe	—	—	2.5	2.745	A	
	Black Pattern	—	—	1.162	1.278	A	
QFHD 60Hz Output Power Consumption	White Pattern	P <sub>T</sub>	—	14.49	15.939	W	
	Horizontal Stripe	P <sub>T</sub>	—	30.222	33.244	W	
	Black Pattern	P <sub>T</sub>	—	14.214	15.635	W	
QFHD 60Hz Output Power Supply Current	White Pattern	—	—	1.208	1.328	A	
	Horizontal Stripe	—	—	2.519	2.77	A	
	Black Pattern	—	—	1.184	1.303	A	
V-by-One HS	Differential Input High Threshold Voltage	VLVTH	—	—	+50	mV	
	Differential Input Low Threshold Voltage	VLVTL	-50	—	—	mV	
CMOS interface	Input High Threshold Voltage	V <sub>IH</sub>	2.7	—	3.3	V	
	Input Low Threshold Voltage	V <sub>IL</sub>	0	—	0.7	V	

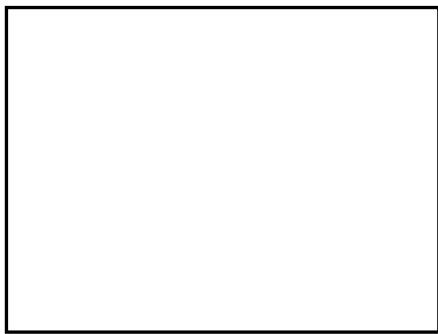
Note (1) The module should be always operated within the above ranges. The ripple voltage should be controlled under 10% of  $V_{cc}$  (Typ.)

Note (2) Measurement condition :



Note (3) The specified power supply current is under the conditions at  $V_{cc} = 12\text{ V}$ ,  $T_a = 25 \pm 2\text{ }^\circ\text{C}$ ,  $f_v = 60/120\text{ Hz}$ , whereas a power dissipation check pattern below is displayed.

a. White Pattern



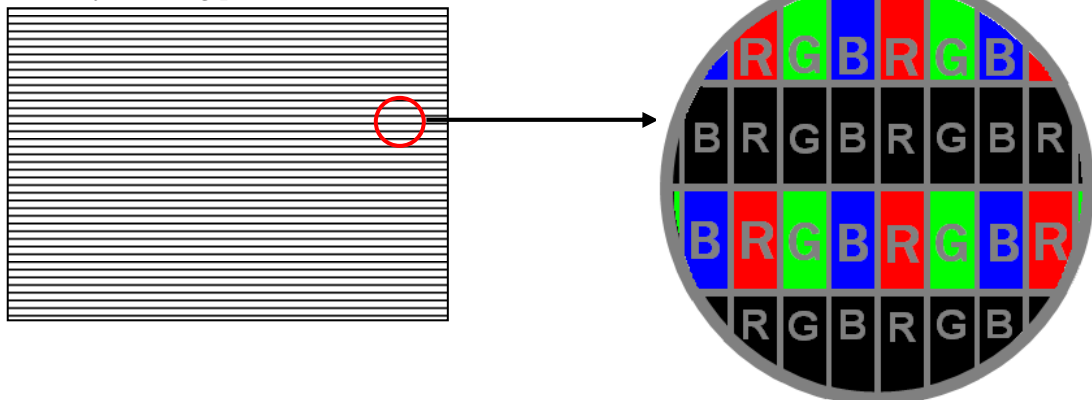
Active Area

b. Black Pattern



Active Area

c. Heavy Loading pattern



### 3.2 BACKLIGHT CONVERTER UNIT

#### 3.2.1 CONVERTER CHARACTERISTICS (Ta=25±2°C)

Parameter	Symbol	Value			Unit	Note
		Min.	Typ.	Max.		
Power Consumption	P <sub>BL</sub>	-	102.84	118.95	W	(1), (2)
Converter Input Voltage	V <sub>BL</sub>	22.8	24.0	25.2	VDC	
Converter Input Current	I <sub>BL</sub>	-	4.29	4.96	A	Non Dimming
Input Inrush Current	I <sub>R</sub>	-	-	9.5	A <sub>peak</sub>	V <sub>BL</sub> =22.8V <sub>T</sub> (3) (6)
Dimming Frequency	FB	150	160	170	Hz	(5)
Dimming Duty Ratio	DDR	5	-	100	%	(4) (5)
Life Time	-	30,000	-	-	Hrs	(7)

Note (1) The power supply capacity should be higher than the total converter power consumption PBL. Since the pulse width modulation (PWM) mode was applied for backlight dimming, the driving current changed as PWM duty on and off. The transient response of power supply should be considered for the changing loading when converter dimming.

Note (2) The measurement condition of Max. value is based on 50" backlight unit under input voltage 24V.

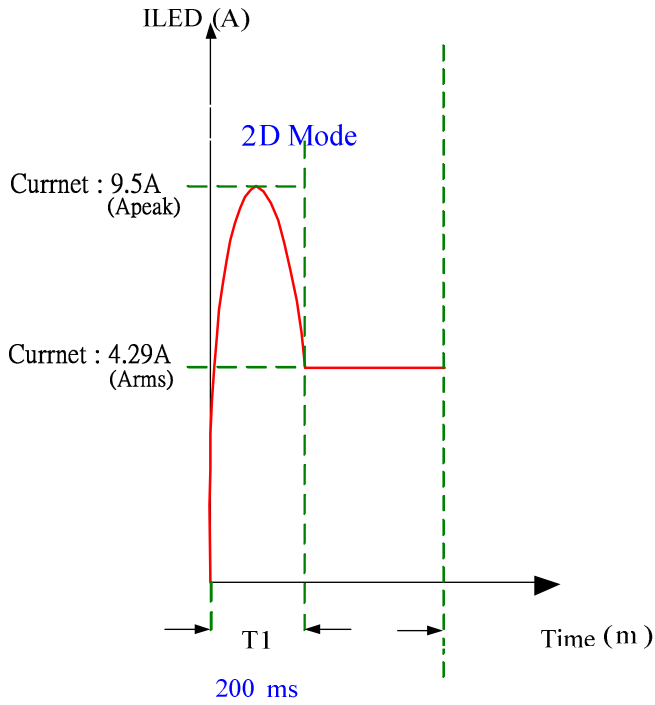
Note (3) For input inrush current measure, the VBL rising time from 10% to 90% is about 20ms.

Note (4) EPWM signal have to input available duty range. Between 97% and 100% duty (DDR) have to be avoided. (97% < DDR < 100%) But 100% duty (DDR) is possible. 5% duty (DDR) is only valid for electrical operation.

Note (5) FB and DDR are available only at 2D Mode.

Note (6) Below diagram is only for power supply design reference.

Test Condition :  $V_{BL}=22.8V$ ,  $I_L=155mA$  at 2D mode



Note (7) The lifetime is defined as the time which luminance of the LED decays to 50% compared to the initial value,  
Operating condition: Continuous operating at  $T_a = 25\pm 2^\circ C$

### 3.2.2 CONVERTER INTERFACE CHARACTERISTICS

Parameter	Symbol	Test Condition	Value			Unit	Note		
			Min.	Typ.	Max.				
On/Off Control Voltage	ON	VBLON	—	2.0	—	5.0	V		
	OFF		—	0	—	0.8	V		
External PWM Control Voltage	HI	VEPWM	—	2.0	—	5.25	V	Duty on	(5) (6)
	LO		—	0	—	0.8	V	Duty off	
External PWM Frequency	F <sub>EPWM</sub>	—	150	160	170	Hz	Normal mode (7)		
Error Signal	ERR	—	—	—	—	—	Abnormal: Open		
VBL Rising Time	Tr1	—	20	—	—	ms	10%-90% V <sub>BL</sub>		
Control Signal Rising Time	Tr	—	—	—	100	ms			
Control Signal Falling Time	Tf	—	—	—	100	ms			
PWM Signal Rising Time	TPWMR	—	—	—	50	us	(6)		
PWM Signal Falling Time	TPWFM	—	—	—	50	us			
Input Impedance	R <sub>in</sub>	—	1	—	—	MΩ	EPWM, BLON		
PWM Delay Time	TPWM	—	100	—	—	ms	(6)		
BLON Delay Time	T <sub>on</sub>	—	300	—	—	ms			
	T <sub>on1</sub>	—	300	—	—	ms			
BLON Off Time	Toff	—	300	—	—	ms			

Note (1) The Dimming signal should be valid before backlight turns on by BLON signal. It is inhibited to change the external PWM signal during backlight turn on period.

Note (2) The power sequence and control signal timing are shown in the Fig.1. For a certain reason, the converter has a possibility to be damaged with wrong power sequence and control signal timing.

Note (3) While system is turned ON or OFF, the power sequences must follow as below descriptions:

Turn ON sequence: VBL → PWM signal → BLON

Turn OFF sequence: BLOFF → PWM signal → VBL

Note (4) When converter protective function is triggered, ERR will output open collector status. (Fig.2)

Note (5) The EPWM interface that inserts a pull up resistor to 5V in Max Duty (100%), please refers to Fig.3.

Note (6) EPWM is available only at 2D Mode.

Note (7) EPWM signal have to input available frequency range.

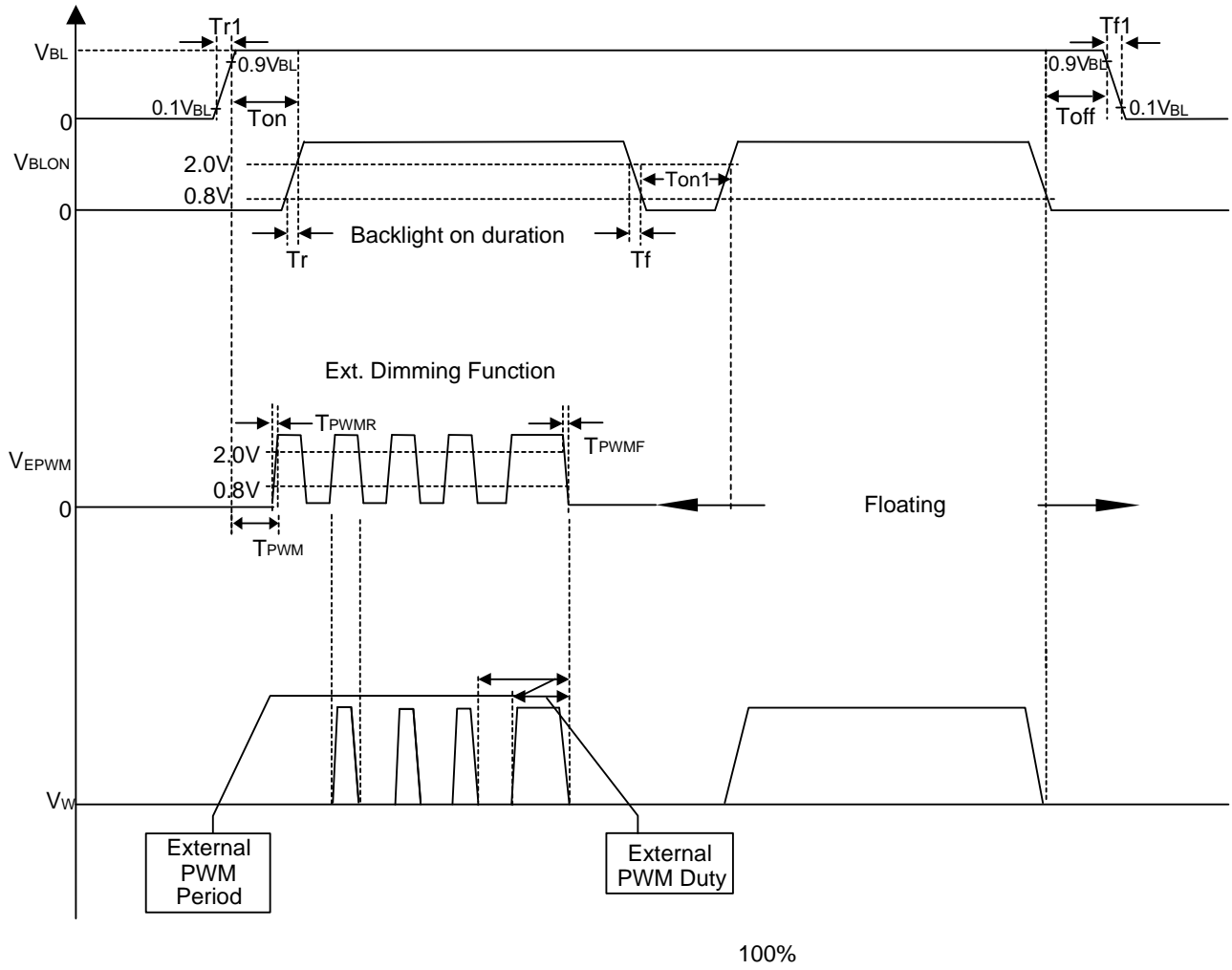


Fig. 1

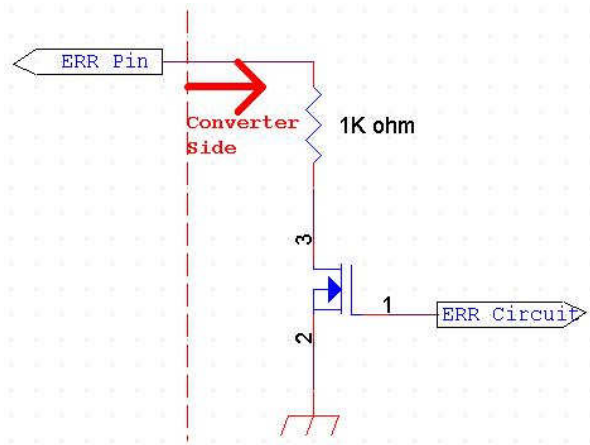


Fig. 2

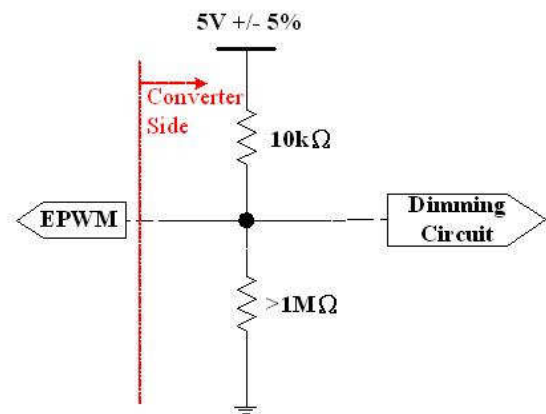
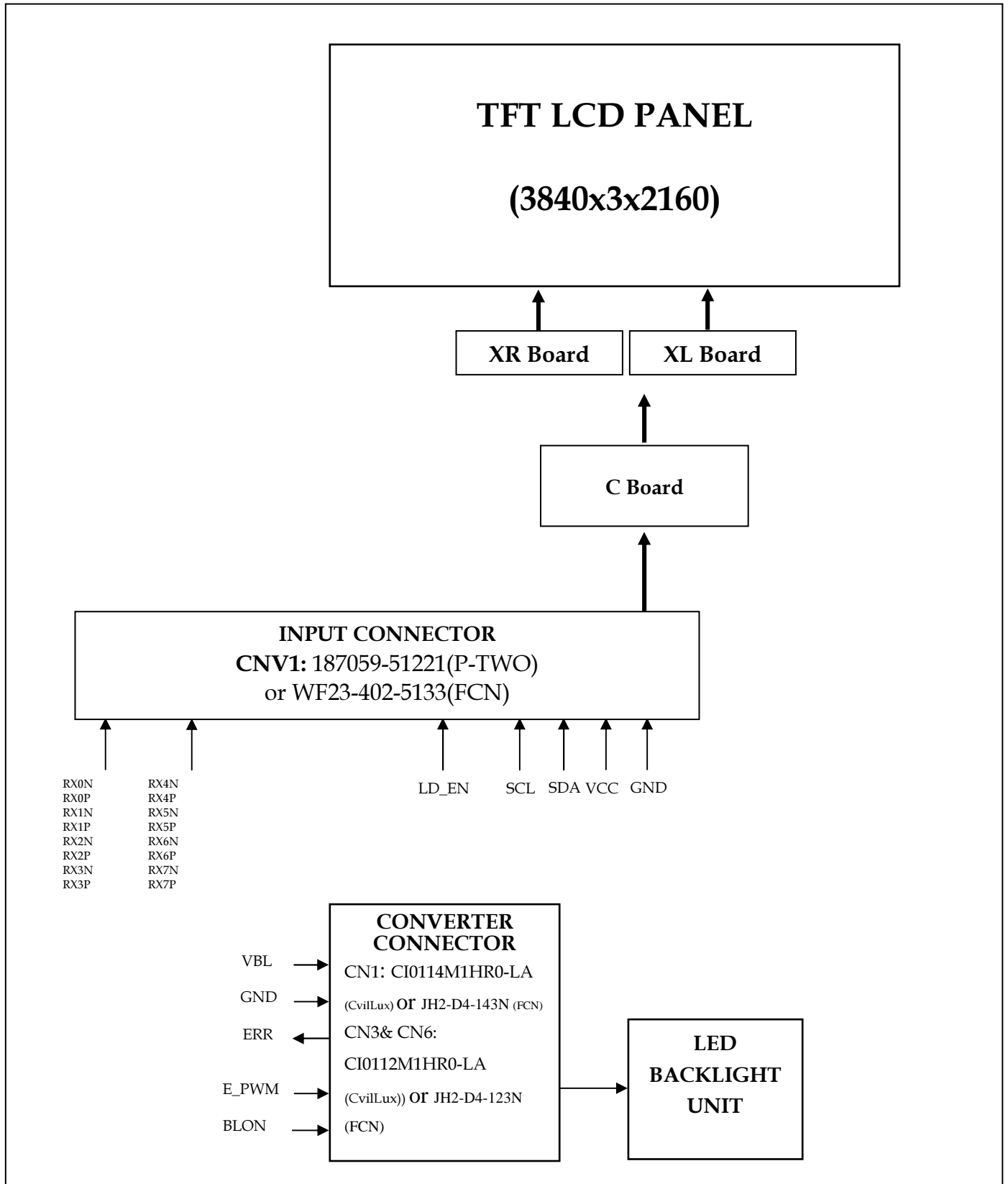


Fig. 3

#### 4. BLOCK DIAGRAM OF INTERFACE

##### 4.1 TFT LCD MODULE



## 5. INTERFACE PIN CONNECTION

### 5.1 TFT LCD MODULE

CNV1 Connector Pin Assignment (187059-51221(P-TWO) or WF23-402-5133(FCN))

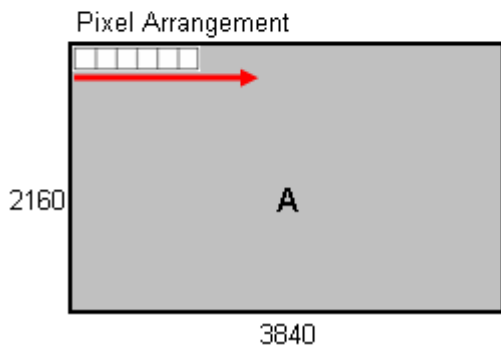
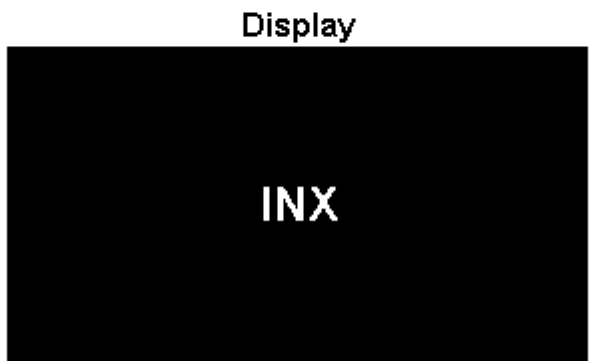
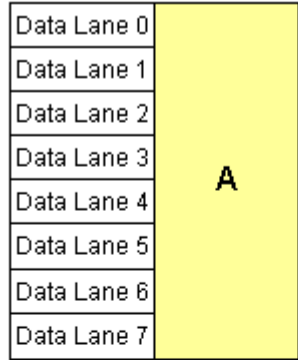
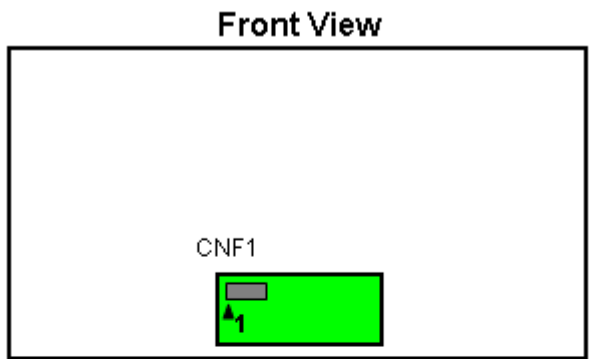
Pin	Name	Description	Note
1	Vin	Power input (+12V)	
2	Vin	Power input (+12V)	
3	Vin	Power input (+12V)	
4	Vin	Power input (+12V)	
5	Vin	Power input (+12V)	
6	Vin	Power input (+12V)	
7	Vin	Power input (+12V)	
8	Vin	Power input (+12V)	
9	N.C.	No Connection	(7)
10	GND	Ground	
11	GND	Ground	
12	GND	Ground	
13	GND	Ground	
14	GND	Ground	
15	N.C.	No Connection	(7)
16	N.C.	No Connection	(7)
17	N.C.	No Connection	(7)
18	SDA	I2C Data signal	(8)
19	SCL	I2C Clock signal	(8)
20	N.C.	No Connection	(7)
21	N.C.	No Connection	(7)
22	LD_EN	Local Dimming Mode Enable.	(2) (3)
23	N.C.	No Connection	(7)
24	N.C.	No Connection	(7)
25	HTPDN	Hot plug detect output, Open drain.	
26	LOCKN	Lock detect output, Open drain.	
27	GND	Ground	
28	RX0N	1 <sup>ST</sup> Pixel Negative V-by-One differential data input in area A. Lane 0	(1)
29	RX0P	1 <sup>ST</sup> Pixel Positive V-by-One differential data input in area A. Lane 0	
30	GND	Ground	
31	RX1N	2 <sup>ND</sup> Pixel Negative V-by-One differential data input in area A. Lane 1	(1)
32	RX1P	2 <sup>ND</sup> Pixel Positive V-by-One differential data input in area A. Lane 1	
33	GND	Ground	
34	RX2N	3 <sup>RD</sup> Pixel Negative V-by-One differential data input in area A. Lane 2	(1)
35	RX2P	3 <sup>RD</sup> Pixel Positive V-by-One differential data input in area A. Lane 2	
36	GND	Ground	



37	RX3N	4 <sup>TH</sup> Pixel Negative V-by-One differential data input in area A. Lane 3	(1)
38	RX3P	4 <sup>TH</sup> Pixel Positive V-by-One differential data input in area A. Lane 3	
39	GND	Ground	
40	RX4N	5 <sup>TH</sup> Pixel Negative V-by-One differential data input in area A. Lane 4	(1)
41	RX4P	5 <sup>TH</sup> Pixel Positive V-by-One differential data input in area A. Lane 4	
42	GND	Ground	
43	RX5N	6 <sup>TH</sup> Pixel Negative V-by-One differential data input in area A. Lane 5	(1)
44	RX5P	6 <sup>TH</sup> Pixel Positive V-by-One differential data input in area A. Lane 5	
45	GND	Ground	
46	RX6N	7 <sup>TH</sup> Pixel Negative V-by-One differential data input in area A. Lane 6	(1)
47	RX6P	7 <sup>TH</sup> Pixel Positive V-by-One differential data input in area A. Lane 6	
48	GND	Ground	
49	RX7N	8 <sup>TH</sup> Pixel Negative V-by-One differential data input in area A. Lane 7	(1)
50	RX7P	8 <sup>TH</sup> Pixel Positive V-by-One differential data input in area A. Lane 7	
51	GND	Ground	

Note (1) V-by-One<sup>R</sup> HS Data Mapping

Area	Lane	Data Stream
A	Lane 0	1, 9, 17, ....., 3825, 3833
	Lane 1	2, 10, 18, ....., 3826, 3834
	Lane 2	3, 11, 19, ....., 3827, 3835
	Lane 3	4, 12, 20, ....., 3828, 3836
	Lane 4	5, 13, 21, ....., 3829, 3837
	Lane 5	6, 14, 22, ....., 3830, 3838
	Lane 6	7, 15, 23, ....., 3831, 3839
	Lane 7	8, 16, 24, ....., 3832, 3840



Note (2) Local dimming enable selection. (Default: enable)

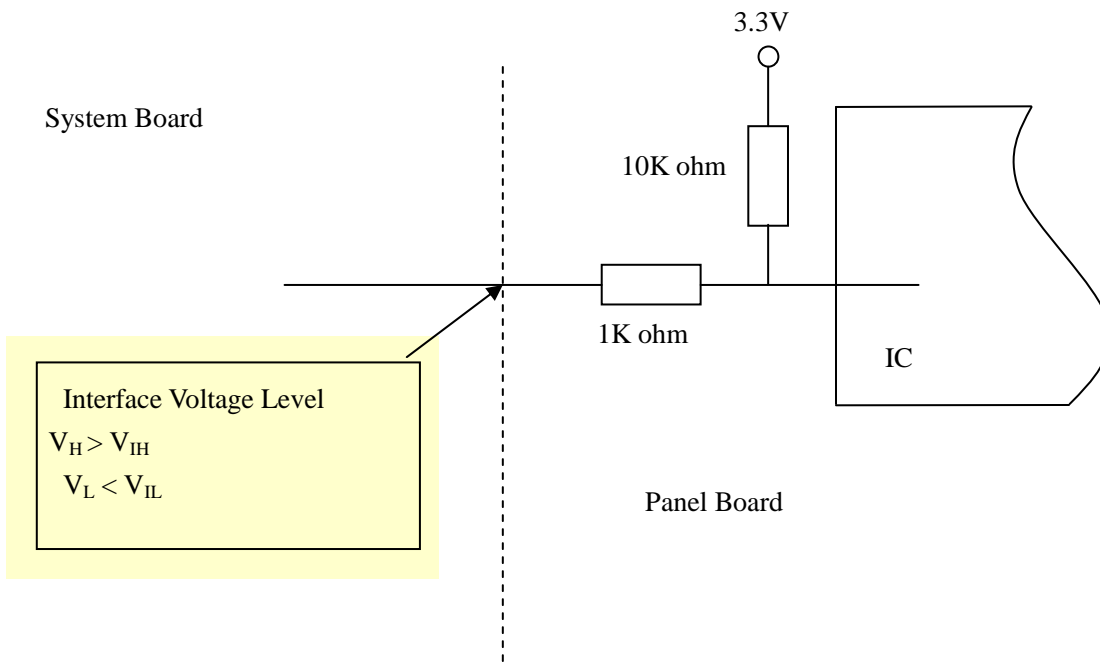
L= Connect to GND, H=Connect to +3.3V or Open

LD_EN	Note
L	Local Dimming Disable
H or Open	Local Dimming Enable

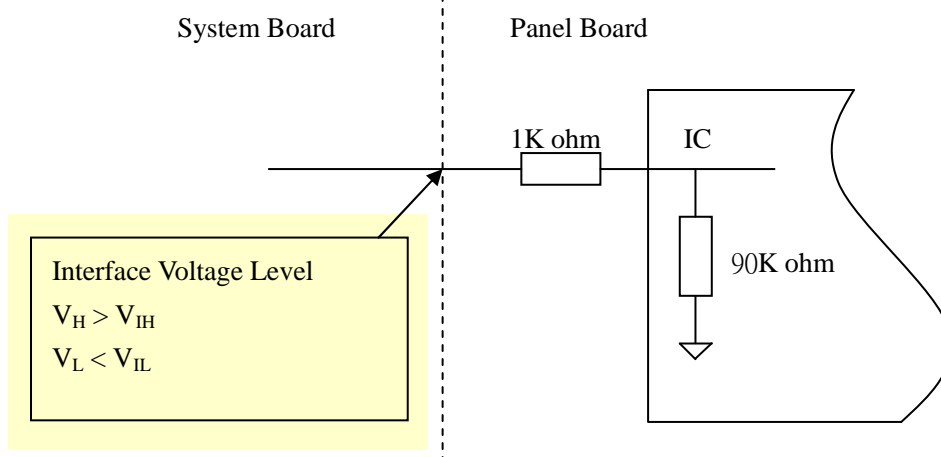
LD\_EN enable pin should be set in power on stage.

Backlight should be turned off in the period of changing original setting after power on.

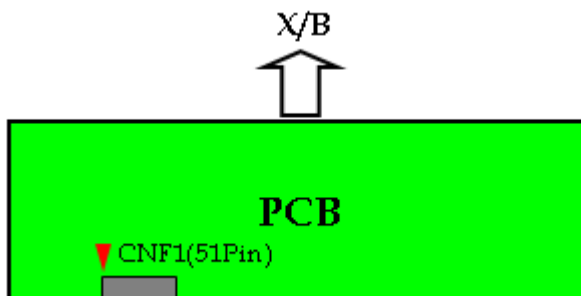
Note (3) Interface optional pin has internal scheme as following diagram. Customer should keep the interface voltage level requirement which including Panel board loading as below.



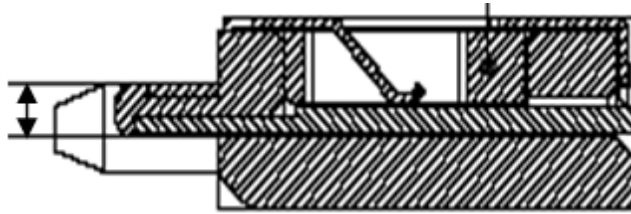
Note (4) Interface optional pin has internal scheme as following diagram. Customer should keep the interface voltage level requirement which including Panel board loading as below.



Note (5) V-by-One HS connector pin order defined as follows



Note (6) V-by-One connector mating dimension range request is 0.93mm~1.0mm as below.



Note (7) Reserved for internal use. Please leave it open.

Note (8) The detail setting such as I2C command or timing requirement in FHD/QFHD is specified in USMP application note. It's important and necessary to follow the specification either in product SPEC or application note, otherwise it may lead to abnormal or no display. USMP application note would be provided by USMP in the design-in stage.

## 5.2 BACKLIGHT UNIT

The pin configuration for the housing and the lead wire is shown in the table below.

CN3 & CN6

Connector Type : JH2-D4-123N(FCN) or CI0112M1HR0-LA(Cvilux)

Pin No.	Symbol	Description
1	N-	Negative of LED string
2	N-	
3	N-	
4	N-	
5	N-	
6	N-	
7	NC	NC
8	NC	NC
9	NC	NC
10	NC	NC
11	VLED+	Positive of LED string
12	VLED+	

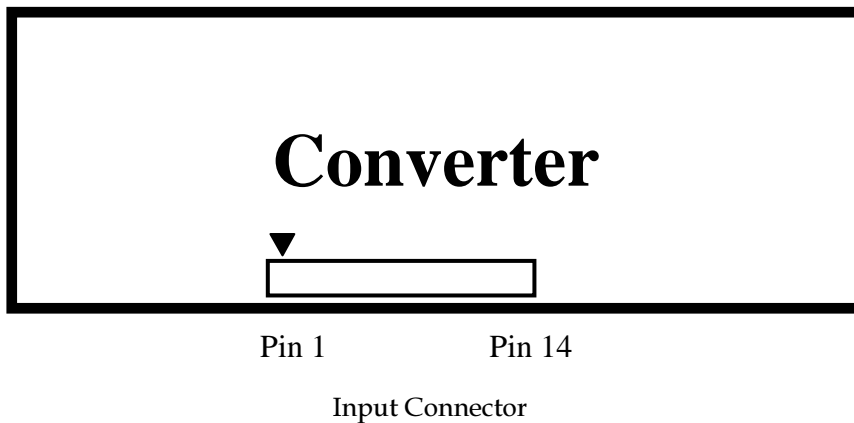
### 5.3 CONVERTER UNIT

CN1(Header): CI0114M1HR0-LA (CvilLux) or JH2-D4-143N (FCN)

Pin No	Symbol	Feature
1	VBL	+24V
2		
3		
4		
5		
6	GND	GND
7		
8		
9		
10		
11	ERR	Normal (GND) Abnormal (Open collector)
12	BLON	BL ON/OFF
13	NC	NC
14	E_PWM	External PWM Control

Note (1) If Pin14 is open, E\_PWM is 100% duty.

Note (2) Input connector pin order defined as follows



## 5.4 COLOR DATA INPUT ASSIGNMENT

The brightness of each primary color (red, green and blue) is based on the 10-bit gray scale data input for the color. The higher the binary input the brighter the color. The table below provides the assignment of color versus data input.

Color		Data Signal																																						
		Red										Green										Blue																		
		R9	R8	R7	R6	R5	R4	R3	R2	R1	R0	G9	G8	G7	G6	G5	G4	G3	G2	G1	G0	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0									
Basic Colors	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Green	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0
	Blue	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1
	Cyan	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
	Magenta	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1
	Yellow	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0
	White	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Gray Scale Of Red	Red (0) / Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
	Red (1)	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
	Red (2)	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	
	Red (1021)	1	1	1	1	1	1	1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
	Red (1022)	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
Red (1023)	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0		
Gray Scale Of Green	Green (0) / Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
	Green (1)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	
	Green (2)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	
	Green (1021)	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	
	Green (1022)	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	
Green (1023)	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0		
Gray Scale Of Blue	Blue (0) / Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
	Blue (1)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	
	Blue (2)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	
Blue (1021)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	0		
Blue (1022)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	0		
Blue (1023)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1		

Note (1) 0: Low Level Voltage , 1: High Level Voltage

## 6. INTERFACE TIMING

### 6.1 INPUT SIGNAL TIMING SPECIFICATIONS

The input signal timing specifications are shown as the following table and timing diagram. ( $T_a = 25 \pm 2 \text{ }^\circ\text{C}$ )

Signal	Item	Symbol	Min.	Typ.	Max.	Unit	Note
Frequency	Data Clock	1/Tc	69	74.25	79	MHZ	(1)
V-by-One Receiver	Intra-Pair skew		-0.3	—	0.3	UI	(2)
	Inter-pair skew		-5	—	5	UI	(3)
	Spread spectrum modulation range	$F_{\text{elkin\_mod}}$	1/Tc-0.5%	—	1/Tc+0.5%	MHz	(4)
	Spread spectrum modulation frequency	$F_{\text{SSM}}$	—	—	30	KHz	

#### 6.1.1 Input Timing spec for QFHD Frame Rate = 50Hz

Signal	Item	Symbol	Min.	Typ.	Max.	Unit	Note	
Frame Rate	2D Mode	$F_r$	49	50	51	Hz	(5),(6)	
Vertical Active Display Term (8 Lane,3840X2160 Active Area)	2D Mode	Total	$T_v$	2200	2700	2790	Th	$T_v=T_{vd}+T_{vb}$
		Display	$T_{vd}$	2160			Th	
		Blank	$T_{vb}$	40	540	630	Th	
Horizontal Active Display Term (8 Lane,3840X2160 Active Area)	2D Mode	Total	$T_h$	530	550	590	Tc	$T_h=T_{hd}+T_{hb}$
		Display	$T_{hd}$	480			Tc	
		Blank	$T_{hb}$	50	70	110	Tc	

#### 6.1.2 Input Timing spec for QFHD Frame Rate = 60Hz

Signal	Item	Symbol	Min.	Typ.	Max.	Unit	Note	
Frame Rate	2D Mode	$F_r$	59	60	61	Hz	(5),(6)	
Vertical Active Display Term (8 Lane,3840X2160 Active Area)	2D Mode	Total	$T_v$	2230	2250	2350	Th	$T_v=T_{vd}+T_{vb}$
		Display	$T_{vd}$	2160			Th	
		Blank	$T_{vb}$	70	90	190	Th	
Horizontal Active Display Term	2D Mode	Total	$T_h$	530	550	600	Tc	$T_h=T_{hd}+T_{hb}$



(8 Lane, 3840X2160 Active Area)	Display	Thd	480			Tc	
	Blank	Thb	50	70	120	Tc	

### 6.1.3 Input Timing Spec for FHD, Frame Rate = 50Hz

Signal	Item	Symbol	Min.	Typ.	Max.	Unit	Note	
Frame Rate	2D Mode	$F_r$	49	50	51	Hz	(5),(6)	
Vertical Active Display Term (2 Lane, 1920X1080 Active Area)	2D Mode	Total	Tv	1104	1350	1395	Th	$T_v = T_{vd} + T_{vb}$
		Display	Tvd	1080			Th	
		Blank	Tvb	24	270	315	Th	
Horizontal Active Display Term (2 Lane, 1920X1080 Active Area)	2D Mode	Total	Th	1060	1100	1150	Tc	$T_h = T_{hd} + T_{hb}$
		Display	Thd	960			Tc	
		Blank	Thb	100	140	190	Tc	

### 6.1.4 Input Timing Spec for FHD, Frame Rate = 60Hz

Signal	Item	Symbol	Min.	Typ.	Max.	Unit	Note	
Frame Rate	2D Mode	$F_r$	59	60	61	Hz	(5),(6)	
Vertical Active Display Term (2 Lane, 1920X1080 Active Area)	2D Mode	Total	Tv	1104	1125	1395	Th	$T_v = T_{vd} + T_{vb}$
		Display	Tvd	1080			Th	
		Blank	Tvb	24	45	315	Th	
Horizontal Active Display Term (2 Lane, 1920X1080 Active Area)	2D Mode	Total	Th	1060	1100	1150	Tc	$T_h = T_{hd} + T_{hb}$
		Display	Thd	960			Tc	
		Blank	Thb	100	140	190	Tc	

### 6.1.5 Input Timing Spec for FHD, Frame Rate = 100Hz

Signal	Item	Symbol	Min.	Typ.	Max.	Unit	Note	
Frame Rate	2D Mode	$F_r$	98	100	102	Hz	(5),(6)	
Vertical Active Display Term (4 Lane, 1920X1080 Active Area)	2D Mode	Total	Tv	1108	1350	1370	Th	$T_v = T_{vd} + T_{vb}$
		Display	Tvd	1080			Th	
		Blank	Tvb	28	270	290	Th	
Horizontal Active	Total	Th	530	550	650	Tc	$T_h = T_{hd} + T_{hb}$	

Display Term (4 Lane,1920X1080 Active Area)	Display	Thd	480			Tc	
	Blank	Thb	50	70	170	Tc	

#### 6.1.6 Input Timing Spec for FHD, Frame Rate = 120Hz

Signal	Item	Symbol	Min.	Typ.	Max.	Unit	Note	
Frame Rate	2D Mode	$F_r$	118	120	121	Hz	(5),(6)	
Vertical Active Display Term (4 Lane,1920X1080 Active Area)	2D Mode	Total	Tv	1108	1125	1370	Th	$Tv=Tvd+Tvb$
		Display	Tvd	1080			Th	
		Blank	Tvb	28	45	290	Th	
Horizontal Active Display Term (4 Lane,1920X1080 Active Area)	2D Mode	Total	Th	530	550	650	Tc	$Th=Thd+Thb$
		Display	Thd	480			Tc	
		Blank	Thb	50	70	170	Tc	

#### 6.1.7 Input Timing spec for QFHD, Frame Rate = 24Hz

Signal	Item	Symbol	Min.	Typ.	Max.	Unit	Note	
Frame Rate	2D Mode	$F_r$	23.5	24	24.5	Hz	(5),(6)	
Vertical Active Display Term (4 Lane,3840X2160 Active Area)	2D Mode	Total	Tv	2208	2750	3200	Th	$Tv=Tvd+Tvb$
		Display	Tvd	2160			Th	
		Blank	Tvb	48	590	1040	Th	
Horizontal Active Display Term (4 Lane,3840X2160 Active Area)	2D Mode	Total	Th	1060	1100	1180	Tc	$Th=Thd+Thb$
		Display	Thd	960			Tc	
		Blank	Thb	100	140	220	Tc	

#### 6.1.8 Input Timing spec for QFHD, Frame Rate = 30Hz

Signal	Item	Symbol	Min.	Typ.	Max.	Unit	Note	
Frame Rate	2D Mode	$F_r$	29.5	30	30.5	Hz	(5),(6)	
Vertical Active Display Term (4 Lane,3840X2160 Active Area)	2D Mode	Total	Tv	2208	2250	2450	Th	$Tv=Tvd+Tvb$
		Display	Tvd	2160			Th	
		Blank	Tvb	48	90	290	Th	
Horizontal Active Display Term	2D Mode	Total	Th	1060	1100	1180	Tc	$Th=Thd+Thb$
		Display	Thd	960			Tc	

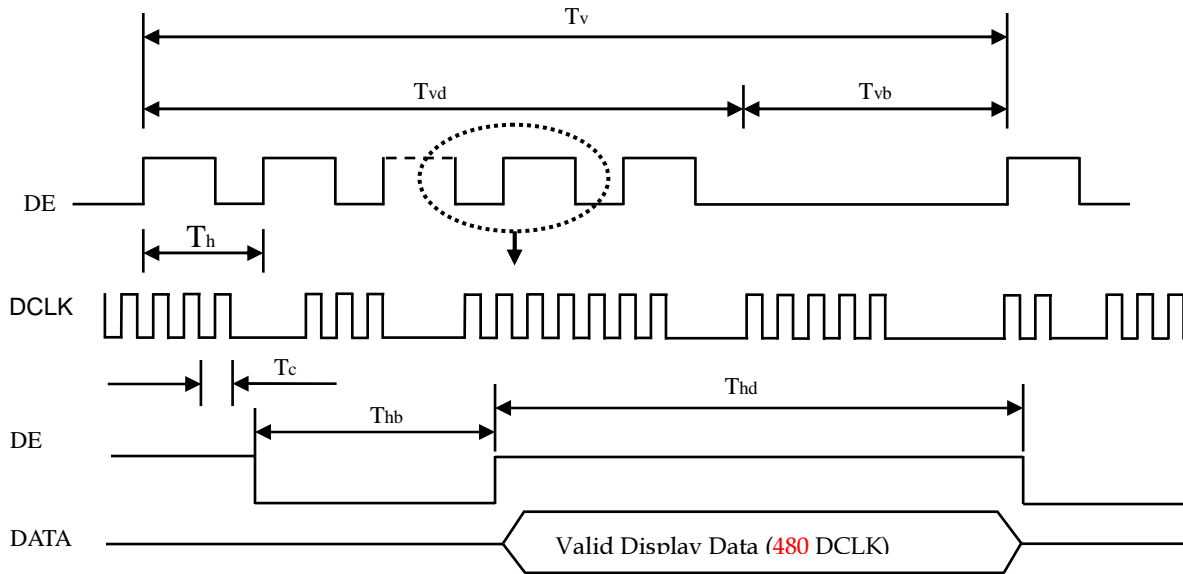
(4 Lane, 3840X2160 Active Area)		Blank	Thb	80	140	220	Tc	
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Note (1) Please make sure the range of pixel clock has follow the below equation :

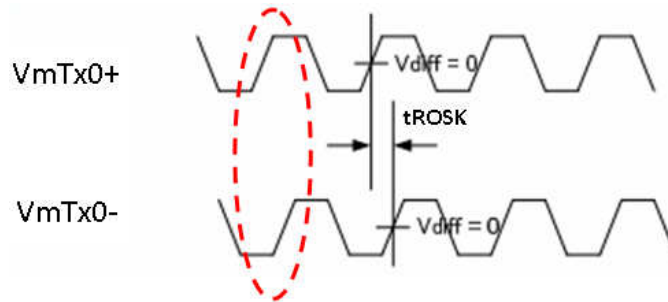
$$F_{clk}(max) \geq Fr \times Tv \times Th$$

$$Fr \times Tv \times Th \geq F_{clk}(min)$$

### INPUT SIGNAL TIMING DIAGRAM

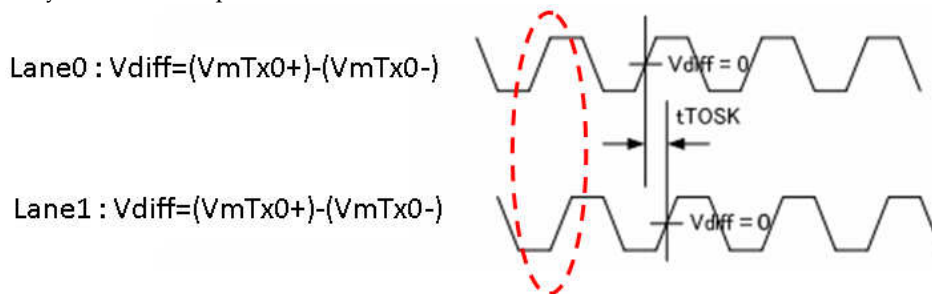


Note (2) Intra-pair Data skew



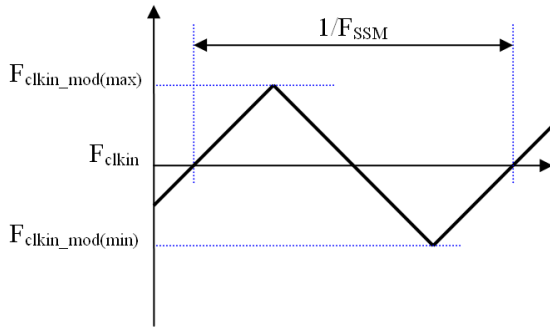
The same pair signal

Note (3) V-by-One HS Inter-pair skew.



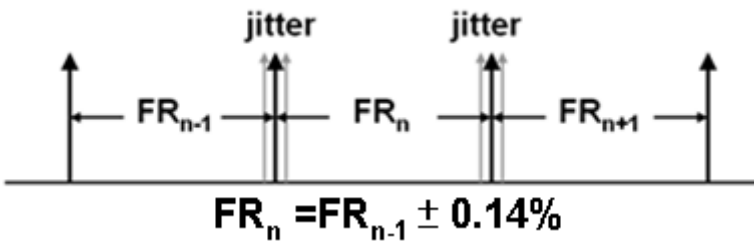
Different lanes

Note (4) The SSCG (Spread spectrum clock generator) is defined as below figures.

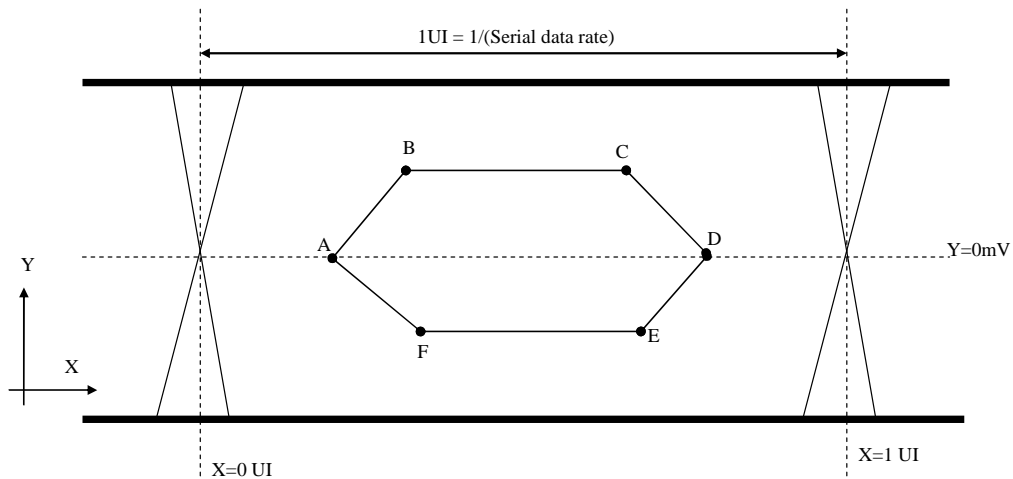


Note (5) The frame-to-frame jitter of the input frame rate is defined as the above figures.  $FR_n = FR_{n-1} \pm 0.14\%$ .

Note (6) The setup of the frame rate jitter > 0.14% may result in the cosmetic LED backlight symptom but the electric function is not affected.



**6.2 V by One Input Signal Timing Diagram**



**Table 1 Eye Mask Specification**

	X [UI]	Y [mV]	Note
A	0.25	0	(1)
B	0.3	50	(1)
C	0.7	50	(1)

D	0.75	0	(1)
E	0.7	-50	(1)
F	0.3	-50	(1)

Note (1) Input levels of V-by-One HS signals are comes from "V-by-One HS Stander Ver.1.4"

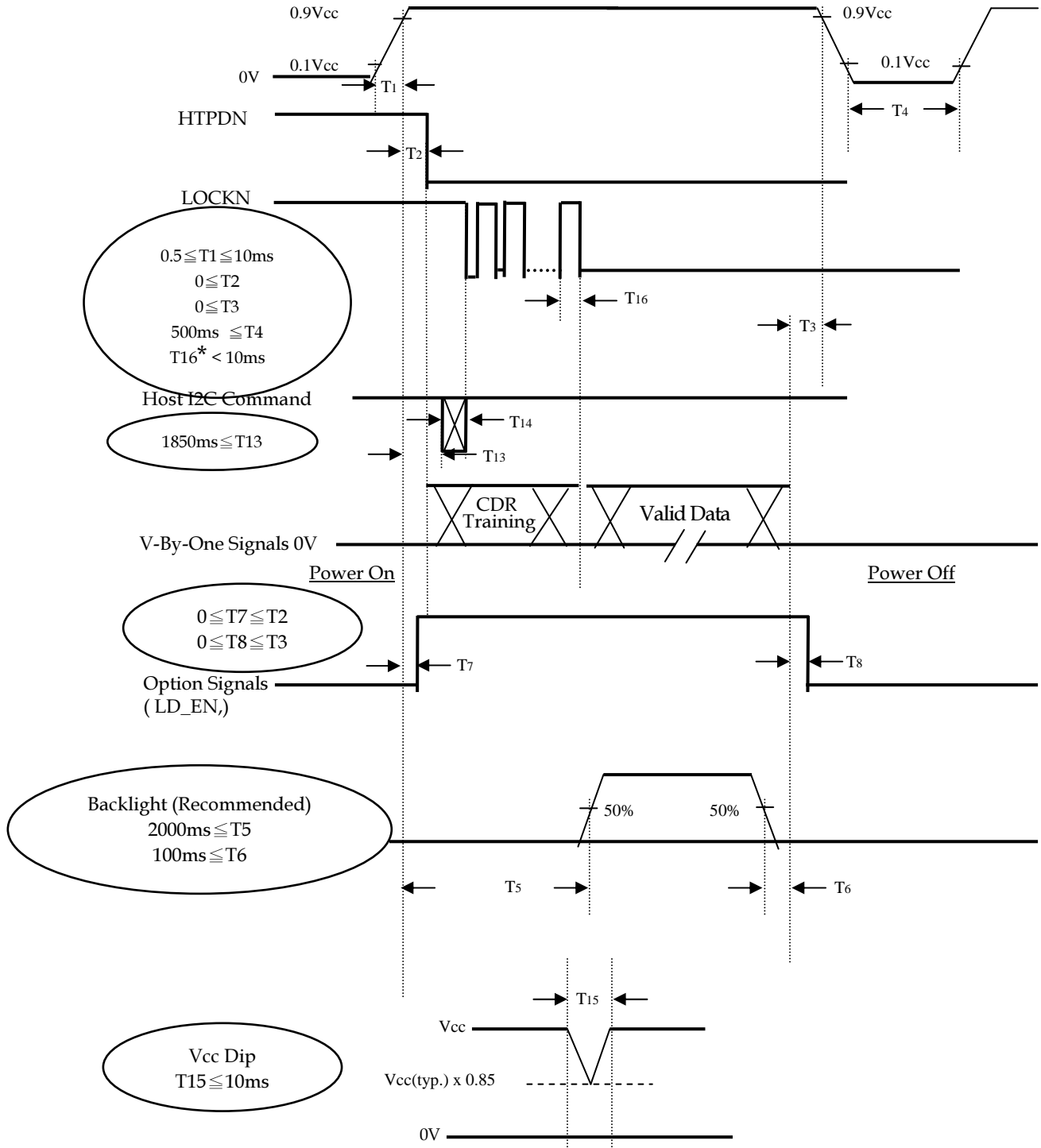
### 6.3 Byte Length and Color mapping of V-by-One HS

Packer input & Unpacker output	30bpp RGB (10bit)	
Byte 0	D[0]	R[2]
	D[1]	R[3]
	D[2]	R[4]
	D[3]	R[5]
	D[4]	R[6]
	D[5]	R[7]
	D[6]	R[8]
	D[7]	R[9]
Byte 1	D[8]	G[2]
	D[9]	G[3]
	D[10]	G[4]
	D[11]	G[5]
	D[12]	G[6]
	D[13]	G[7]
	D[14]	G[8]
	D[15]	G[9]
Byte 2	D[16]	B[2]
	D[17]	B[3]
	D[18]	B[4]
	D[19]	B[5]
	D[20]	B[6]
	D[21]	B[7]
	D[22]	B[8]
	D[23]	B[9]
Byte 3	D[24]	X
	D[25]	X
	D[26]	B[0]
	D[27]	B[1]
	D[28]	G[0]
	D[29]	G[1]
	D[30]	R[0]
	D[31]	R[1]

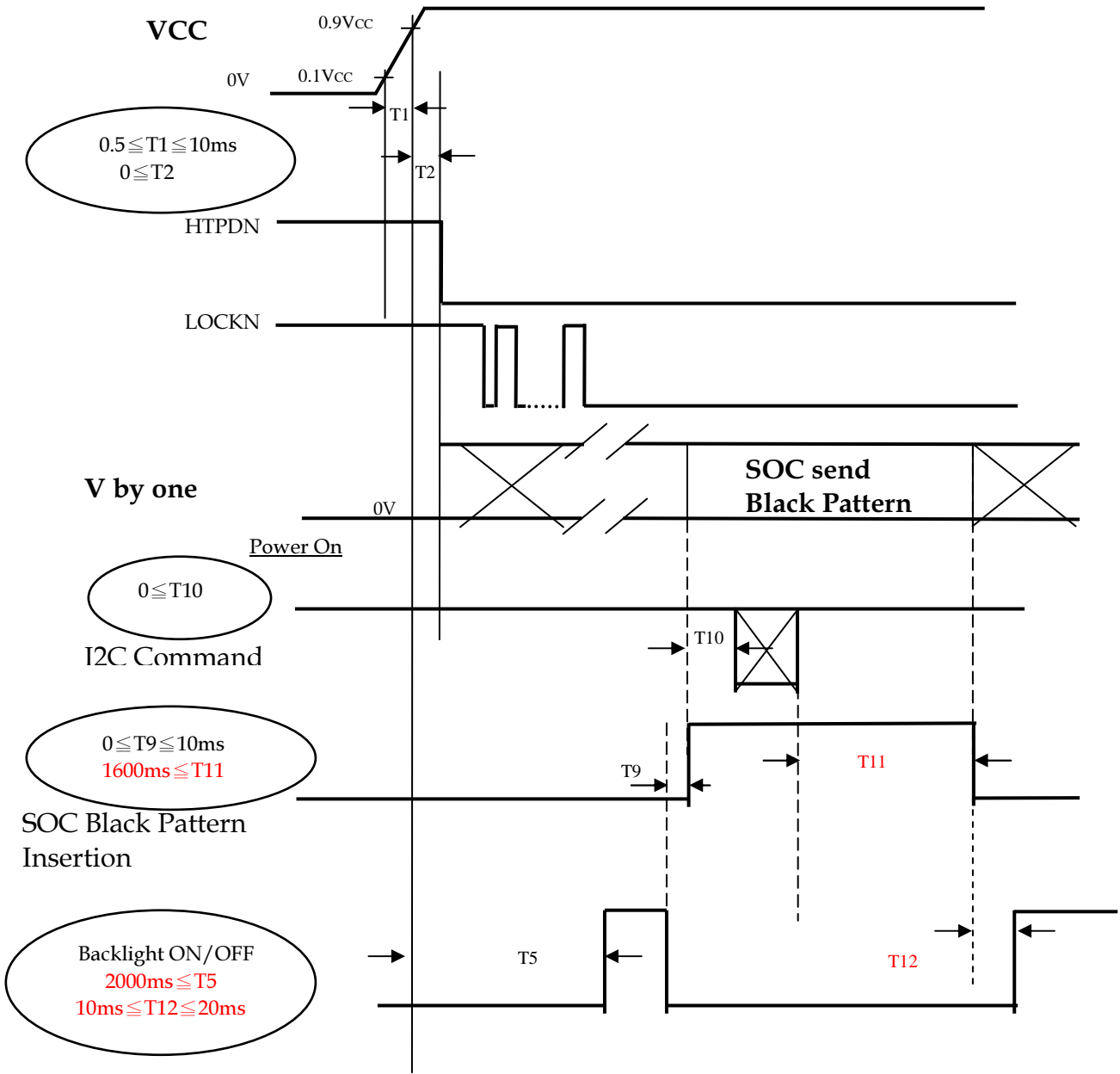
### 6.4 POWER ON/OFF SEQUENCE

( $T_a = 25 \pm 2^\circ\text{C}$ )

To prevent a latch-up or DC operation of LCD module, the power on/off sequence should be as the diagram below.



**6.5 MODE CHANGE SIGNAL SEQUENCE WITHOUT VCC TURN OFF AND TURN**



- Note (1) The supply voltage of the external system for the module input should follow the definition of Vcc.
- Note (2) Apply the LED voltage within the LCD operation range. When the backlight turns on before the LCD operation or the LCD turns off before the backlight turns off, the display may momentarily become abnormal screen.
- Note (3) In case of Vcc is in off level, please keep the level of input signals on the low or high impedance. If  $T2 < 0$ , that maybe cause electrical overstress failure.
- Note (4) T4 should be measured after the module has been fully discharged between power off and on period.
- Note (5) Interface signal shall not be kept at high impedance when the power is on.
- Note (6) Vcc must decay smoothly when power-off.
- Note (7)  $T5 > (T13 + T14)$
- Note (8) T16, V-by-One signals shall be stabilized and follows timing specification which defined by section 6.1 & 6.2
- Note (9) T11 is at least 1600ms. It is also determined by the SOC stability time. If SOC would spend some time into stable state, T11 will be stable time plus 1600ms.

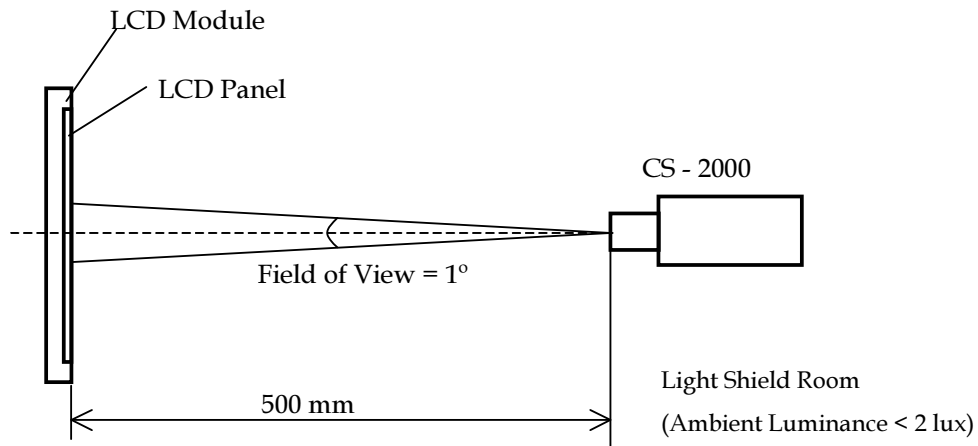


## 7. OPTICAL CHARACTERISTICS

### 7.1 TEST CONDITIONS

Item	Symbol	Value	Unit
Ambient Temperature	Ta	25±2	°C
Ambient Humidity	Ha	50±10	%RH
Supply Voltage	VCC	12±1.2	V
Input Signal	According to typical value in "3. ELECTRICAL CHARACTERISTICS"		
Vertical Frame Rate	Fr	60	Hz

The LCD module should be stabilized at given temperature for 1 hour to avoid abrupt temperature change during measuring in a windless room.



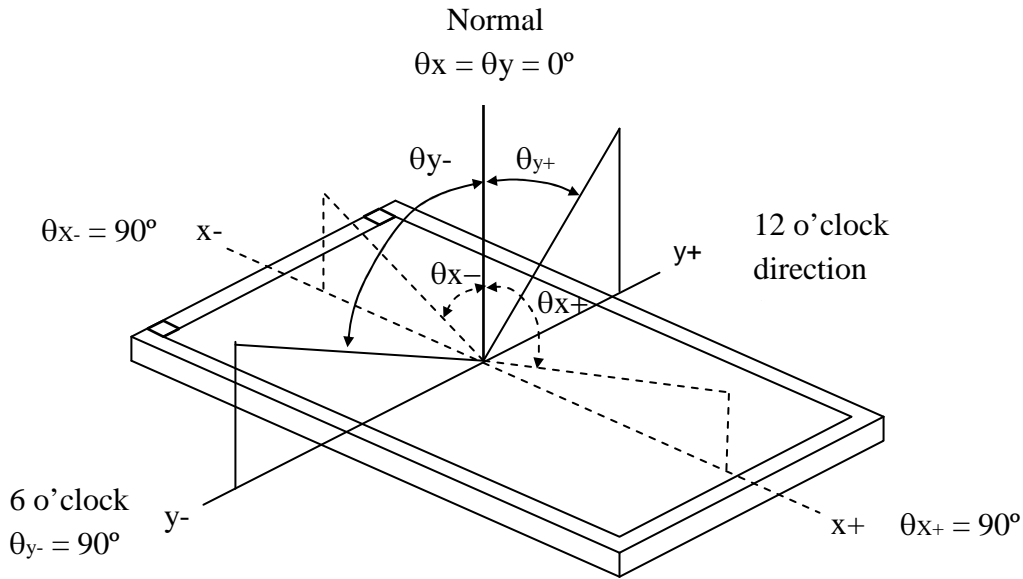
## 7.2 OPTICAL SPECIFICATIONS

The relative measurement methods of optical characteristics are shown in 7.2. The following items should be measured under the test conditions described in 7.1 and stable environment shown in 7.1.

Item		Symbol	Condition	Min.	Typ.	Max.	Unit	Note			
Contrast Ratio		CR		2800	4000		-	(2)			
Response Time (VA)		Gray to gray			9.5	19	ms	(3)			
Response Time (TN Model)		Tr					ms	(3)			
		Tf					ms	(3)			
Center Luminance of White		L <sub>c</sub>		400	500		cd/m <sup>2</sup>	(4)			
White Variation		δW				1.3	-	(6)			
Cross Talk		CT				4	%	(5)			
Color Chromaticity	Red	R <sub>x</sub>		Typ. -0.03	Typ. +0.03	0.670	-	-			
		R <sub>y</sub>				0.310	-				
	Green	G <sub>x</sub>				0.265	-				
		G <sub>y</sub>	0.651			-					
	Blue	B <sub>x</sub>	0.152			-					
		B <sub>y</sub>	0.055			-					
	White	W <sub>x</sub>	0.280			-					
		W <sub>y</sub>	0.290			-					
	Correlated color temperature					-	10000		-	K	-
	Color Gamut	C.G.	-			88	-		%	NTSC	
Viewing Angle	Horizontal	θ <sub>x+</sub>	CR≥10	80	89	-	Deg.	(1)			
		θ <sub>x-</sub>		80	89	-					
	Vertical	θ <sub>y+</sub>		80	89	-					
		θ <sub>y-</sub>		80	89	-					

Note (1) Definition of Viewing Angle ( $\theta_x, \theta_y$ ) :

Viewing angles are measured by Autronic Conoscope Cono-80 (or Eldim EZ-Contrast 160R).



Note (2) Definition of Contrast Ratio (CR) :

The contrast ratio can be calculated by the following expression.

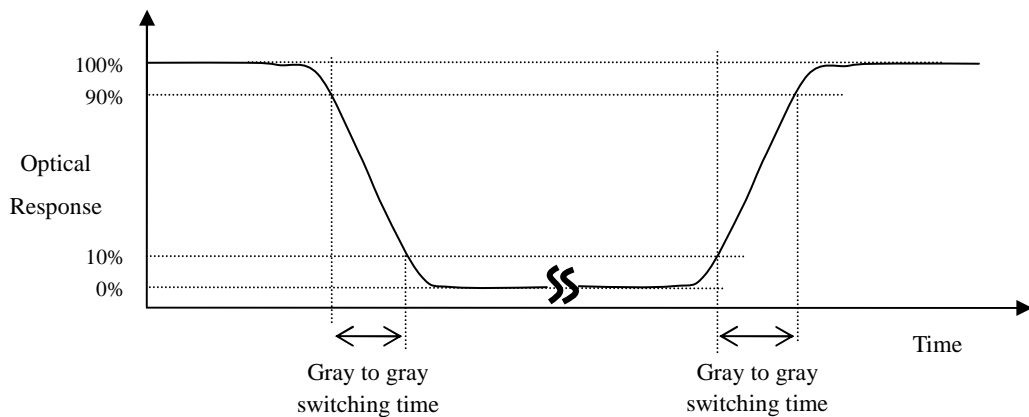
$$\text{Contrast Ratio (CR)} = \frac{\text{Surface Luminance of L1023}}{\text{Surface Luminance of L0}}$$

L255: Luminance of gray level 1023

L 0: Luminance of gray level 0

CR = CR (X), where CR (X) is corresponding to the Contrast Ratio of the point X at the figure in Note (6).

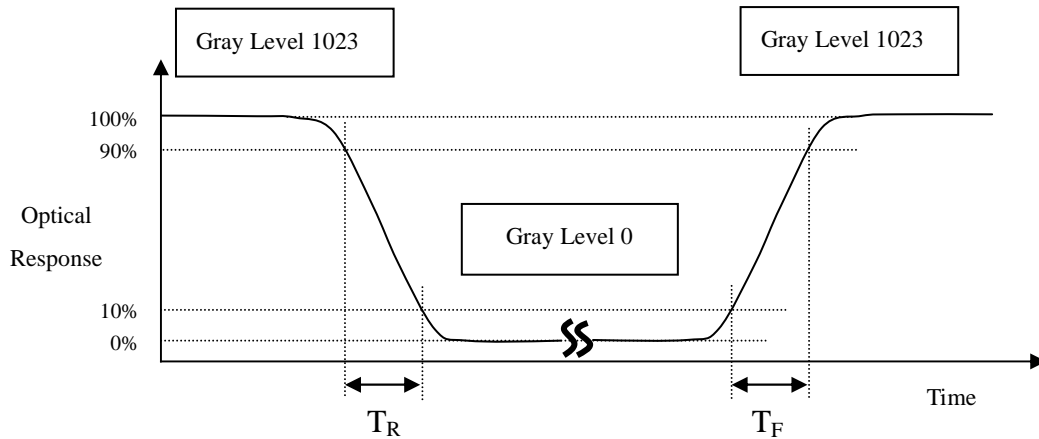
Note (3) Definition of Gray-to-Gray Switching Time : (VA Case)



The driving signal means the signal of gray level 0, 124, 252, 380, 508, 636, 764, 892 and 1023.

Gray to gray average time means the average switching time of gray level 0, 124, 252, 380, 508, 636, 764, 892 and 1023 to each other.

Note (3) Definition of Response Time ( $T_r$ ,  $T_f$ ) (TN Model) :



Note (4) Definition of Luminance of White ( $L_C$ ,  $L_{AVE}$ ) :

Measure the luminance of gray level 1023 at center point and 5 points

$L_C = L(5)$ , where  $L(X)$  is corresponding to the luminance of the point X at the figure in Note (6).

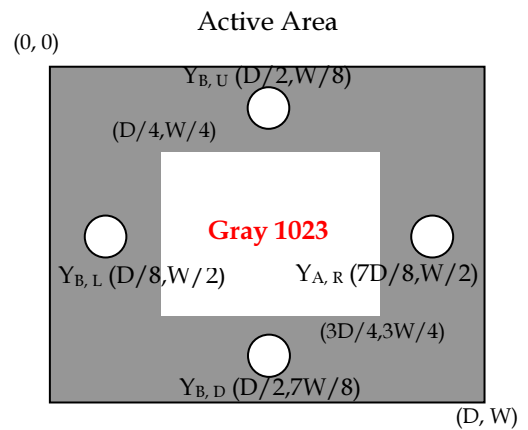
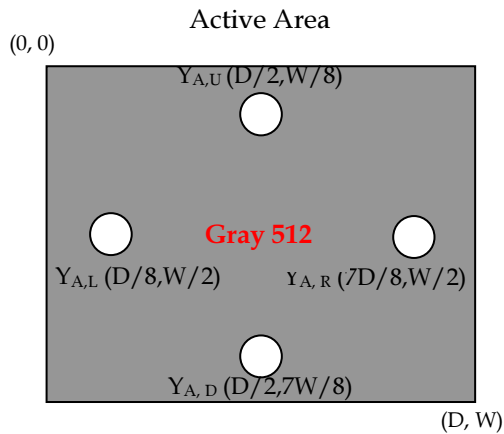
Note (5) Definition of Cross Talk (CT) : (VA Model)

$$CT = | Y_B - Y_A | / Y_A \times 100 (\%)$$

Where:

$Y_A$  = Luminance of measured location without gray level 1023 pattern (cd/m<sup>2</sup>)

$Y_B$  = Luminance of measured location with gray level 1023 pattern (cd/m<sup>2</sup>)



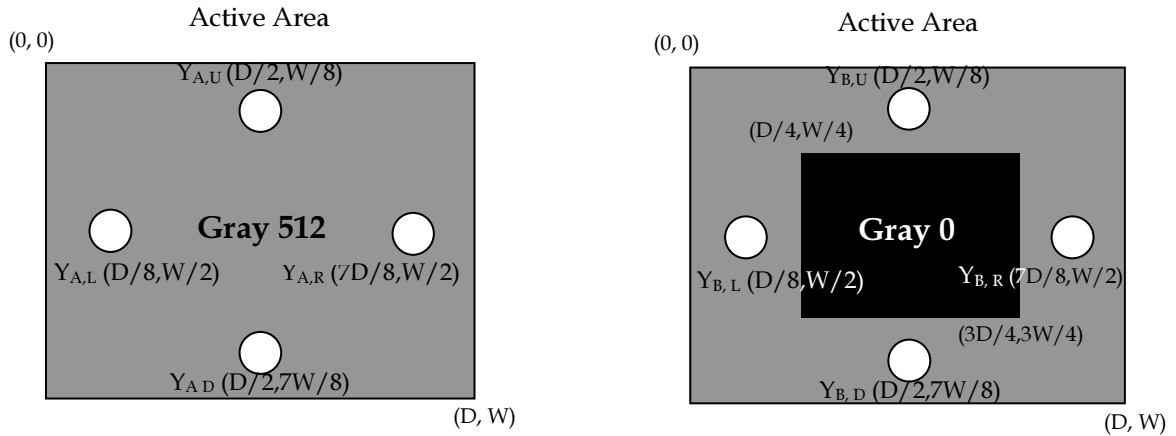
Note (5) Definition of Cross Talk (CT): (TN Model)

$$CT = | Y_B - Y_A | / Y_A \times 100 (\%)$$

Where :

Y<sub>A</sub> = Luminance of measured location without gray level 0 pattern (cd/m<sup>2</sup>)

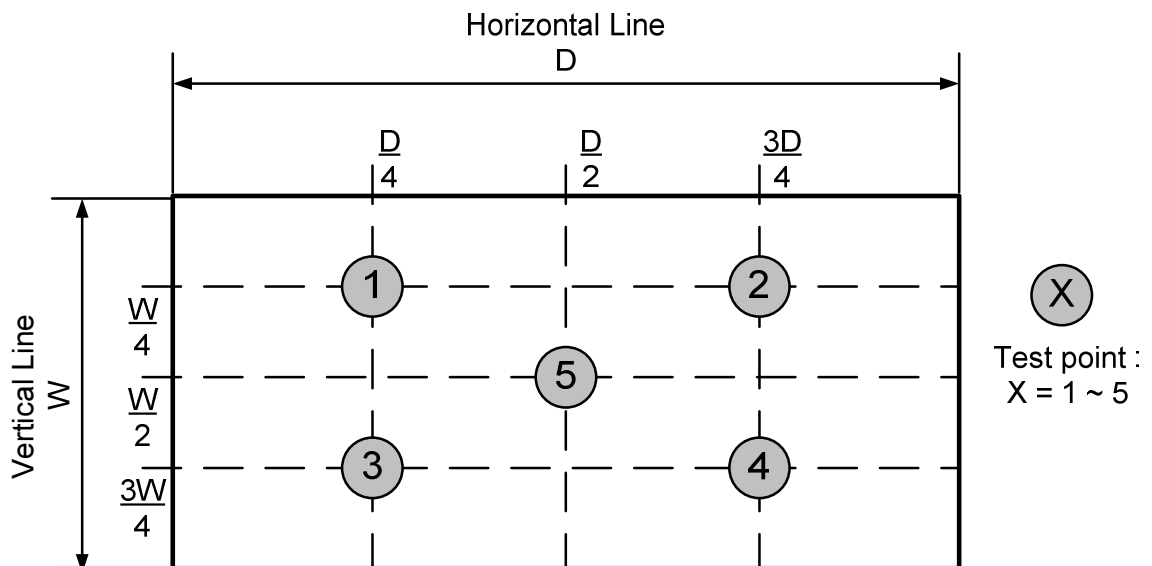
Y<sub>B</sub> = Luminance of measured location with gray level 0 pattern (cd/m<sup>2</sup>)



Note (6) Definition of White Variation ( $\delta W$ ) :

Measure the luminance of gray level 1023 at 5 points

$$\delta W = \frac{\text{Maximum [L (1), L (2), L (3), L (4), L (5)]}}{\text{Minimum [L (1), L (2), L (3), L (4), L (5)]}}$$



## 8. PRECAUTIONS

### 8.1 ASSEMBLY AND HANDLING PRECAUTIONS

- [1] Do not apply rough force such as bending or twisting to the module during assembly.
- [2] Do not apply pressure or impulse to the module to prevent the damage of LCD panel and Backlight.
- [3] Bezel of Set can not press or touch the panel surface. It will make light leakage or scrape.
- [4] It should be attached to the system firmly using all mounting holes.
- [5] It is recommended to assemble or to install a module into the user's system in clean working areas. The dust and oil may cause electrical short or worsen the polarizer, do not press or scratch the surface harder than a HB pencil lead.
- [6] Use finger-stalls with soft gloves in order to keep display clean during the incoming inspection and assembly process.
- [7] Protection film for polarizer on the module should be slowly peeled off just before use so that the electrostatic charge can be minimized.
- [8] Do not disassemble the module.
- [9] Always follow the correct power-on sequence when the LCD module is turned on. This can prevent the damage and latch-up of the CMOS LSI chips.
- [10] Do not plug in or pull out the I/F connector while the module is in operation, pins of I/F connector should not be touched directly with bare hands. Do not adjust the variable resistor located on the module.
- [11] Use a soft dry cloth without chemicals for cleaning, because the surface of polarizer is very soft and easily scratched. Water, IPA (Isopropyl Alcohol) or Hexane are desirable cleaners. Do not use Ketone type materials (ex. Acetone), Ethyl alcohol, Toluene, Ethyl acid or Methyl chloride. It might permanent damage to the polarizer due to chemical reaction.
- [12] Moisture can easily penetrate into LCD module and may cause the damage during operation.
- [13] When storing modules as spares for a long time, the following precaution is necessary.
  - [13.1] Do not leave the module in high temperature, and high humidity for a long time. It is highly recommended to store the module with temperature from 0 to 35°C at normal humidity (under 70%) without condensation.
  - [13.2] The module shall be stored in dark place. Do not store the TFT-LCD module in direct sunlight or fluorescent light.
- [14] When ambient temperature is lower than 10°C, the display quality might be reduced. For example, the response time will become slow, and the starting voltage of LED will be higher than that of room temperature.

### 8.2 SAFETY PRECAUTIONS

To optimize PID module's lifetime and functions, operating conditions should be followed as below

- [1] Normal operating condition
  - [1.1] Temperature : 20±15°C
  - [1.2] Humidity : 55±20%
  - [1.3] Well-ventilated place is suggested to set up PID module and system.
  - [1.4] Display pattern : regular switched patterns or moving pictures.
    - [1.4.1] Periodical power-off or screen saver is needed after long-term static display.
    - [1.4.2] Moving picture or black pattern is strongly recommended for screen saver.
- [2] Operating requirements of PID modules and systems to prevent uneven display under long-term operating.

[2.1] PID suitable operating time : under 20 hrs a day.

[2.2] Periodical display contents should be changed from static image to moving picture.

[2.2.1] Different background and image colors changed respectively, and changed colors periodically.

[2.2.2] Background and image with large different luminance displayed at the same time should be avoided.

[3] The startup voltage of a Backlight may cause an electrical shock while assembling with the converter. Do not disassemble the module or insert anything into the Backlight unit.

[4] Do not connect or disconnect the module in the "Power On" condition.

[5] Do not exceed the absolute maximum rating value. (supply voltage variation, input voltage variation, variation in part contents and environmental temperature...) Otherwise the module may be damaged.

[6] If the liquid crystal material leaks from the panel, it should be kept away from the eyes or mouth. In case of contact with hands, skin or clothes, it has to be washed away thoroughly with soap.

[7] Module should be turned clockwise (regular front view perspective) when used in portrait mode.

[8] Ultra-violet ray filter is necessary for outdoor operation.

[9] Only when PID module is operated under right operating conditions, lifetime in this spec can be guaranteed.

After the module's end of life, it is not harmful in case of normal operation and storage.

### 8.3 SAFETY STANDARDS

The LCD module should be certified with safety regulations as follows:

Regulatory	Item	Standard
Information Technology equipment	UL	UL60950-1:2006 or Ed.2:2007
	cUL	CAN/CSA C22.2 No.60950-1-03 or 60950-1-07
	CB	IEC60950-1:2005 / EN60950-1:2006+ A11:2009
Audio/Video Apparatus	UL	UL60065 Ed.7:2007
	cUL	CAN/CSA C22.2 No.60065-03:2006 + A1:2006
	CB	IEC60065:2001+ A1:2005 / EN60065:2002 + A1:2006+ A11:2008

## 9. DEFINITION OF LABELS

### 9.1 MODULE LABEL

The barcode nameplate is pasted on each module as illustration, and its definitions are as following explanation.



## 9.2 CARTON LABEL

The barcode nameplate is pasted on each box as illustration, and its definitions are as following explanation.

## 10. PACKAGING

### 10.1 PACKAGING SPECIFICATIONS

- (1) 22 LCD TV modules / 1 Box
- (2) Box dimensions : 1288(L) X 1138 (W) X 775 (H) mm
- (3) Weight: Approx. 296Kg (22 modules per carton)

### 10.2 PACKAGING METHOD

Packaging method is shown as following figures.

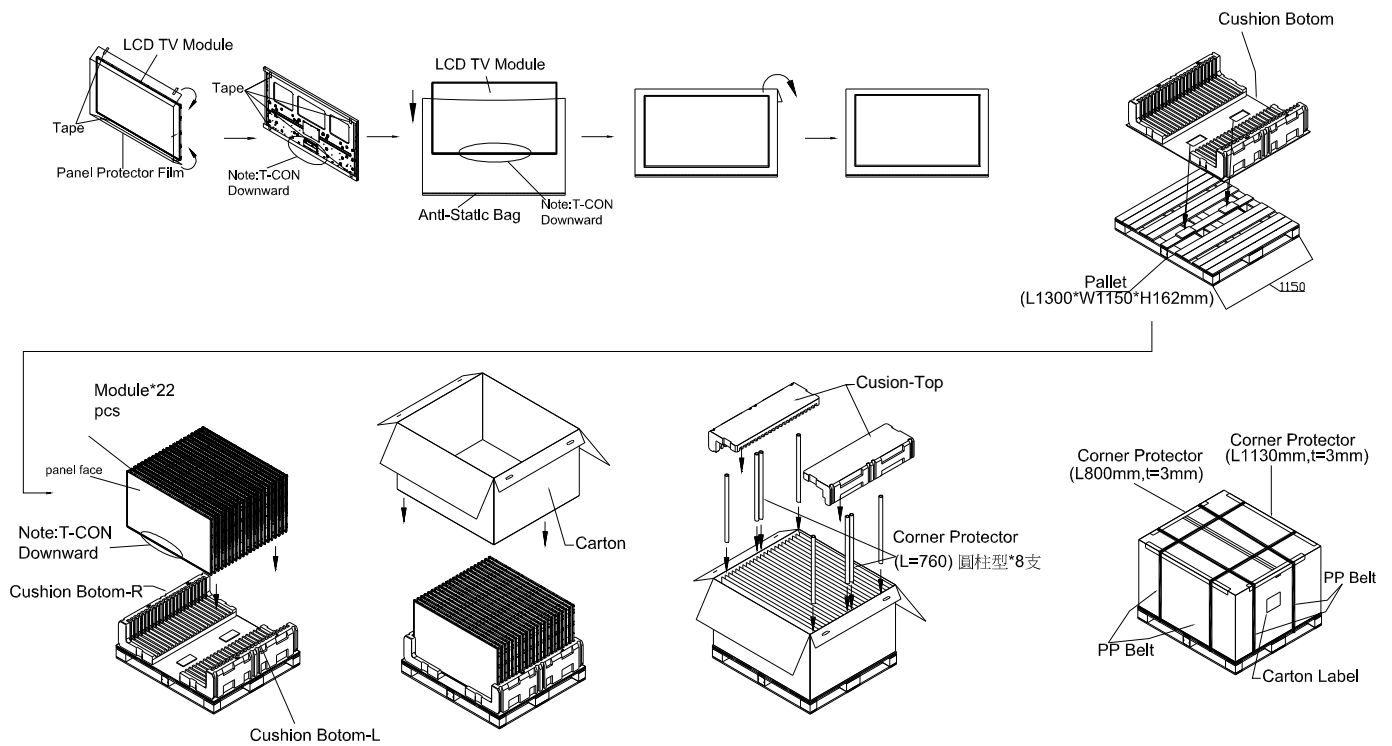
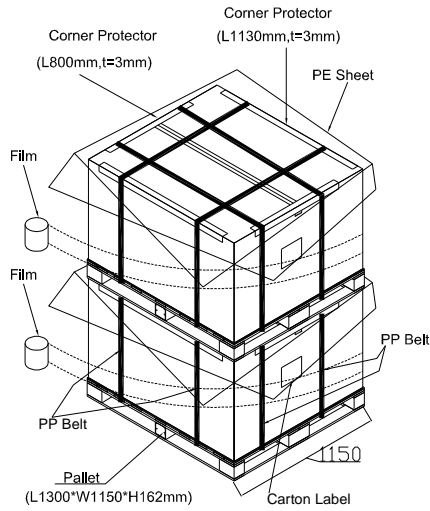


Figure.10-1 packing method

**Sea / Land Transportation  
(40ft HQ/40ft/20ft Container)**



**Air Transportation**

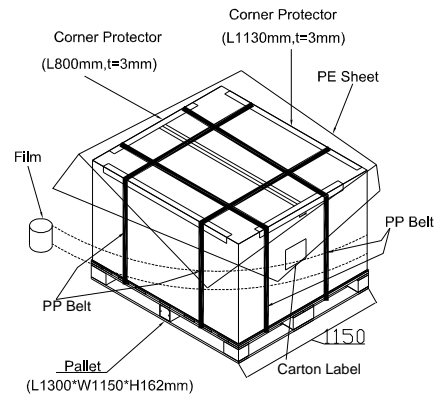


Figure. 10-2 Packing

**10.3 UN-PACKAGING METHOD**

Un-packaging method is shown as following figures.

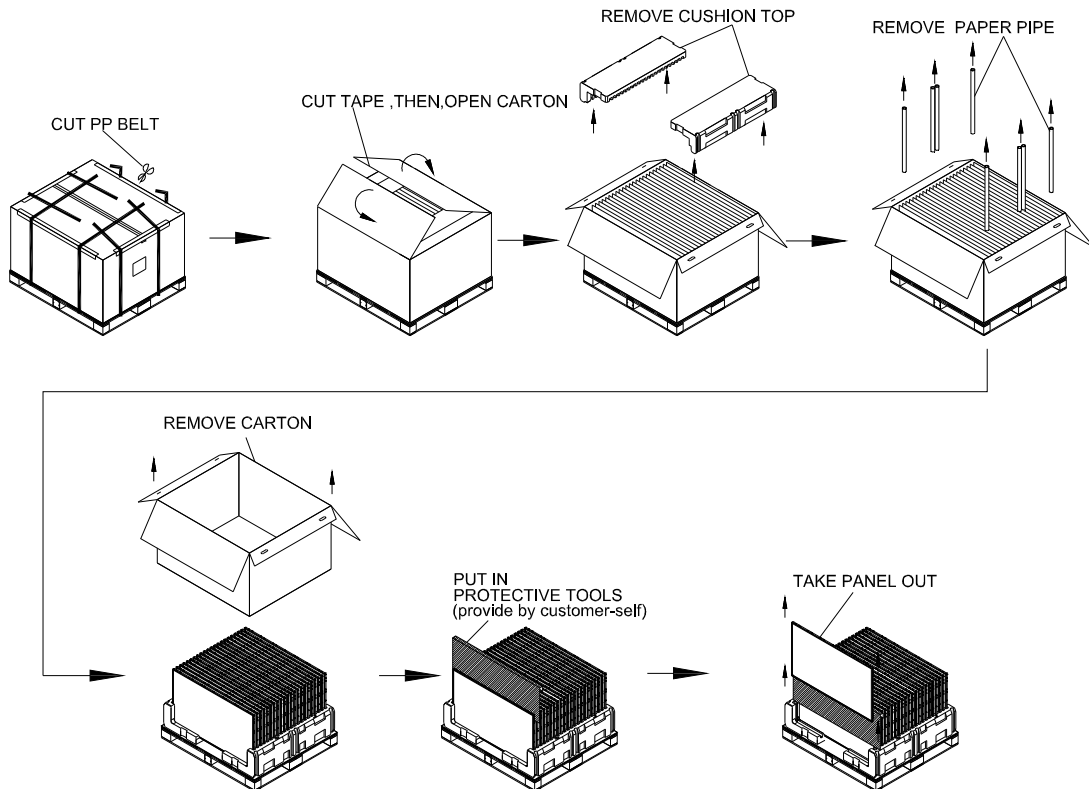
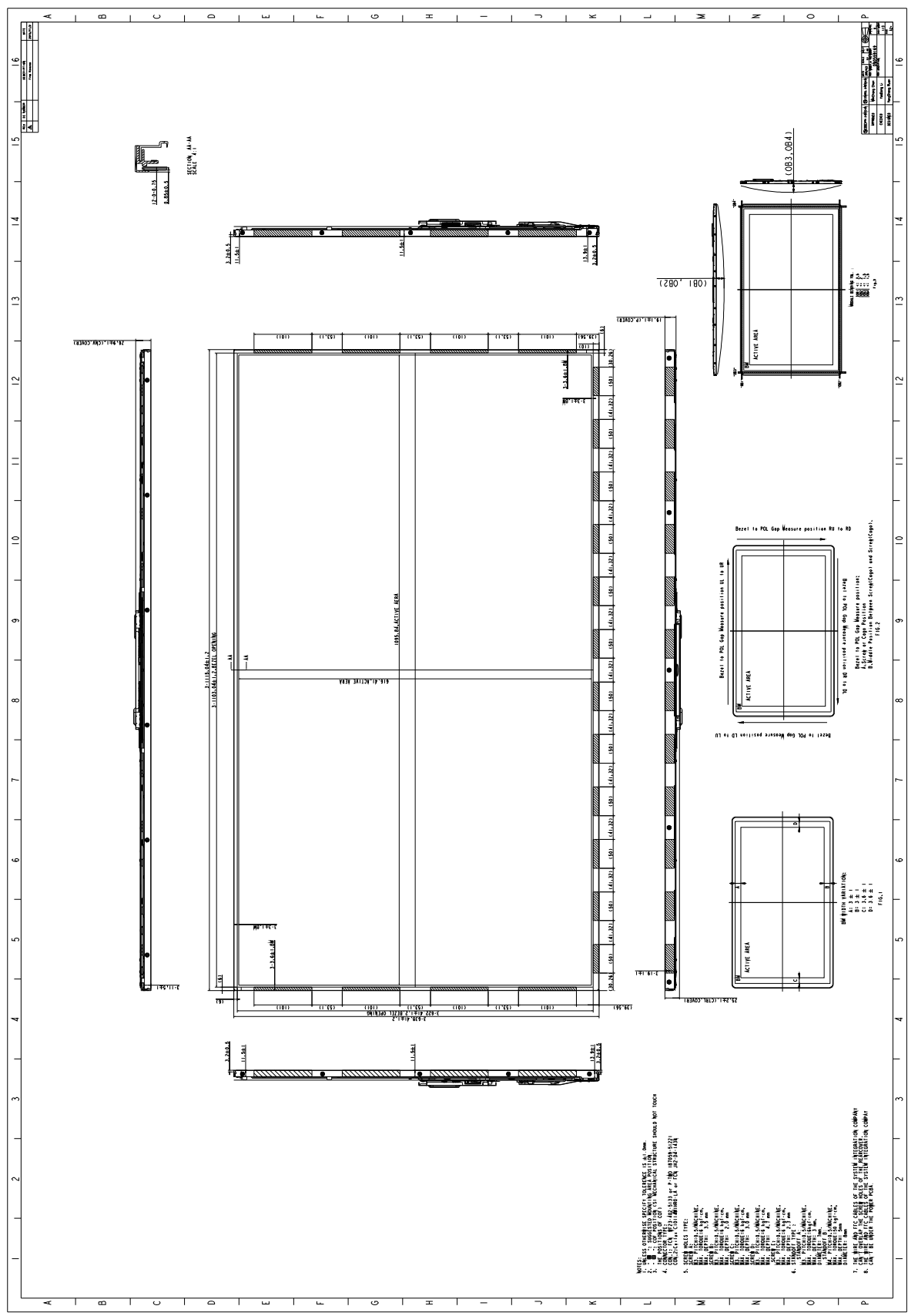
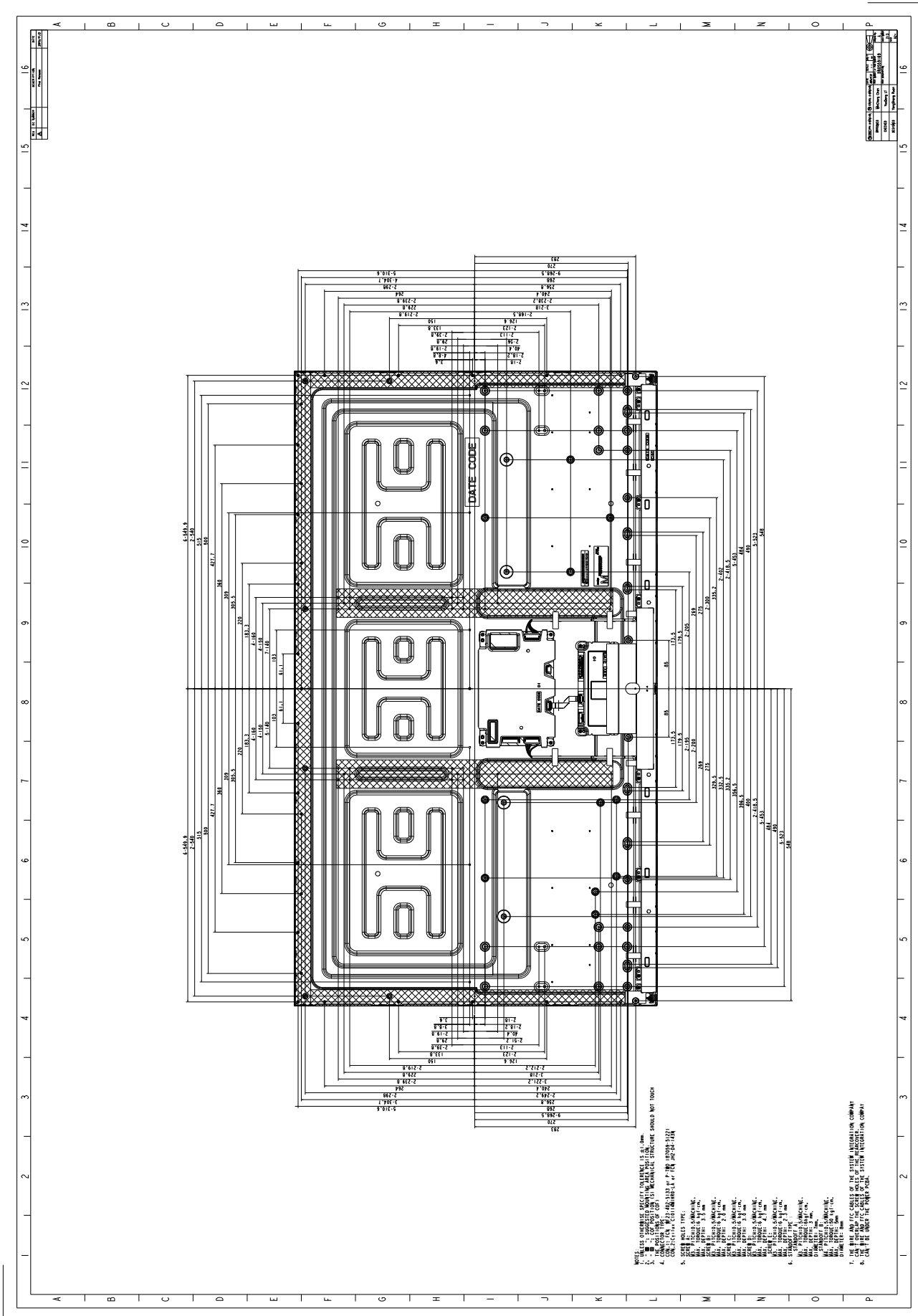
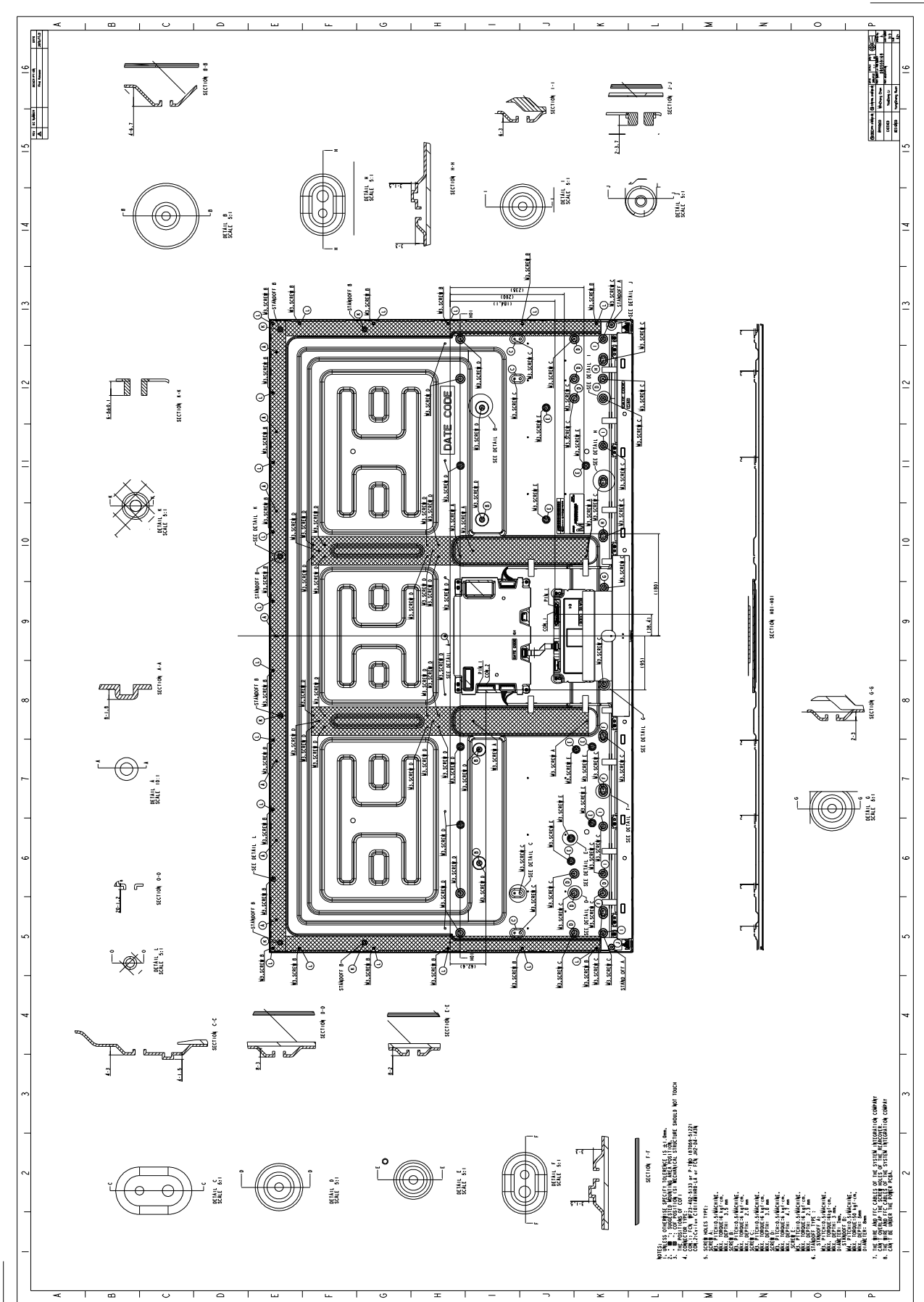


Figure. 10-3 un-packing

# 11. MECHANICAL CHARACTERISTIC







- NOTES: 1. DIMENSIONS UNLESS SPECIFIED IN DECIMALS ARE IN MILLIMETERS.  
2. DIMENSIONS IN PARENTHESES ARE IN INCHES.  
3. DIMENSIONS IN PARENTHESES ARE IN INCHES.  
4. DIMENSIONS IN PARENTHESES ARE IN INCHES.  
5. DIMENSIONS IN PARENTHESES ARE IN INCHES.  
6. DIMENSIONS IN PARENTHESES ARE IN INCHES.  
7. DIMENSIONS IN PARENTHESES ARE IN INCHES.  
8. DIMENSIONS IN PARENTHESES ARE IN INCHES.