US Micro Products
*Electronic Products for the OEM*

# OLED PRODUCT SPECIFICATION

Manufactured by:

RITEK GROUP
RiTdisplay Corporation

| | |
|---|---|
| **PART NUMBER:** | **USMP-P24701** |
| **DESCRIPTION:** | 0.5" OLED, WHITE,<br>72x32 resolution,<br>COG, Driver IC SPD0301 |

| ISSUE DATE | APPROVED BY<br>(Customer Use Only) | CHECKED BY | PREPARED BY |
|---|---|---|---|
| | | | |
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# REVISION RECORD

| REV. | REVISION DESCRIPTION | REV. DATE | REMARK |
|---|---|---|---|
| X01 | ■ INITIAL RELEASE | 2010. 03. 17 | |
| A01 | ■ Transfer from X version<br>■ Add the information of module weight<br>■ Add the packing specification | 2010. 04. 26 | Page 5 & 18 |

# CONTENTS

## 1. SCOPE

The purpose of this specification is to define the general provisions and quality requirements that apply to the supply of display cells manufactured by RiTdisplay. This document, together with the Module Assembly Drawing, is the highest-level specification for this product. It describes the product, identifies supporting documents and contains specifications.

## 2. WARRANTY

RiTdisplay warrants that the products delivered pursuant to this specification (or order) will conform to the agreed specifications for twelve (12) months from the shipping date ("Warranty Period"). RiTdisplay is obligated to repair or replace the products which are found to be defective or inconsistent with the specifications during the Warranty Period without charge, on condition that the products are stored or used as the conditions specified in the specifications. Nevertheless, RiTdisplay is not obligated to repair or replace the products without charge if the defects or inconsistency are caused by the force majeure or the reckless behaviors of the customer.
After the Warranty Period, all repairs or replacements of the products are subject to charge.



## 3. FEATURES

- Small molecular organic light emitting diode.
- Color : White
- Panel resolution : 72*32
- Driver IC : SPD0301
- Excellent Quick response time : 10μs
- Extremely thin thickness for best mechanism design : 1.21 mm
- High contrast : 2000:1
- Wide viewing angle : 160°
- Serial Peripheral Interface
- Wide range of operating temperature : -40 to 70°C
- Anti-glare polarizer.

## 4. MECHANICAL DATA

| NO | ITEM | SPECIFICATION | UNIT |
|---|---|---|---|
| 1 | Dot Matrix | 72 x 32 | dot |
| 2 | Dot Size | 0.136 (W) x 0.136 (H) | $mm^2$ |
| 3 | Dot Pitch | 0.156 (W) x 0.156 (H) | $mm^2$ |
| 4 | Aperture Rate | 76 | % |
| 5 | Active Area | 11.212 (W) x 4.972 (H) | $mm^2$ |
| 6 | Panel Size | 14.9 (W) x 11.29 (H) | $mm^2$ |
| 7* | Panel Thickness | 1.02 ± 0.05 | mm |
| 8 | Module Size | 25.45 (W) x 22.496 (H) x 1.21 (T) | $mm^3$ |
| 9 | Diagonal A/A size | 0.48 | inch |
| 10 | Module Weight | 0.41 ± 10% | gram |

* Panel thickness includes substrate glass, cover glass and UV glue thickness.

## 5. MAXIMUM RATINGS

| ITEM | MIN | MAX | UNIT | Condition | Remark |
|---|---|---|---|---|---|
| Supply Voltage ($V_{DD}$) | -0.3 | 4 | V | Ta = 25°C | IC maximum rating |
| Supply Voltage (Vcc) | 8 | 17 | V | Ta = 25°C | IC maximum rating |
| Operating Temp. | -40 | 70 | °C | | |
| Storage Temp | -40 | 85 | °C | | |
| Humidity | - | 85 | % | | |
| Life Time | 13,000 | - | Hrs | 220 cd/m$^2$, 50% checkerboard | Note (1) |
| Life Time | 15,000 | - | Hrs | 200 cd/m$^2$, 50% checkerboard | Note (2) |
| Life Time | 16,000 | - | Hrs | 180 cd/m$^2$, 50% checkerboard | Note (3) |

Note:

(A) Under Vcc = 13V

(B) Life time is defined the amount of time when the luminance has decayed to less than 50% of the initial measured luminance.

(C) Note (1), Note (2), Note (3) contrast setting are under VDD=2.8V,set VDD selection (0xad)=(0x40) and VDD=1.8V,set VDD selection (0xad)=(0x60).

(1) Setting of 220 cd/m$^2$:

- Contrast setting : 0x44
- Frame rate : 105Hz
- Duty setting : 1/32

(2) Setting of 200 cd/m$^2$:

- Contrast setting : 0x3e
- Frame rate : 105Hz
- Duty setting : 1/32

(3) Setting of 180 cd/m$^2$:

- Contrast setting : 0x37
- Frame rate : 105Hz
- Duty setting : 1/32

# 6. ELECTRICAL CHARACTERISTICS

## 6.1 D.C ELECTRICAL CHARACTERISTICS

| SYMBOL | PARAMETER | TEST CONDITION | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $V_{CC}$ | Operating Voltage | - | 12.5 | 13 | 13.5 | V |
| $V_{DD}$ | Logic Supply Voltage | - | 1.7<br>2.7 | 1.8<br>2.8 | 1.9<br>2.9 | V |
| $V_{OH}$ | High Logic Output Level | $I_{OUT}$ = 100uA, 3.3MHz | 0.9* $V_{DD}$ | - | - | V |
| $V_{OL}$ | Low Logic Output Level | $I_{OUT}$ = 100uA, 3.3MHz | - | - | 0.1*$V_{DD}$ | V |
| $V_{IH}$ | High Logic Input Level | - | 0.8* $V_{DD}$ | - | - | V |
| $V_{IL}$ | Low Logic Input Level | - | - | - | 0.2*$V_{DD}$ | V |
| $I_{DD, SLEEP}$ | Sleep mode Current | $V_{DD}$ = 1.65V~3.3V, $V_{CC}$ = 7V~16V Display OFF, No panel attached | - | - | 10 | uA |
| $I_{CC, SLEEP}$ | Sleep mode Current | $V_{DD}$ = 1.65V~3.3V, $V_{CC}$ = 7V~16V Display OFF, No panel attached | - | - | 10 | uA |
| $I_{CC}$ | $V_{CC}$ Supply Current $V_{DD}$ = 2.8V, $V_{CC}$ =12, IREF =10uA, No Panel attached, Display ON, All ON | Contrast = FFh | - | 450 | 580 | uA |
| $I_{DD}$ | $V_{DD}$ Supply Current $V_{DD}$ =2.8V, $V_{CC}$ = 12, IREF = 10uA , No Panel attached, Display ON, All ON, | | - | 90 | 110 | uA |
| $I_{SEG}$ | Segment Output Current, $V_{DD}$ = 2.8V, $V_{CC}$ =12V, IREF=10uA, Display ON. | Contrast=FFh | 280 | 310 | 340 | uA |
| | | Contrast=AFh | - | 215 | - | |
| | | Contrast=7Fh | - | 155 | - | |
| | | Contrast=3Fh | - | 78 | - | |
| | | Contrast=0Fh | - | 20 | - | |

## 6.2 ELECTRO-OPTICAL CHARACTERISTICS

**PANEL ELECTRICAL SPECIFICATIONS**

| PARAMETER | MIN | TYP. | MAX | UNITS | COMMENTS |
|---|---|---|---|---|---|
| Normal mode current consumption | - | 5.5 | 7.5 | mA | All pixels on |
| Standby mode current consumption | - | 0.5 | 1.5 | mA | Standby mode 10% pixels on |
| Normal mode power consumption | - | 71.5 | 97.5 | mW | All pixels on |
| Standby mode power consumption | - | 6.5 | 19.5 | mW | Standby mode 10% pixels on |
| Pixel Luminance | 180 | 200 | | $cd/m^2$ | Display Average |
| Standby Luminance | | 25 | | $cd/m^2$ | |
| CIEx (White) | 0.24 | 0.28 | 0.32 | | CIE1931 |
| CIEy (White) | 0.28 | 0.32 | 0.36 | | CIE1931 |
| Dark Room Contrast | 2000:1 | | | | |
| Viewing Angle | 160 | | | degree | |
| Response Time | | 10 | | μs | |

Note:

VDD is 2.8V,set VDD selection (0xad)=(0x40),

VDD is 1.8V,set VDD selection (0xad)=(0x60) contrast setting is shown below.

(1) Normal mode condition :

- Driving Voltage : 13V
- Contrast setting : 0x3e
- Frame rate : 105Hz
- Duty setting : 1/32

(2) Standby mode condition :

- Driving Voltage : 13V
- Contrast setting : 0x00
- Frame rate : 105Hz
- Duty setting : 1/32

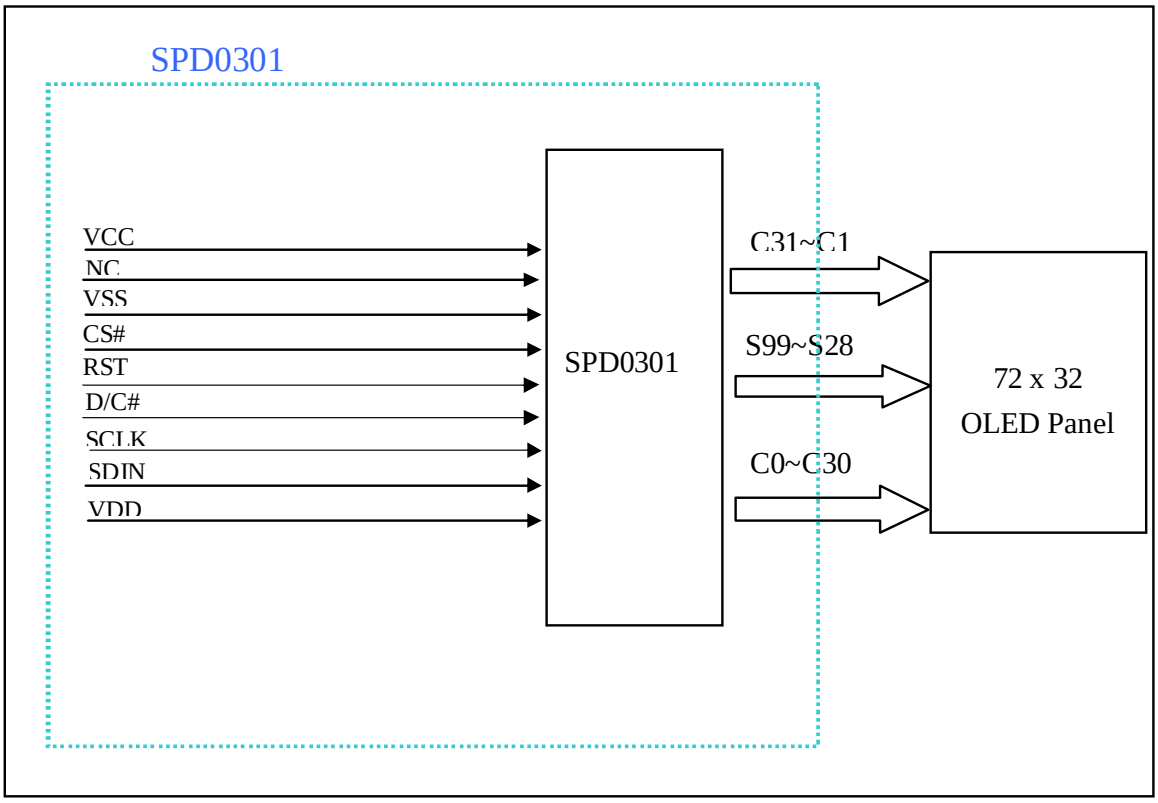
**VDD(Logic Supply Voltage):1.8V and 2.8V setting**

| Brightness(cd/m2) | VDD(V) | Set VDD selection (0xad) | Dot matrix current level (0x81) |
|---|---|---|---|
| 25 (Standby mode) | 2.8 | 0x40 | 0x00 |
| 180 (Minimum mode) | 2.8 | 0x40 | 0x37 |
| 200 (Typical mode) | 2.8 | 0x40 | 0x3e |
| 220 (Maximum mode) | 2.8 | 0x40 | 0x44 |

| Brightness(cd/m2) | VDD(V) | Set VDD selection (0xad) | Dot matrix current level (0x81) |
|---|---|---|---|
| 25 (Standby mode) | 1.8 | 0x60 | 0x00 |
| 180 (Minimum mode) | 1.8 | 0x60 | 0x37 |
| 200 (Typical mode) | 1.8 | 0x60 | 0x3e |
| 220 (Maximum mode) | 1.8 | 0x60 | 0x44 |

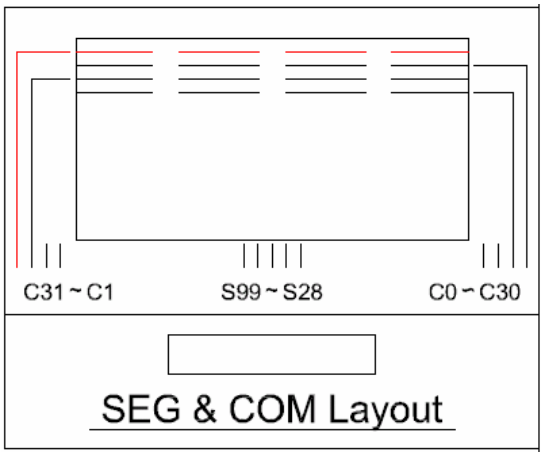
# 7. INTERFACE

## 7.1 FUNCTION BLOCK DIAGRAM




**Ridisplay 72X32 OLED Module**

## 7.2 PANEL LAYOUT DIAGRAM



### 7.3 PIN ASSIGNMENTS

| PIN NO | PIN NAME | DESCRIPTION |
|---|---|---|
| 1 | VCC | Power supply for panel driving voltage. |
| 2 | NC | This is dummy pin. Do not group or short NC pins together. |
| 3 | VSS | Ground pin. It must be connected to external ground. |
| 4 | CS# | This pin is the chip select input connecting to the MCU.<br>The chip is enabled for MCU communication only when CS# is pulled LOW (active LOW). |
| 5 | RST# | This pin is reset signal input.<br>When the pin is pulled LOW, initialization of the chip is executed.<br>Keep this pin pull HIGH during normal operation. |
| 6 | D/C# | This pin is Data/Command control pin connecting to the MCU. |
| 7 | SCLK | These pins are bi-directional data bus connecting to the MCU data bus.<br>When serial interface mode is selected, D0 will be the serial clock input: SCLK; D1 will be the serial data input: SDIN. |
| 8 | SDIN | |
| 9 | VDD | Power supply pin for core logic operation. |
| 10 | VSS | Ground pin. It must be connected to external ground. |
| 11 | VCC | Power supply for panel driving voltage. |

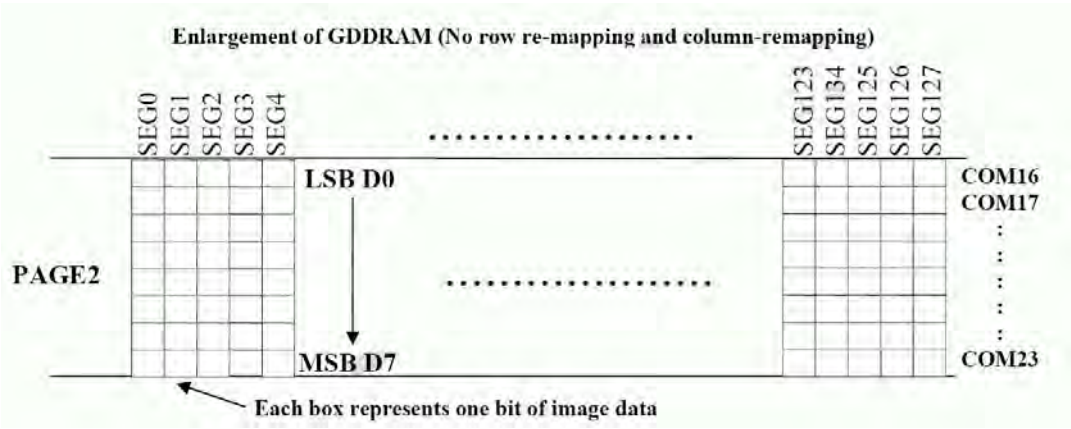
## 7.4 GRAPHIC DISPLAY DATA RAM ADDRESS MAP

The GDDRAM is a bit mapped static RAM holding the bit pattern to be displayed. The size of the RAM is 128 x 64 bits and the RAM is divided into eight pages, from PAGE0 to PAGE7, which are used for monochrome 128x64 dot matrix display, as shown in below figures.

GDDRAM pages structure of SPD0301

| | | Row re-mapping |
|---|---|---|
| PAGE0 (COM0-COM7) | Page 0 | PAGE0 (COM 63-COM56) |
| PAGE1 (COM8-COM15) | Page 1 | PAGE1 (COM 55-COM48) |
| PAGE2 (COM16-COM23) | Page 2 | PAGE2 (COM47-COM40) |
| PAGE3 (COM24-COM31) | Page 3 | PAGE3 (COM39-COM32) |
| PAGE4 (COM32-COM39) | Page 4 | PAGE4 (COM31-COM24) |
| PAGE5 (COM40-COM47) | Page 5 | PAGE5 (COM23-COM16) |
| PAGE6 (COM48–COM55) | Page 6 | PAGE6 (COM15-COM8) |
| PAGE7 (COM56-COM63) | Page 7 | PAGE7 (COM 7-COM0) |
| | SEG0 ----------SEG127 | |
| Column re-mapping | SEG127 ----------SEG0 | |

When one data byte is written into GDDRAM, all the rows image data of the same page of the current column are filled (i.e. the whole column (8 bits) pointed by the column address pointer is filled.). Data bit D0 is written into the top row, while data bit D7 is written into bottom row as shown in below figures.




For mechanical flexibility, re-mapping on both Segment and Common outputs can be selected by software.

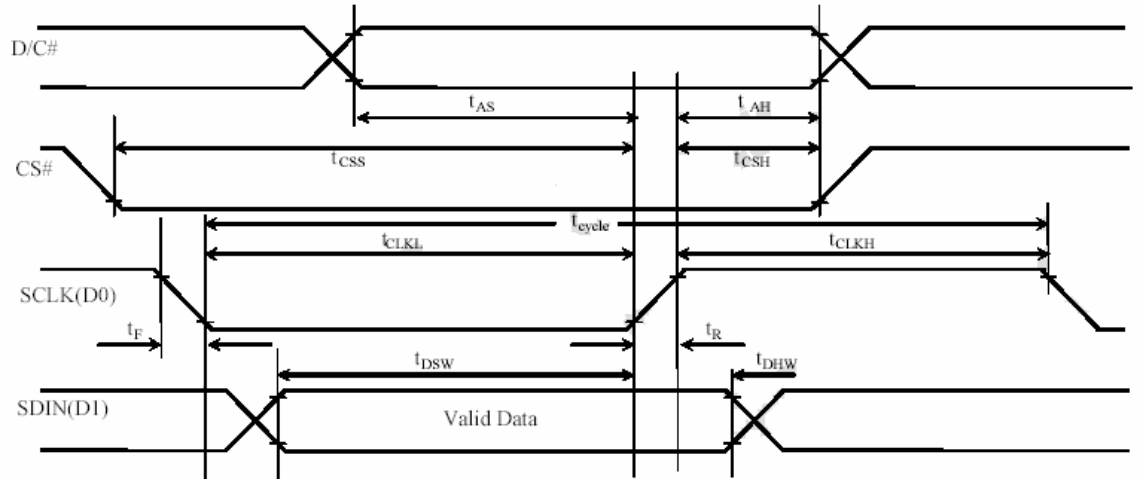
For vertical shifting of the display, an internal register storing the display start line can be set to control the portion of the RAM data to be mapped to the display (command D3h).

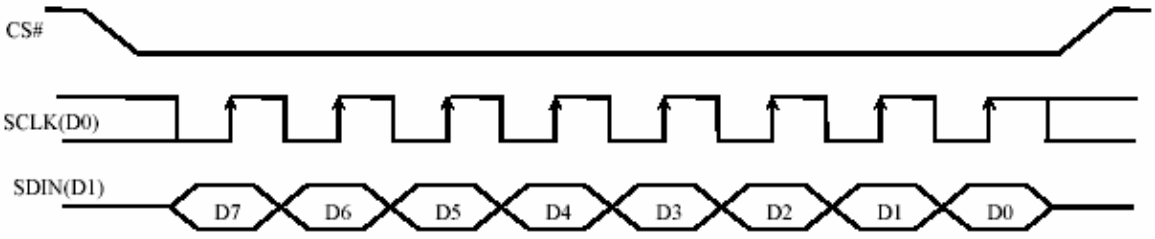
## 7.5 INTERFACE TIMING CHART

### SPI Interface Timing Characteristics.

($V_{DD}$ - $V_{SS}$ = 1.65V~3.3V, $T_A$ = 25°C)

| Symbol | Parameter | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| $t_{cycle}$ | Clock Cycle Time | 100 | - | - | ns |
| $t_{AS}$ | Address Setup Time | 15 | - | - | ns |
| $t_{AH}$ | Address Hold Time | 15 | - | - | ns |
| $t_{CSS}$ | Chip Select Setup Time | 20 | - | - | ns |
| $t_{CSH}$ | Chip Select Hold Time | 10 | - | - | ns |
| $t_{DSW}$ | Write Data Setup Time | 15 | - | - | ns |
| $t_{DHW}$ | Write Data Hold Time | 15 | - | - | ns |
| $t_{CLKL}$ | Clock Low Time | 20 | - | - | ns |
| $t_{CLKH}$ | Clock High Time | 20 | - | - | ns |
| $t_R$ | Rise Time | - | - | 40 | ns |
| $t_F$ | Fall Time | - | - | 40 | ns |



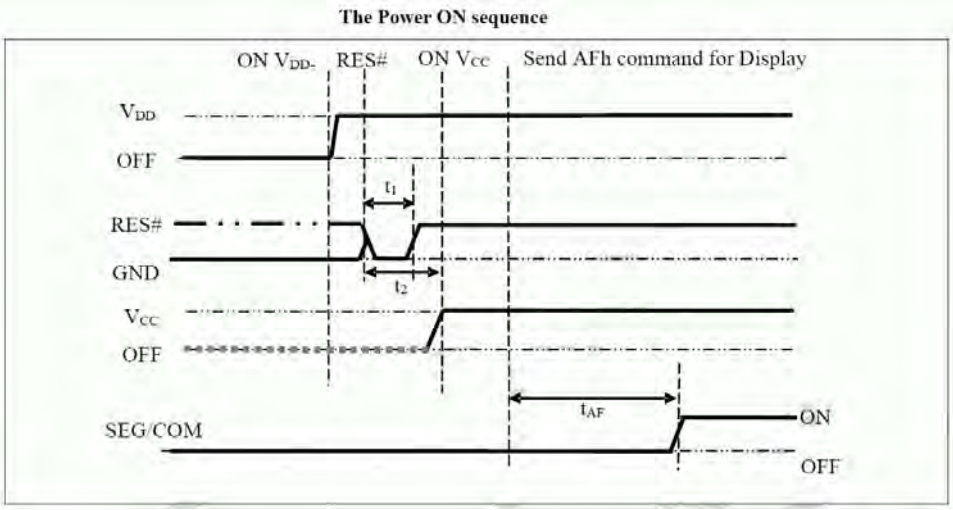
# 8. POWER ON / OFF SEQUENCE & APPLICATION CIRCUIT

## 8.1 POWER ON / OFF SEQUENCE

The following figures illustrate the recommended power ON and power OFF sequence of SPD0301

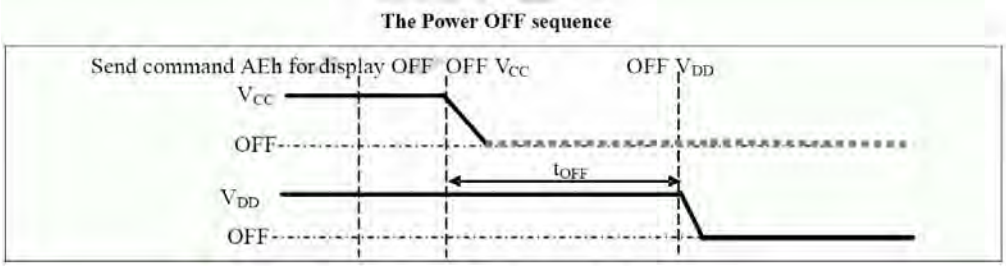
***Power ON sequence*:**

1. Power ON $V_{DD}$
2. After $V_{DD}$ become stable, set RES# pin LOW (logic low) for at least 3us ($t_1$) [3] and then HIGH (logic high).
3. After set RES# pin LOW (logic low), wait for at least 3us ($t_2$). Then Power ON $V_{CC}$. [1]
4. After $V_{CC}$ become stable, send command AFh for display ON. SEG/COM will be ON after 100ms ($t_{AF}$).




***Power OFF sequence*:**

1. Send command AEh for display OFF.
2. Power OFF $V_{CC}$ [1], [2]
3. Power OFF $V_{DD}$ after $t_{OFF}$.[4] (where Minimum $t_{OFF}$=80ms,Typical $t_{OFF}$=100ms)




**Note:**

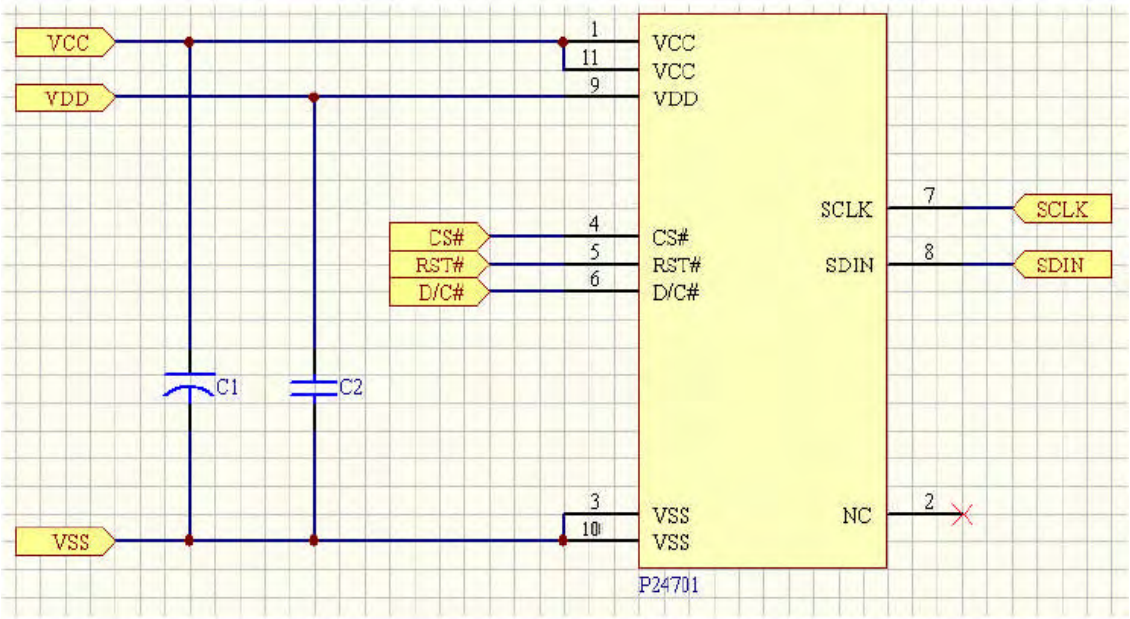
[1] $V_{CC}$ should be disabled when it is OFF.

[2] Power Pins ($V_{DD}$, $V_{CC}$) can never be pulled to ground under any circumstance.

[3] The register values are reset after $t_1$.

[4] $V_{DD}$ should not be Power OFF before $V_{CC}$ Power OFF.

## 8.2 APPLICATION CIRCUIT




**Recommend components:**

C1：4.7uF/25V(Tantalum type) or VISHAY (572D475X0025A2T)

C2：1uF/16V(0603)

**This circuit is for SPI interface.**

## 8.3 COMMAND TABLE

Refer to IC Spec.: SPD0301

## 9. RELIABILITY TEST CONDITIONS

| No. | Items | Specification | Quantity |
|---|---|---|---|
| 1 | High temp. (Non-operation) | 85°C, 240hrs | 5 |
| 2 | High temp. (Operation) | 70°C, 120hrs | 5 |
| 3 | Low temp. (Operation) | -40°C, 120hrs | 5 |
| 4 | High temp. / High humidity (Operation) | 65°C, 90%RH, 120hrs | 5 |
| 5 | Thermal shock (Non-operation) | -40°C ~85°C (-40°C /30min; transit /3min; 85°C /30min; transit /3min) 1cycle: 66min, 100 cycles | 5 |
| 6 | Vibration | Frequency : 5~50HZ, 0.5G<br>Scan rate : 1 oct/min<br>Time : 2 hrs/axis<br>Test axis : X, Y, Z | 1 Carton |
| 7 | Drop | Height: 120cm<br>Sequence : 1 angle、3 edges and 6 faces<br><br>Cycles: 1 | 1 Carton |
| 8 | ESD (Non-operation) | Air discharge model, ±8kV, 10 times | 5 |

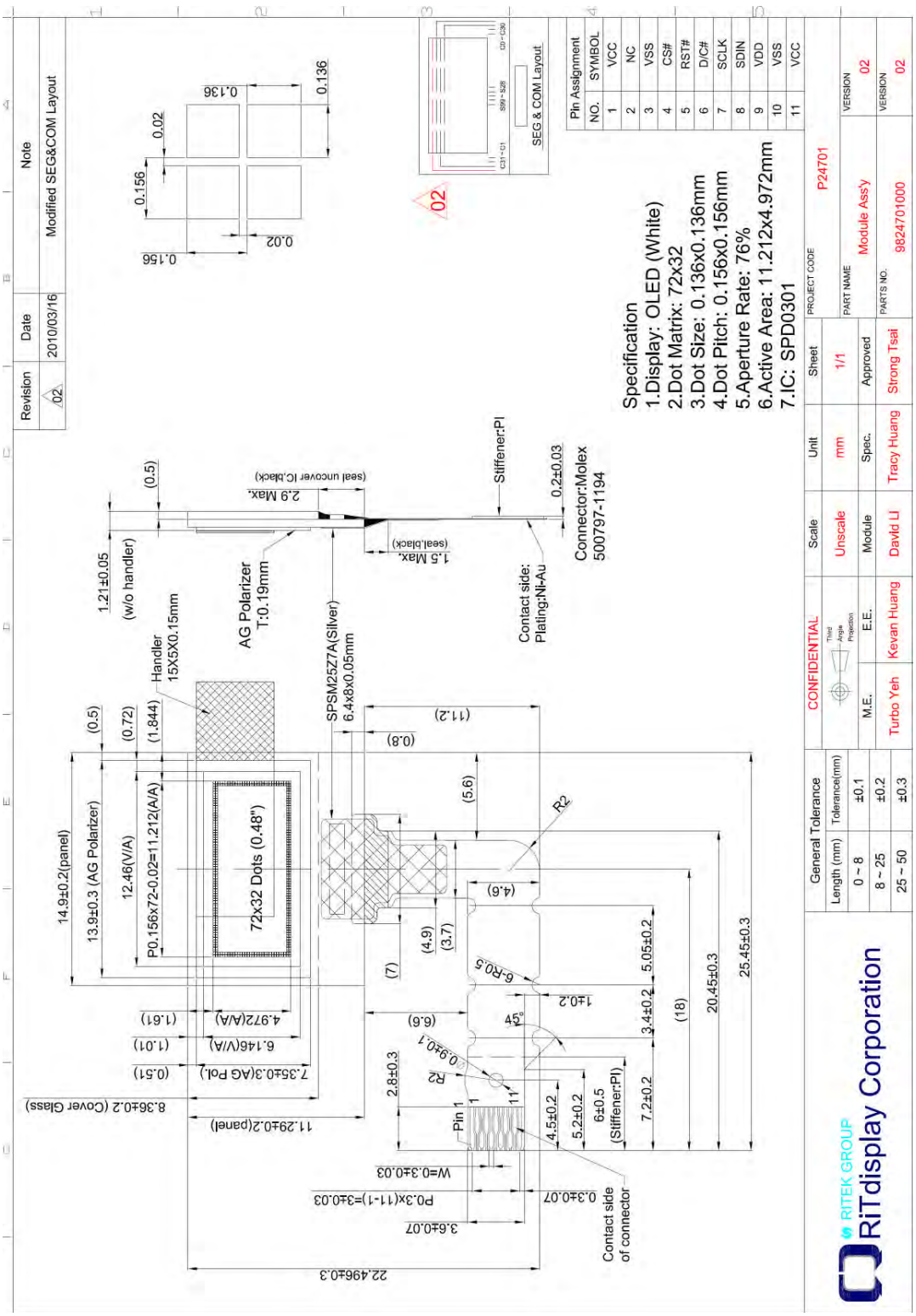
**Test and measurement conditions**

1. All measurements shall not be started until the specimens attain to temperature stability.
2. All-pixels-on is used as operation test pattern.
3. The degradation of Polarizer are ignored for item 1, 4 & 5.

**Evaluation criteria**

1. The function test is OK.
2. No observable defects.
3. Luminance: > 50% of initial value.
4. Current consumption: within ± 50% of initial value.

## 10. EXTERNAL DIMENSION



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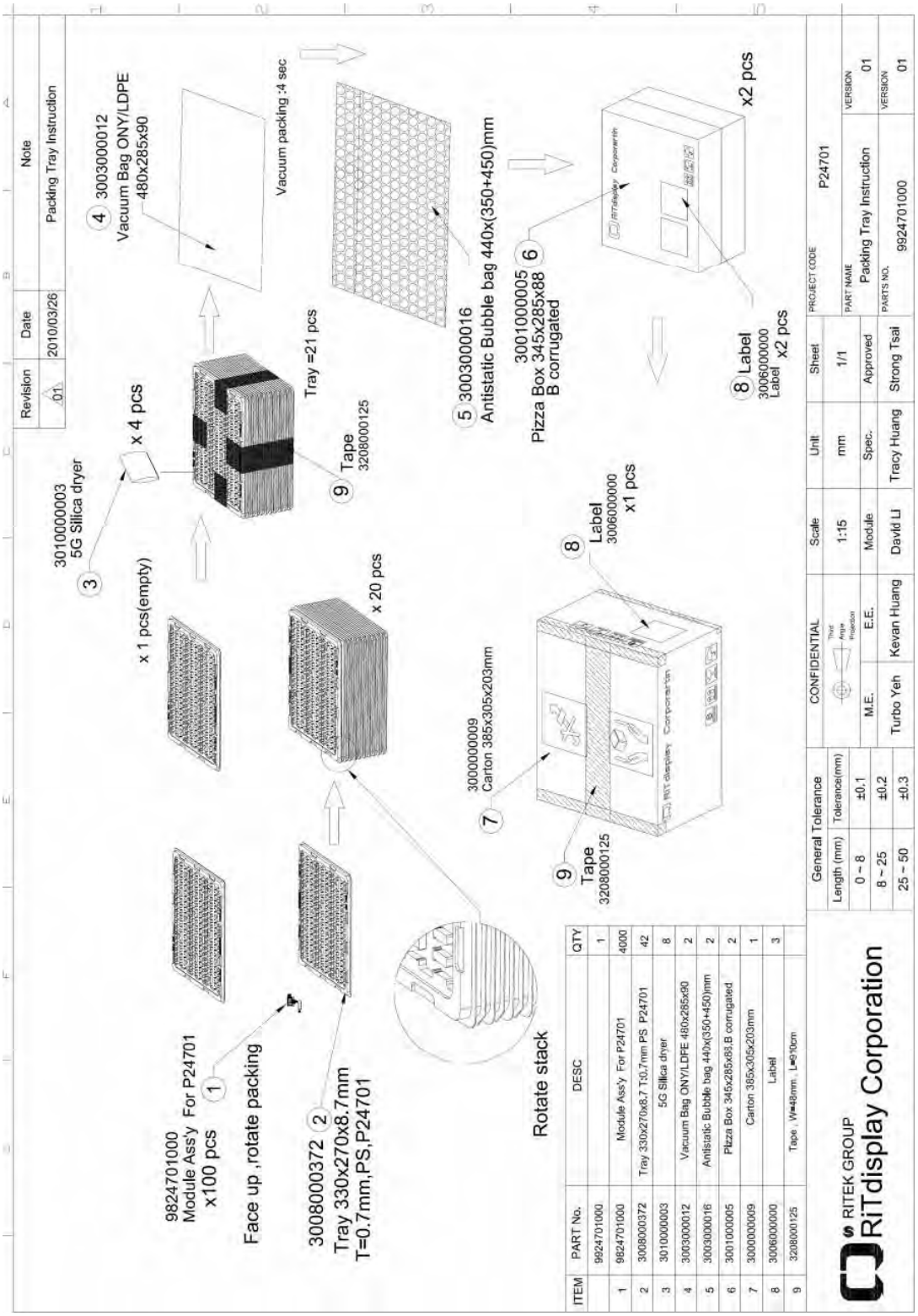
## 11. PACKING SPECIFICATION



# 12. APPENDIXES

## APPENDIX 1: DEFINITIONS

### A. DEFINITION OF CHROMATICITY COORDINATE

The chromaticity coordinate is defined as the coordinate value on the CIE 1931 color chart for R, G, B, W.

### B. DEFINITION OF CONTRAST RATIO

The contrast ratio is defined as the following formula:

$$\text{Contrast Ratio} = \frac{\text{Luminance of all pixels on measurement}}{\text{Luminance of all pixels off measurement}}$$

### C. DEFINITION OF RESPONSE TIME

The definition of turn-on response time Tr is the time interval between a pixel reaching 10% of steady state luminance and 90% of steady state luminance. The definition of turn-off response time Tf is the time interval between a pixel reaching 90% of steady state luminance and 10% of steady state luminance. It is shown in Figure 2.

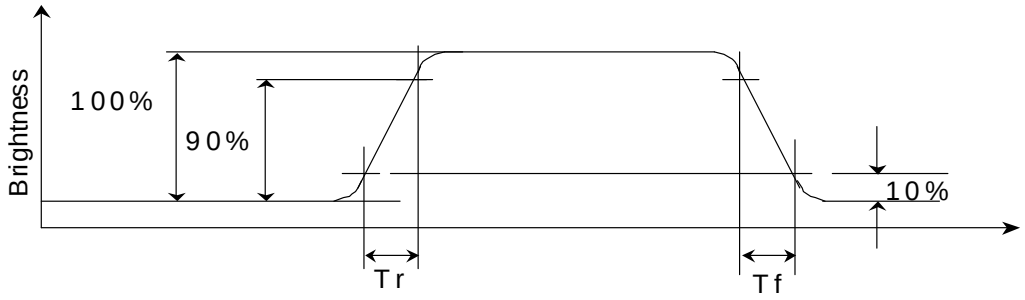



**Figure 2 Response time**

## D. DEFINITION OF VIEWING ANGLE

The viewing angle is defined as Figure 3. Horizontal and vertical (H & V) angles are determined for viewing directions where luminance varies by 50% of the perpendicular value.

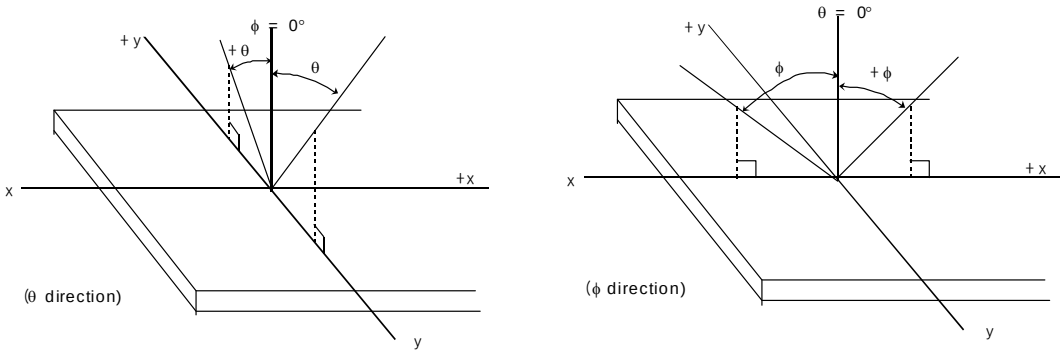
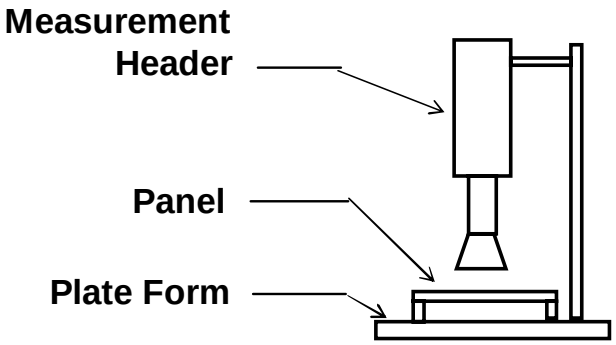



**Figure 3 Viewing angle**

## APPENDIX 2: MEASUREMENT APPARATUS

### A. LUMINANCE/COLOR COORDINATE

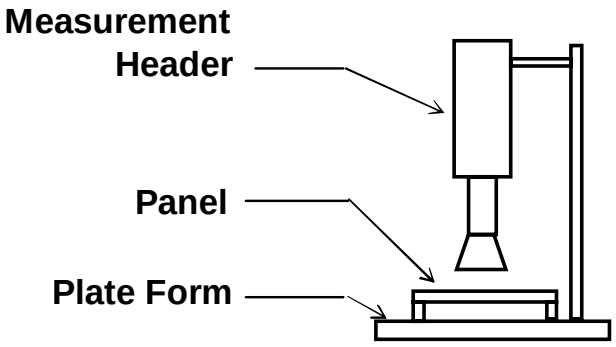
PHOTO RESEARCH PR-705, MINOLTA CS-100




**PR-705 / MINOLTA CS-100 Color Analyzer**

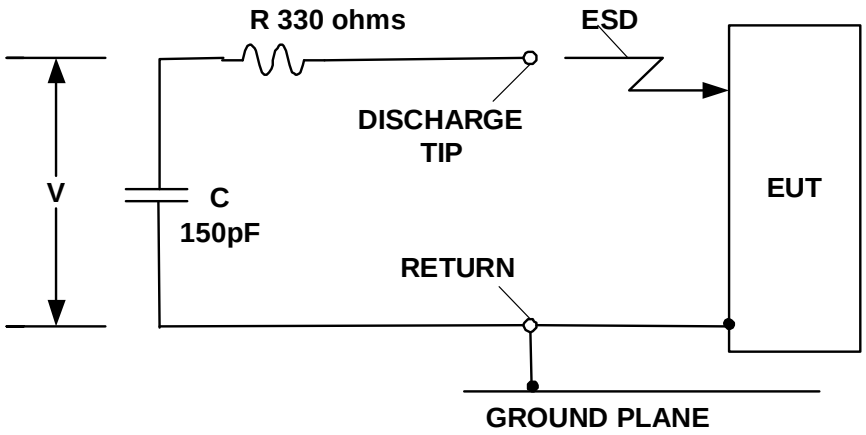
### B. CONTRAST / RESPONSE TIME / VIEWING ANGLE

WESTAR CORPORATION FPM-510




**Westar FPM-510 Display Contrast / Response time / View angle Analyzer**

## C. ESD ON AIR DISCHARGE MODE



## APPENDIX 3: PRECAUTIONS

### A. RESIDUE IMAGE

Because the pixels are lighted in different time, the luminance of active pixels may reduce or differ from inactive pixels. Therefore, the residue image will occur. To avoid the residue image, every pixel needs to be lighted up uniformly.

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