



US Micro Products
Electronic Products for the OEM

OLED PRODUCT SPECIFICATION

Manufactured by:



PART NUMBER:	USMP-P23601
DESCRIPTION:	1.0", 128 x 32, White, LD7032, TAB

ISSUE DATE	APPROVED BY (Customer Use Only)	CHECKED BY	PREPARED BY
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Preliminary Specification

PRODUCT NAME: RGS10128032WR006
PRODUCT NO.: 9923601000

CUSTOMER
APPROVED BY
DATE:

RITDISPLAY CORP. APPROVED

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REVISION RECORD

REV.	REVISION DESCRIPTION	REV. DATE	REMARK
X01	INITIAL RELEASE	2008. 12. 22	

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1. SCOPE

The purpose of this specification is to define the general provisions and quality requirements that apply to the supply of display cells manufactured by RiTdisplay. This document, together with the Module Assembly Drawing, is the highest-level specification for this product. It describes the product, identifies supporting documents and contains specifications.

2. WARRANTY

RiTdisplay warrants that the products delivered pursuant to this specification (or order) will conform to the agreed specifications for twelve (12) months from the shipping date ("Warranty Period"). RiTdisplay is obligated to repair or replace the products which are found to be defective or inconsistent with the specifications during the Warranty Period without charge, on condition that the products are stored or used as the conditions specified in the specifications. Nevertheless, RiTdisplay is not obligated to repair or replace the products without charge if the defects or inconsistency are caused by the force majeure or the reckless behaviors of the customer.

After the Warranty Period, all repairs or replacements of the products are subject to charge.

3. FEATURES

- Small molecular organic light emitting diode.
- Color : White
- Panel matrix : 128*32
- Driver IC : LD7032
- Excellent quick response time.
- Extremely thin thickness for best mechanism design : 1.21mm
- High contrast : 2000:1
- Wide viewing angle : 160°
- 8080 or 6800 series parallel interface, Serial Peripheral Interface, I²C Serial Interface.
- Wide range of operating temperature : -40 to 70 °C
- Anti-glare polarizer.

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4. MECHANICAL DATA

NO	ITEM	SPECIFICATION	UNIT
1	Dot Matrix	128 (W) x 32 (H)	dot
2	Dot Size	0.18 (W) x 0.18 (H)	mm ²
3	Dot Pitch	0.20 (W) x 0.20 (H)	mm ²
4	Aperture Rate	81	%
5	Active Area	25.58 (W) x 6.38 (H)	mm ²
6	Panel Size	29.8 (W) x 15.4 (H)	mm ²
7	Panel Thickness	1.21 ± 0.1	mm
8	Module Size	29.8 (W) x 22.4 (H) x 1.21 (D)	mm ³
9	Diagonal A/A size	1.0	inch
10	Module Weight	TBD	gram

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5. MAXIMUM RATINGS

ITEM	MIN	MAX	UNIT	Condition	Remark
Supply Voltage (VDD)	-0.3	3.63	V	-40~+85°C	IC maximum rating
Supply Voltage (VCC C)	8	18	V	-40~+85°C	IC maximum rating
Operating Temp.	-40	70	°C		
Storage Temp	-40	85	°C		
Humidity	-	85	%		
Life Time	21,000	-	Hrs	140cd/m ² , 50% checkerboard	Note (1)
Life Time	25,000		Hrs	120 cd/m ² , 50% checkerboard	Note (2)
Life Time	30,000	-	Hrs	100 cd/m ² , 50% checkerboard	Note (3)

Note:

(A) Under VCC C = TBD, Ta = 25°C, 50% RH.

(B) Life time is defined the amount of time when the luminance has decayed to less than 50% of the initial measured luminance.

(1) Setting of 140 cd/m² :

- Contrast setting : TBD
- Frame rate : TBD
- Duty setting : 1/32

(2) Setting of 120 cd/m² :

- Contrast setting : TBD
- Frame rate : TBD
- Duty setting : 1/32

(3) Setting of 100 cd/m² :

- Contrast setting : TBD
- Frame rate : TBD
- Duty setting : 1/32

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6. ELECTRICAL CHARACTERISTICS

6.1 D.C ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
VDD	Logic Power 1		1.65	2.8	3.5	V
VCC C	OLED operating voltage		TBD	TBD	TBD	V
V _{IH}	High Logic Input Level		0.8*VDD	-	VDD	V
V _{IL}	Low Logic Input Level		0	-	0.2*VDD	V
V _{OH}	High Logic Output Level	I _{out} = -100uA	0.9*VDD	-	VDD	V
V _{OL}	Low Logic Output Level	I _{out} = 100uA	0	-	0.1*VDD	V
IIL	Input Leakage Current		-1.0		+1.0	μA
C _{ptp1}	Output Current Pin to Pin Evenness *1)	I _{out} = 50uA	-2.0	-	+2.0	%
C _{alp1}	Output Current Evenness *2)	I _{out} = 50uA	-4.0	-	+4.0	%
C _{alp2}	Output Current Evenness *4)	I _{out} = 50uA	TBD	-	TBD	%
C _{chip1}	Output Current Absolute Correctness *3)	I _{out} = 50uA	-6.0	-	+6.0	%

NOTICE:

*1) $(I_k - I_{k+1}) / I_{avg}$: (k = 0 to 127), $I_{avg} = \sum (I_k) / 127$: (k = 0 to 127)

*2) $(I_{max} - I_{avg}) / I_{avg}$, $(I_{min} - I_{avg}) / I_{avg}$, $I_{avg} = \sum (I_k) / 127$: (k = 0 to 127)

*3) $(I_{avg} - I_{ref}(SPEC)) / I_{ref}(SPEC)$

*4) Area Current Deviation at 1chip.

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6.2 ELECTRO-OPTICAL CHARACTERISTICS

PANEL ELECTRICAL SPECIFICATIONS

PARAMETER	MIN	TYP.	MAX	UNITS	COMMENTS
Normal mode current		TBD	TBD	mA	All pixels on (1)
Standby mode current		TBD	TBD	mA	Standby mode 10% pixels on (2)
Normal mode power consumption		TBD	TBD	mW	All pixels on (1)
Standby mode power consumption		TBD	TBD	mW	Standby mode 10% pixels on (2)
Normal Luminance	100	120		cd/m ²	Display Average
Standby Luminance		TBD		cd/m ²	Display Average
CIE _x (White)	0.24	0.28	0.32		x, y (CIE 1931)
CIE _y (White)	0.28	0.32	0.36		
Dark Room Contrast	2000:1				
Viewing Angle	160			degree	
Response Time		10		μs	

(1) Normal mode condition :

- Driving Voltage : TBD
- Contrast setting : TBD
- Frame rate : TBD
- Duty setting : 1/32

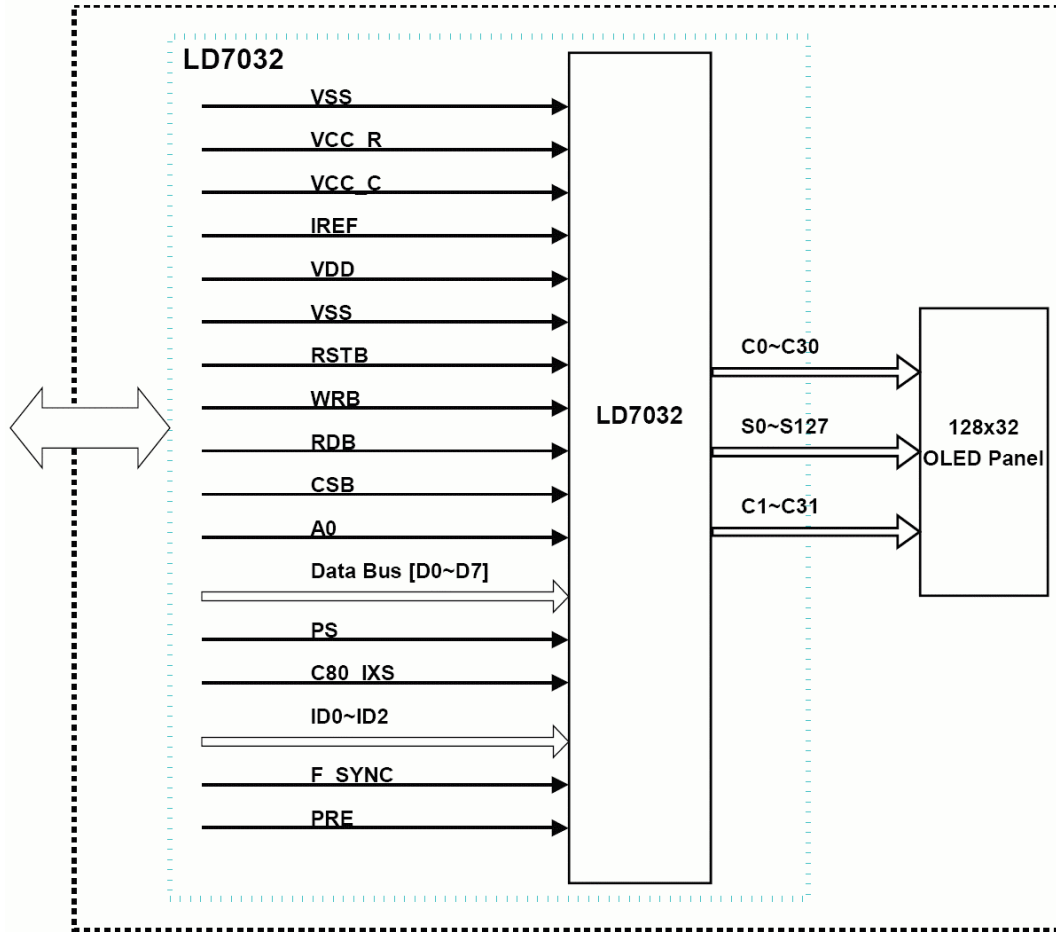
(2) Standby mode condition :

- Driving Voltage : TBD
- Contrast setting : TBD
- Frame rate : TBD
- Duty setting : 1/32

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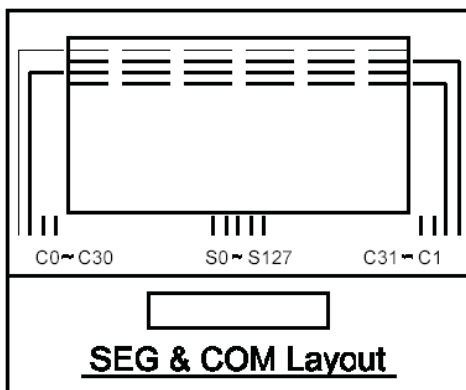
7. INTERFACE

7.1 FUNCTION BLOCK DIAGRAM



RiTdisplay 128x32 OLED Module

7.2 PANEL LAYOUT DIAGRAM



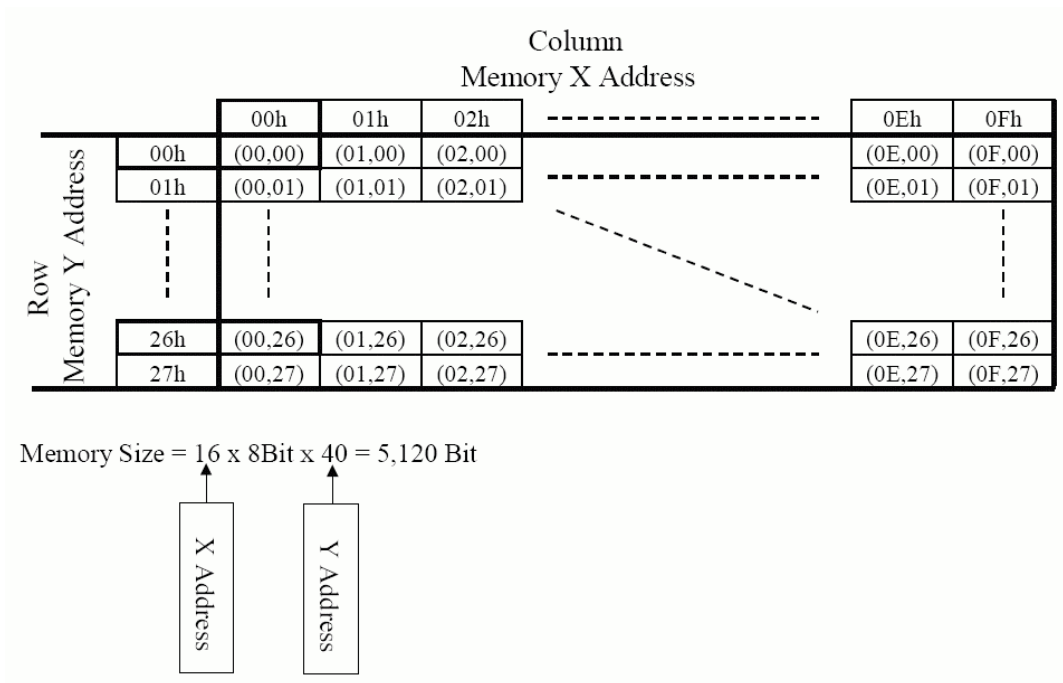
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7.3 PIN ASSIGNMENTS

PIN NO.	PIN NAME	DESCRIPTION
1	VSS	Ground pin.
2	VCC R	OELD Dot Matrix Power Supply for Row Driver. A 4.7uF capacitor is recommended to connect between VCC R and GND. If internal row power regulator is disabled, It must be connected to the external high voltage source or VCC C.
3	VCC C	OELD Dot Matrix Power Supply for Column VCC C Driver.
4	IREF	This pin is the dot output current reference pin. A resistor should be connected between this pin and VSS.
5	VDD	Analog and digital voltage supply.
6	VSS	Ground pin.
7	RSTB	Reset (Active Low).
8	WRB	Write (Active Low, 80 Interface). H:Read L:Write (68 Interface).
9	RDB	Read (Active Low, 80 Interface). Enable (68 Interface).
10	CSB	Chip Select (Active Low).
11	A0	Address (L: command, H: Parameter).
12	D7	These are 8-bit bi-directional data bus to be connected to the microprocessor's data bus.
13	D6	
14	D5	When I ² C interface mode is selected, D1 will be the I ² C data input (SDA) and D0 will be the I ² C bus clock input (SCL), and D2 ~ D7 should be tied VDD or VSS or floating.
15	D4	
16	D3	When serial interface mode is selected, D1 will be the serial data input (SDIN), D0 will be the serial clock input (SCLK), and D2 ~ D7 should be tied VDD or VSS or floating.
17	D2	
18	D1	
19	D0	
20	PS	H: Parallel L: Serial
21	C80 IXS	H: 68CPU, I ² C is selected. L: 80CPU, I ² C is not selected.
22	ID2	These pins configure I ² C interface address. Using these pins, I ² C Address can be selected.
23	ID1	
24	ID0	
25	F SYNC	Frame Sync Signal.
26	PRE	Pre-Charge Voltage.
27	VCC C	OELD Dot Matrix Power Supply for Column VCC C Driver.
28	VSS	Ground pin.

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7.4 GRAPHIC DISPLAY DATA RAM ADDRESS MAP



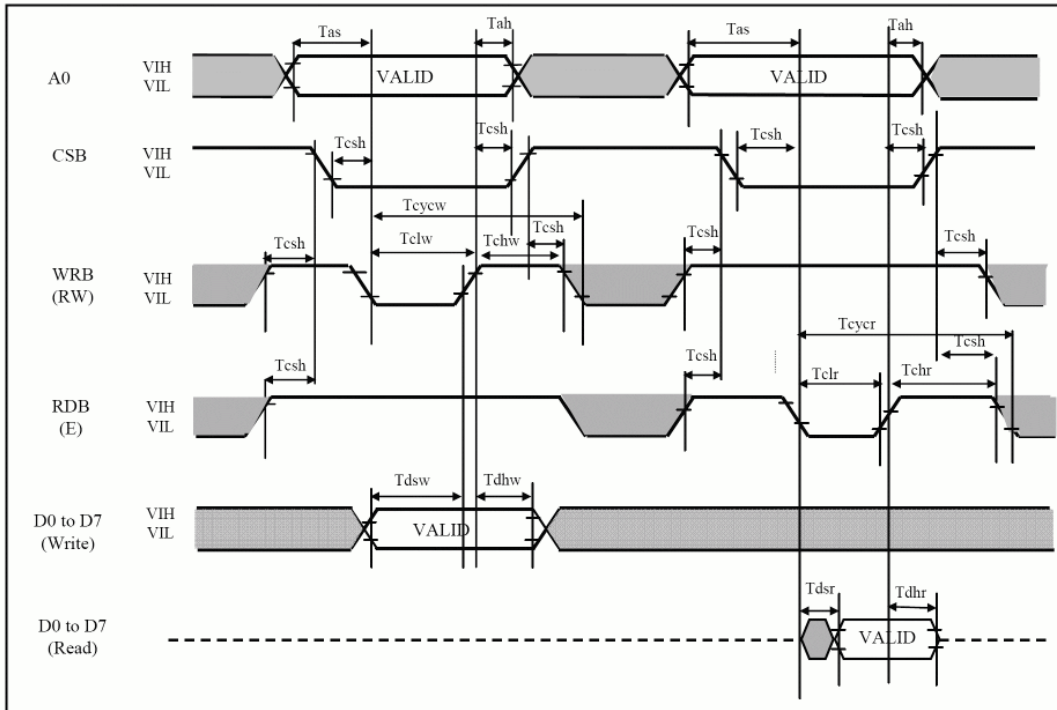
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7.5 INTERFACE TIMING CHART

Parallel Interface 1 (Write/Read Timing)

(VSS = 0V, VDD= 2.6V~3.5V, Ta = 25 °C)

Parameter	Symbol	Condition	Specification		Units
			MIN	MAX	
Address setup time	Tas	A0	20		ns
Address hold time	Tah	A0	10		
System cycle time	Teyw	WRB	Write	100	
	Teyr	RDB	Read	500	
Write control low pulse width	Tclw	WRB		40	
Write control high pulse width	Tchw			40	
Read control low pulse time	Tclr	RDB		60	
Read control high pulse time	Tchr			80	
Write data setup time	Tdsw	D0 - D7		20	
Write data hold time	Tdhw			10	
Read data setup time (Data Output Access Time)	Tdsr			200	
Read data hold time (Data output disable time)	Tdhr			10	
CSB - WRB , RDB time	Tesh		CSB	10	



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Parallel Interface2 (Write/Read Timing)

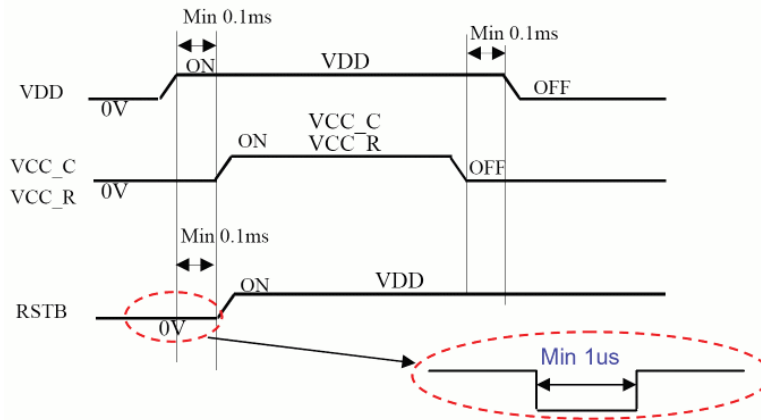
(VSS = 0V, VDD= 1.65V~3.5V, Ta = 25°C)

Parameter	Symbol	Condition		Specification		Units
				MIN	MAX	
Address setup time	Tas	A0		60		ns
Address hold time	Tah	A0		30		
System cycle time	Teyw	WRB	Write	300		
	Teyr	RDB	Read	500		
Write control low pulse width	Telw	WRB		120		
Write control high pulse width	Tehw			120		
Read control low pulse time	Telr	RDB		60		
Read control high pulse time	Tchr			80		
Write data setup time	Tdsw	D0 - D7		60		
Write data hold time	Tdhw			30		
Read data setup time (Data Output Access Time)	Tdsr				200	
Read data hold time (Data output disable time)	Tdhr			10		
CSB - WRB , RDB time	Tesh	CSB		30		

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8. POWER ON / OFF SEQUENCE & APPLICATION CIRCUIT

8.1 POWER ON / OFF SEQUENCE



Power On Sequence

System Power On 1 (Vdd On)

Wait for Several ms

RESB Active

System Power On 2 (Vcc On)

Wait for Several ms



Use Graphics Case

DSTBY OFF 14h 00h

3. Panel Condition Set

4. Drive Condition Set

5. Memory Data Write

DDISP ON 02h 01h

Graphics Off Sequence

Iref Off 12h 00h

DDISP Off 02h 00h

DSTBY ON 14h 01h



System Power Off 2 (Vcc Off)

Wait for Several ms

System Power Off 1 (Vdd Off)

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8.2 APPLICATION CIRCUIT

TBD

8.3 COMMAND TABLE

Refer to LD7032 IC Spec.

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9. RELIABILITY TEST CONDITIONS

No.	Items	Specification	Quantity
1	High temp. (Non-operation)	85°C, 240hrs	5
2	High temp. (Operation)	70°C, 120hrs	5
3	Low temp. (Operation)	-40°C, 120hrs	5
4	High temp. / High humidity (Operation)	65°C, 90%RH, 120hrs	5
5	Thermal shock (Non-operation)	-40°C ~85°C (-40°C /30min; transit /3min; 85°C /30min; transit /3min) 1cycle: 66min, 100 cycles	5
6	Vibration	Frequency : 5~50HZ, 0.5G Scan rate : 1 oct/min Time : 2 hrs/axis Test axis : X, Y, Z	1 Carton
7	Drop	Height: 120cm Sequence : 1 angle 、 3 edges and 6 faces Cycles: 1	1 Carton
8	ESD (Non-operation)	Air discharge model, ±8kV, 10 times	5

Test and measurement conditions

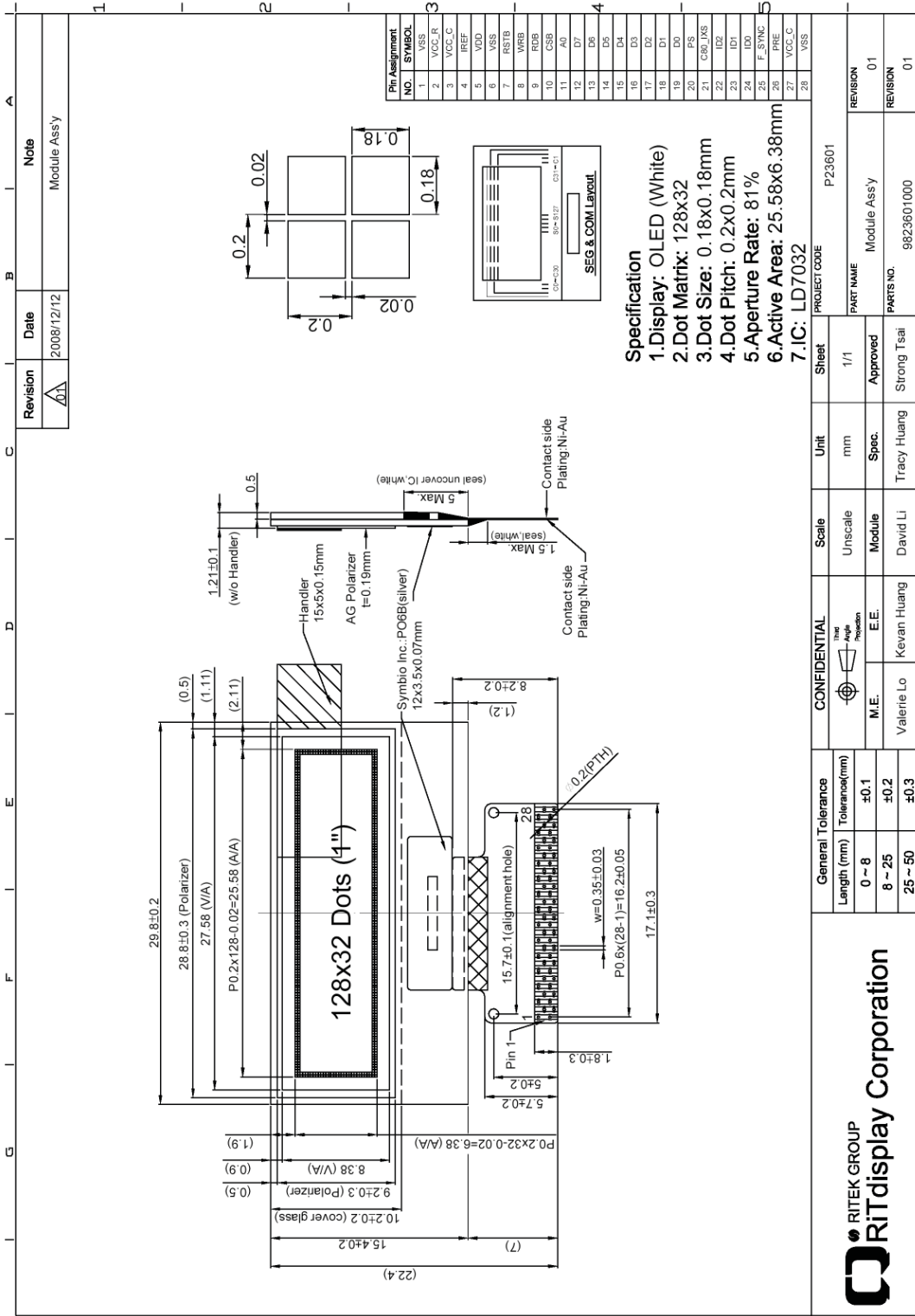
1. All measurements shall not be started until the specimens attain to temperature stability.
2. All-pixels-on is used as operation test pattern.
3. The degradation of Polarize are ignored for item 1, 4 & 5.

Evaluation criteria

1. The function test is OK.
2. No observable defects.
3. Luminance: > 50% of initial value.
4. Current consumption: within $\pm 50\%$ of initial value.

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10. EXTERNAL DIMENSION



11. PACKING SPECIFICATION

TBD

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12. APPENDIXES

APPENDIX 1: DEFINITIONS

A. DEFINITION OF CHROMATICITY COORDINATE

The chromaticity coordinate is defined as the coordinate value on the CIE 1931 color chart for R, G, B, W.

B. DEFINITION OF CONTRAST RATIO

The contrast ratio is defined as the following formula:

$$\text{Contrast Ratio} = \frac{\text{Luminance of all pixels on measurement}}{\text{Luminance of all pixels off measurement}}$$

C. DEFINITION OF RESPONSE TIME

The definition of turn-on response time T_r is the time interval between a pixel reaching 10% of steady state luminance and 90% of steady state luminance. The definition of turn-off response time T_f is the time interval between a pixel reaching 90% of steady state luminance and 10% of steady state luminance. It is shown in Figure 2.

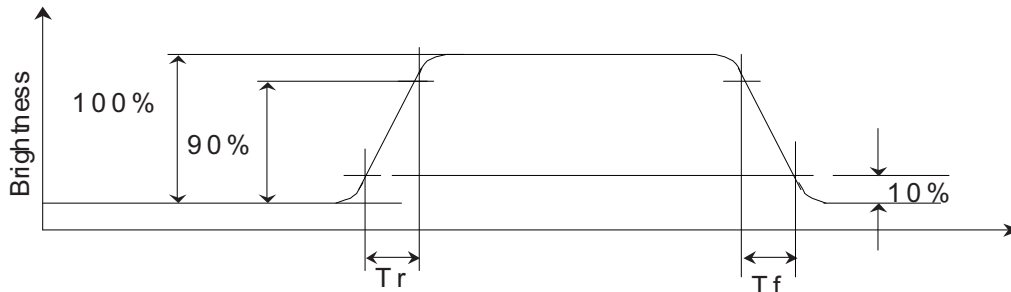


Figure 2: Response time

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D. DEFINITION OF VIEWING ANGLE

The viewing angle is defined as Figure 3. Horizontal and vertical (H & V) angles are determined for viewing directions where luminance varies by 50% of the perpendicular value.

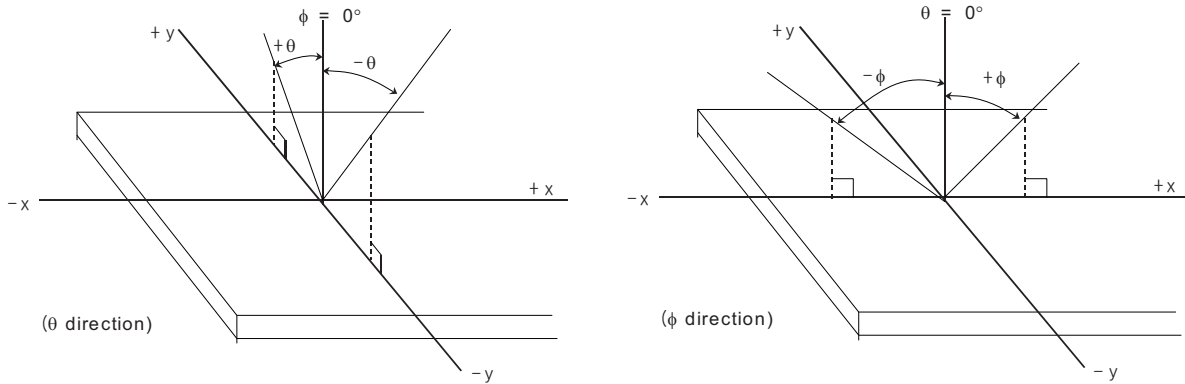


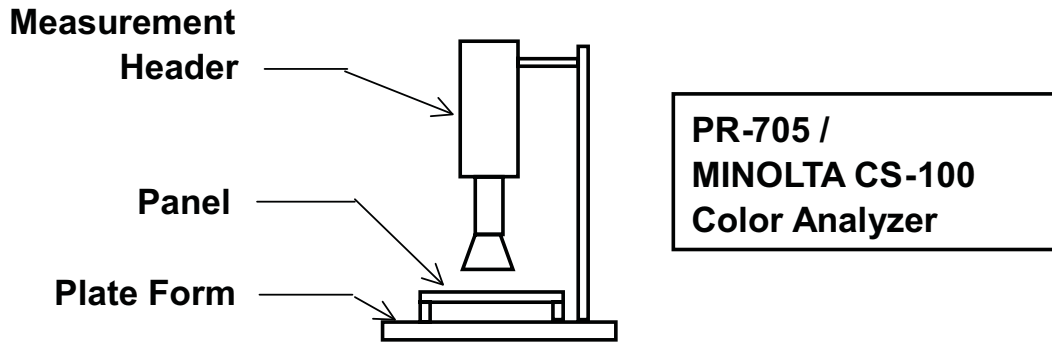
Figure 3: Viewing Angle

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APPENDIX 2: MEASUREMENT APPARATUS

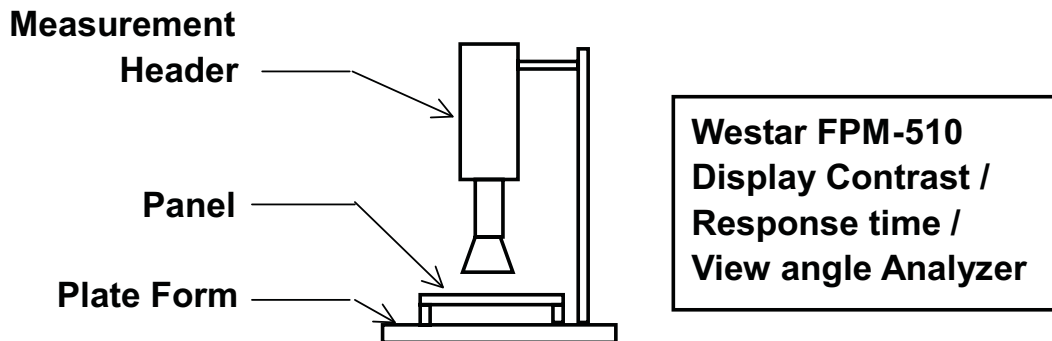
A. LUMINANCE/COLOR COORDINATE

PHOTO RESEARCH PR-705, MINOLTA CS-100



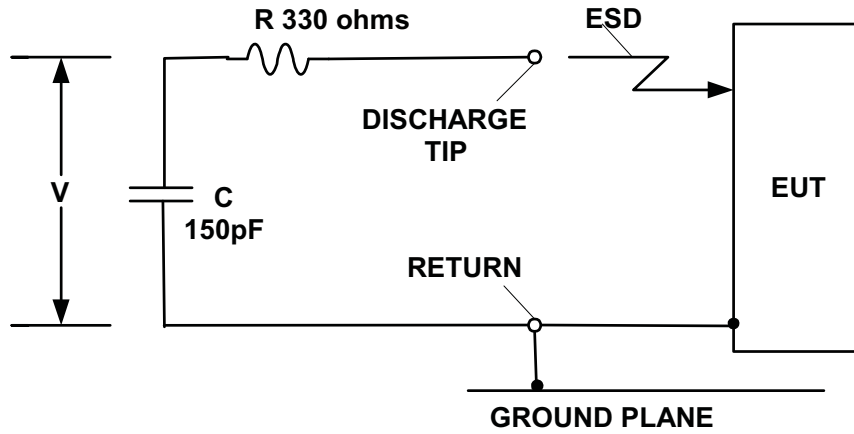
B. CONTRAST / RESPONSE TIME / VIEW ANGLE

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C. ESD ON AIR DISCHARGE MODE



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APPENDIX 3: PRECAUTIONS

A. RESIDUE IMAGE

Because the pixels are lighted in different time, the luminance of active pixels may reduce or differ from inactive pixels. Therefore, the residue image will occur. To avoid the residue image, every pixel needs to be lighted up uniformly.

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