



US Micro Products
Electronic Products for the OEM

OLED PRODUCT SPECIFICATION

Manufactured by:



| | |
|---------------------|---|
| PART NUMBER: | USMP-P21302 |
| DESCRIPTION: | 3.2", 256 x 64, Yellow, COF, SSD1322 |

| ISSUE DATE | APPROVED BY (Customer Use Only) | CHECKED BY | PREPARED BY |
|--------------------------|---|------------|-------------|
| | | | |
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REVISION RECORD

| REV. | REVISION DESCRIPTION | REV. DATE | REMARK |
|------|---|--------------|----------------------|
| X01 | INITIAL RELEASE | 2008. 09. 03 | |
| X02 | <ul style="list-style-type: none"> ■ Add the information of module weight ■ Add the lifetime specifications ■ Add the panel electrical specifications ■ Add the application circuit | 2008. 11. 10 | Page 5, 6, 7, 8 & 15 |
| A01 | <ul style="list-style-type: none"> ■ Transfer from X version | 2009. 02. 09 | |

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1. SCOPE

The purpose of this specification is to define the general provisions and quality requirements that apply to the supply of display cells manufactured by RiTdisplay. This document, together with the Module Ass'y Drawing, is the highest-level specification for this product. It describes the product, identifies supporting documents and contains specifications.

2. WARRANTY

RiTdisplay warrants that the products delivered pursuant to this specification (or order) will conform to the agreed specifications for twelve (12) months from the shipping date ("Warranty Period"). RiTdisplay is obligated to repair or replace the products which are found to be defective or inconsistent with the specifications during the Warranty Period without charge, on condition that the products are stored or used as the conditions specified in the specifications. Nevertheless, RiTdisplay is not obligated to repair or replace the products without charge if the defects or inconsistency are caused by the force majeure or the reckless behaviors of the customer.

After the Warranty Period, all repairs or replacements of the products are subject to charge.

3. FEATURES

- Small molecular organic light emitting diode.
- Color : Yellow.
- Panel matrix : 256x64.
- Driver IC : SSD1322.
- Excellent Quick response time : 10 μ s.
- Extremely thin thickness for best mechanism design : 2.01mm.
- High contrast : 2000:1.
- Wide viewing angle : 160°.
- 8-bit 6800/8080-series parallel interface, 3/4-wire Serial Peripheral Interface.
- Wide range of operating temperature : -40 to 70 °C.
- Anti-glare polarizer.

4. MECHANICAL DATA

| NO | ITEM | SPECIFICATION | UNIT |
|----|-------------------|--------------------------------|-----------------|
| 1 | Dot Matrix | 256 (W) x 64 (H) | dot |
| 2 | Dot Size | 0.289 (W) x 0.289 (H) | mm ² |
| 3 | Dot Pitch | 0.309 (W) x 0.309 (H) | mm ² |
| 4 | Aperture Rate | 88 | % |
| 5 | Active Area | 79.084 (W) x 19.756 (H) | mm ² |
| 6 | Panel Size | 87.4 (W) x 28.5 (H) | mm ² |
| 7 | Panel Thickness | 2.01 | mm |
| 8 | Module Size | 87.4 (W) x 51.3 (H) x 2.01 (T) | mm ³ |
| 9 | Diagonal A/A size | 3.2 | inch |
| 10 | Module Weight | 11.03 ± 10% | gram |

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5. MAXIMUM RATINGS

| ITEM | MIN | MAX | UNIT | Condition | Remark |
|-----------------------------|--------|-----|------|--|-------------------|
| Supply Voltage (V_{CI}) | -0.3 | 4 | V | Ta = 25°C | IC maximum rating |
| Supply Voltage (V_{CC}) | 10 | 21 | V | Ta = 25°C | IC maximum rating |
| Operating Temp. | -40 | 70 | °C | | |
| Storage Temp | -40 | 85 | °C | | |
| Humidity | | 85 | % | | |
| Life Time | 24,000 | - | Hrs | 100 cd/m ² , 50% checkerboard | Note (1) |
| Life Time | 26,000 | - | Hrs | 90 cd/m ² , 50% checkerboard | Note (2) |
| Life Time | 30,000 | - | Hrs | 80 cd/m ² , 50% checkerboard | Note (3) |

(A) Under VCC = 14.5V, Ta = 25°C, 50% RH.

(B) Life time is defined the amount of time when the luminance has decayed to less than 50% of the initial measured luminance.

(1) Setting of 100 cd/m² :

- Contrast setting : 0x74
- Frame rate : 105Hz
- Duty setting : 1/64

(2) Setting of 90 cd/m² :

- Contrast setting : 0x58
- Frame rate : 105Hz
- Duty setting : 1/64

(3) Setting of 80 cd/m² :

- Contrast setting : 0x4a
- Frame rate : 105Hz
- Duty setting : 1/64

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6. ELECTRICAL CHARACTERISTICS

6.1 D.C ELECTRICAL CHARACTERISTICS

| SYMBOL | PARAMETERS | TEST CONDITION | MIN | TYP | MAX | UNIT |
|-------------------|---|---|---------------------------|------|---------------------------|------|
| V _{CC} | Operating Voltage | - | 14 | 14.5 | 15 | V |
| V _{CI} | Low voltage power supply | - | 2.4 | 2.8 | 3.5 | V |
| V _{DDIO} | Power Supply for I/O pins | - | 1.65 | 1.8 | V _{CI} | V |
| V _{IH} | High Logic Input Level | - | 0.8* V _{DDIO} | - | V _{DDIO} | V |
| V _{IL} | Low Logic Input Level | - | 0 | - | 0.2* V _{DDIO} | V |
| V _{OH} | High Logic Output Level | I _{OUT} = 100uA | 0.9* V _{DDIO} | - | V _{DDIO} | V |
| V _{OL} | Low Logic Output Level | I _{OUT} = 100uA | 0 | - | 0.1* V _{DDIO} | V |
| I _{CC} | VCC Supply Current | V _{CI} = 2.8V, V _{CC} = 18V, V _{DDIO} = 2.8V, Display ON, No panel attached, contrast = FF | External VDD = 2.5V | 2.2 | 2.6 | mA |
| | | | Internal VDD = 2.5V | 2.2 | 2.6 | |
| I _{CI} | VCI Supply Current | V _{CI} = 2.8V, V _{CC} = 18V, V _{DDIO} = 2.8V, Display ON, No panel attached, contrast = FF | External VDD = 2.5V | 35 | 45 | uA |
| | | | Internal VDD = 2.5V | 170 | 220 | |
| I _{DDIO} | VDDIO Supply Current | V _{CI} = 2.8V, V _{CC} = 18V, V _{DDIO} = 2.8V, Display ON, No panel attached, contrast = FF | External VDD = 2.5V | 40 | 50 | uA |
| | | | Internal VDD = 2.5V | 40 | 50 | |
| ISEG | Segment Output Current Setting V _{CC} =20V, I _{REF} =10uA | Contrast = FF | 310 | 340 | 370 | uA |
| | | Contrast = 7F | - | 170 | - | uA |
| | | Contrast = 3F | - | 85 | - | uA |

Note 1: V_{CI}= 2.8 V ; V_{CC}= 14.5V ; Frame rate= 105Hz ; No panel attached.

Note 2: The Vcc input must keep in a stable value; ripple and noise are not allowed.

6.2 ELECTRO-OPTICAL CHARACTERISTICS

PANEL ELECTRICAL SPECIFICATIONS

| PARAMETER | MIN | TYP. | MAX | UNITS | COMMENTS |
|--------------------------------|--------|------|------|-------------------|-----------------------------------|
| Normal mode current | | 42 | 44 | mA | All pixels on (1) |
| Standby mode current | | 4 | 5 | mA | Standby mode 10% pixels on (2) |
| Normal mode power consumption | | 609 | 638 | mW | All pixels on (1) |
| Standby mode power consumption | | 58 | 72.5 | mW | Standby mode 10% pixels on (2) |
| Normal mode Luminance | 80 | 90 | | cd/m ² | Display Average |
| Standby mode Luminance | | 20 | | cd/m ² | Display Average |
| CIE _x (Yellow) | 0.43 | 0.47 | 0.51 | | x, y (CIE 1931) |
| CIE _y (Yellow) | 0.45 | 0.49 | 0.53 | | |
| Dark Room Contrast | 2000:1 | | | | |
| Viewing Angle | 160 | | | degree | |
| Response Time | | 10 | | μs | |

(1) Normal mode condition :

- Driving Voltage : 14.5V
- Contrast setting : 0x58
- Frame rate : 105Hz
- Duty setting : 1/64

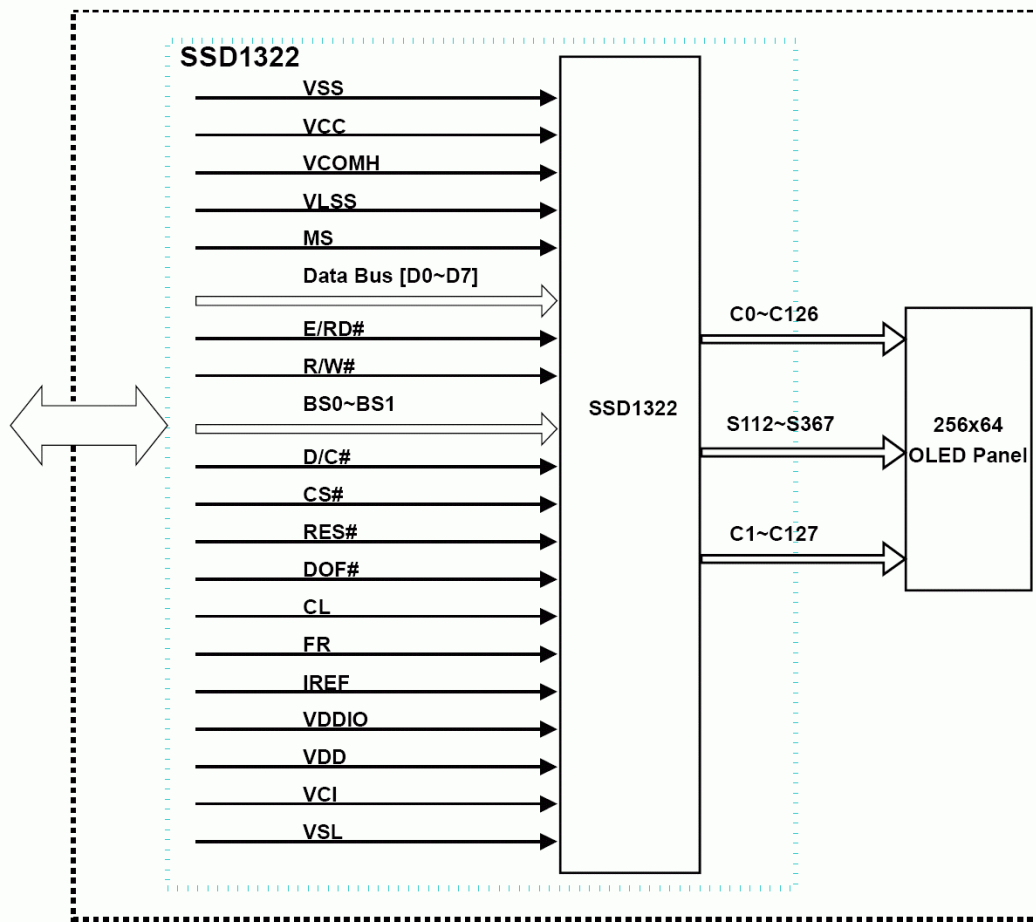
(2) Standby mode condition :

- Driving Voltage : 14.5V
- Contrast setting : 0x0f
- Frame rate : 105Hz
- Duty setting : 1/64

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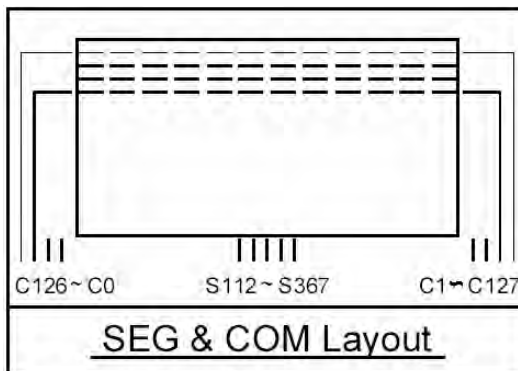
7. INTERFACE

7.1 FUNCTION BLOCK DIAGRAM



RiTdisplay 256x64 OLED Module

7.2 PANEL LAYOUT DIAGRAM



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7.3 PIN ASSIGNMENTS

| PIN NAME | PIN NO. | DESCRIPTION |
|----------|---------|---|
| NC | 1 | No connection. |
| VSS | 2 | Ground pin. |
| NC | 3 | No connection. |
| VCC | 4 | Power supply for panel driving voltage. |
| VCOMH | 5 | COM signal deselected voltage level. A capacitor should be connected between this pin and VSS. |
| VLSS | 6 | Analog system ground pin. |
| MS | 7 | This pin must be connected to VDDIO to enable the chip. |
| D7 | 8 | These pins are bi-directional data bus connecting to the MCU data bus. |
| D6 | 9 | |
| D5 | 10 | |
| D4 | 11 | |
| D3 | 12 | |
| D2 | 13 | |
| D1 | 14 | |
| D0 | 15 | |
| E/RD# | 16 | When connecting to an 8080-microprocessor, this pin receives the Read (RD#) signal. Read operation is initiated when this pin is pulled LOW and the chip is selected. When serial interface is selected, this pin E(RD#) must be connected to VSS. |
| R/W# | 17 | When 8080 interface mode is selected, this pin will be the Write (WR#) input. Data write operation is initiated when this pin is pulled LOW and the chip is selected. When serial interface is selected, this pin R/W (WR#) must be connected to VSS. |
| BS0 | 18 | MCU bus interface selection pins. |
| BS1 | 19 | |
| DC# | 20 | This pin is Data/Command control pin connecting to the MCU. |
| CS# | 21 | This pin is the chip select input connecting to the MCU. The chip is enabled for MCU communication only when CS# is pulled LOW. |
| RES# | 22 | This pin is reset signal input. When the pin is pulled LOW, initialization of the chip is executed. |
| DOF# | 23 | This pin is No Connection pins. |
| CL | 24 | External clock input pin. |
| FR | 25 | This pin is No Connection pins. |
| IREF | 26 | A resistor should be connected between this pin and VSS. |
| VDDIO | 27 | Power supply for interface logic level. It should be matched with the MCU interface voltage level. |
| VDD | 28 | Power supply pin for core logic operation. A capacitor is required to connect between this pin and VSS. |

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| | | |
|------|----|--|
| VCI | 29 | Low voltage power supply. VCI must always be equal to or higher than VDD and VDDIO. |
| VSL | 30 | This is segment voltage reference pin. When external VSL is used, connect with resistor and diode to ground. |
| VLSS | 31 | Analog system ground pin. |
| NC | 32 | No connection. |
| VCC | 33 | Power supply for panel driving voltage. |
| NC | 34 | No connection. |

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7.4 GRAPHIC DISPLAY DATA RAM ADDRESS MAP

The GDDRAM address map shows the GDDRAM in Gray Scale mode. Since in Gray Scale mode, there are 16 gray levels. Therefore four bits (one nibble) are allocated for each pixel.

For example D30480[3:0] corresponds to the pixel located in (COM127, SEG2). So the lower nibble and higher nibble of D0, D1, D2, ..., D30717, D30718, D30719 represent the 480x128 data nibbles in the GDDRAM.

GDDRAM in Gray Scale mode (RESET)

| | SEG0 | SEG1 | SEG2 | SEG3 | SEG476 | SEG477 | SEG478 | SEG479 | SEG Outputs RAM Column address (HEX) |
|--------|------|-------------|-------------|--------------------|-------------|-------------|-------------|-------------|--------------------------------------|
| | 00 | | 00 | | 77 | | 77 | | |
| COM0 | 00 | D1[3:0] | D1[7:4] | D0[3:0] | D0[7:4] | D239[3:0] | D239[7:4] | D238[3:0] | D238[7:4] |
| COM1 | 01 | D241[3:0] | D241[7:4] | D240[3:0] | D240[7:4] | D479[3:0] | D479[7:4] | D478[3:0] | D478[7:4] |
| ... | ... | ... | ... | ... | ... | ... | ... | ... | ... |
| COM126 | 7E | D30241[3:0] | D30241[7:4] | D30240[3:0] | D30240[7:4] | D30479[3:0] | D30479[7:4] | D30478[3:0] | D30478[7:4] |
| COM127 | 7F | D30481[3:0] | D30481[7:4] | D30480[3:0] | D30480[7:4] | D30719[3:0] | D30719[7:4] | D30718[3:0] | D30718[7:4] |

RAM Row Address (HEX)

COM Outputs Address (HEX)

Corresponding to one pixel

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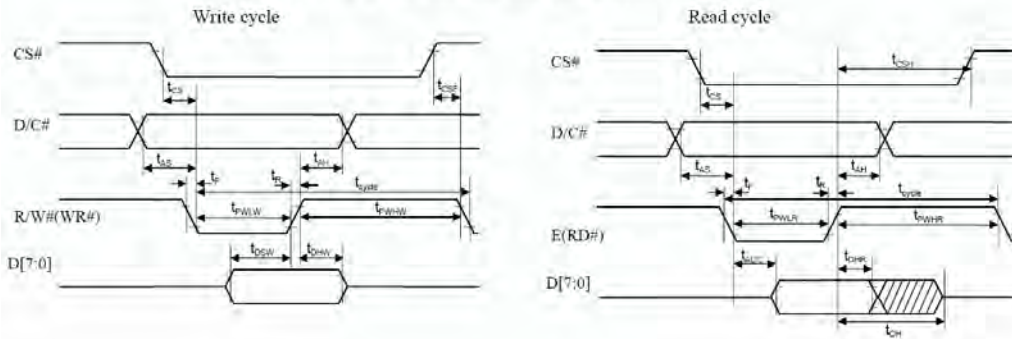
7.5 INTERFACE TIMING CHART

8080-Series MCU Parallel Interface Timing Characteristics

($V_{DD} - V_{SS} = 2.4$ to $2.6V$, $V_{DDIO} = 1.6V$, $V_{CI} = 3.3V$, $T_A = 25^\circ C$)

| Symbol | Parameter | Min | Typ | Max | Unit |
|-------------|--------------------------------------|-----|-----|-----|------|
| t_{cycle} | Clock Cycle Time | 300 | - | - | ns |
| t_{AS} | Address Setup Time | 10 | - | - | ns |
| t_{AH} | Address Hold Time | 0 | - | - | ns |
| t_{DSW} | Write Data Setup Time | 40 | - | - | ns |
| t_{DHW} | Write Data Hold Time | 7 | - | - | ns |
| t_{DHR} | Read Data Hold Time | 20 | - | - | ns |
| t_{OH} | Output Disable Time | - | - | 70 | ns |
| t_{ACC} | Access Time | - | - | 140 | ns |
| t_{PWLW} | Read Low Time | 150 | - | - | ns |
| t_{PWLW} | Write Low Time | 60 | - | - | ns |
| t_{PWHR} | Read High Time | 60 | - | - | ns |
| t_{PWHW} | Write High Time | 60 | - | - | ns |
| t_R | Rise Time | - | - | 15 | ns |
| t_F | Fall Time | - | - | 15 | ns |
| t_{CS} | Chip select setup time | 0 | - | - | ns |
| t_{CSH} | Chip select hold time to read signal | 0 | - | - | ns |
| t_{CSF} | Chip select hold time | 20 | - | - | ns |

8080-series MCU parallel interface characteristics



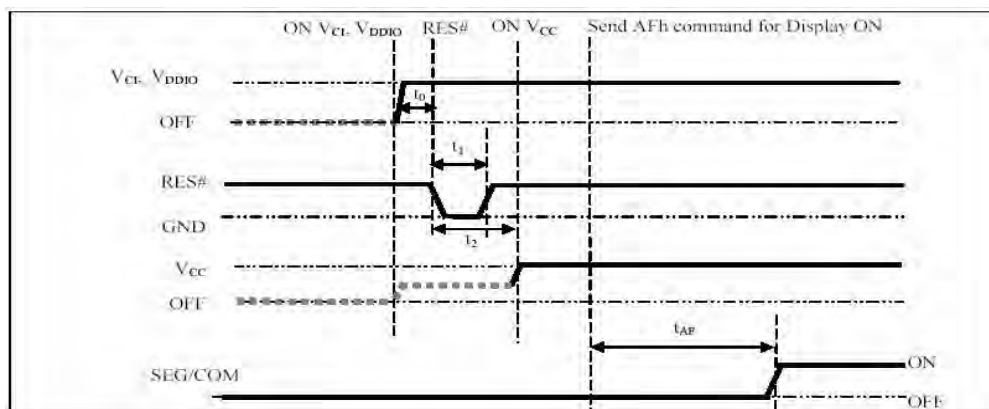
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8. POWER ON / OFF SEQUENCE & APPLICATION CIRCUIT

8.1 POWER ON / OFF SEQUENCE

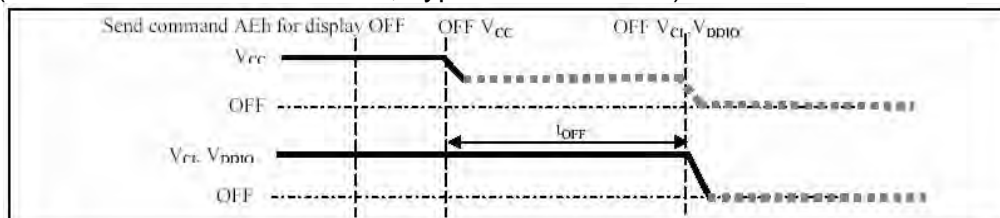
Power ON sequence:

1. Power ON V_{CI}, V_{DDIO} .
2. After V_{CI}, V_{DDIO} become stable, set wait time at least 1ms (t_0) for internal V_{DD} become stable. Then set RES# pin LOW (logic low) for at least 100us (t_1)⁽⁴⁾ and then HIGH (logic high).
3. After set RES# pin LOW (logic low), wait for at least 100us (t_2). Then Power ON V_{CC} .⁽¹⁾
4. After V_{CC} become stable, send command AFh for display ON. SEG/COM will be ON after 200ms (t_{AF}).



Power OFF sequence:

1. Send command AEh for display OFF.
2. Power OFF V_{CC} .^{(1), (2)}
3. Wait for t_{OFF} . Power OFF V_{CI}, V_{DDIO} .
 (where Minimum $t_{OFF}=80ms$ ⁽³⁾, Typical $t_{OFF}=100ms$)

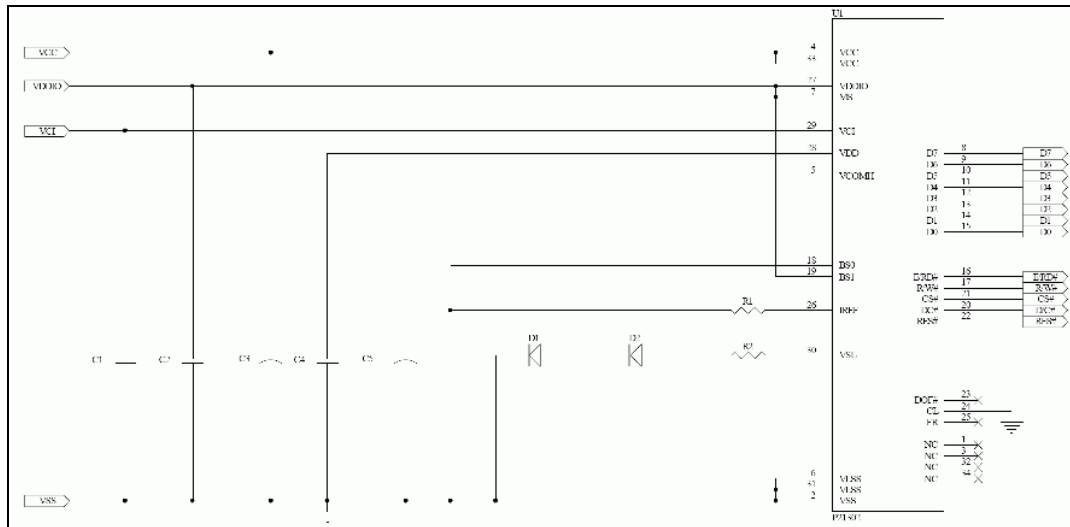


Note:

- (1). Since an ESD protection circuit is connected between V_{CI}, V_{DDIO} and V_{CC} , V_{CC} becomes lower than V_{CI} whenever V_{CI}, V_{DDIO} is ON and V_{CC} is OFF as shown in the dotted line of V_{CC} in Figure.
- (2). V_{CC} should be kept float (disable) when it is OFF.
- (3). V_{CI}, V_{DDIO} should not be Power OFF before V_{CC} Power OFF.
- (4). The register values are reset after t_1 .
- (5). Power pins (V_{DD}, V_{CC}) can never be pulled to ground under any circumstance.

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8.2 APPLICATION CIRCUIT



Recommend components:

- C1, C2, C4: 1uF/16V(0805)
- C3, C5: 4.7uF/35V (Tantalum type) or VISHAY (572D475X0025A2T)
- R1: 430K ohm 1%(0603)
- R2: 50 ohm 1/4W
- D1, D2: RB480K(ROHM)

This circuit is for 8080 8bits interface.

8.3 COMMAND TABLE

Refer to SSD1322 IC Spec.

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9. RELIABILITY TEST CONDITIONS

| No. | Items | Specification | Quantity |
|-----|--|---|----------|
| 1 | High temp. (Non-operation) | 85°C, 240hrs | 5 |
| 2 | High temp. (Operation) | 70°C, 120hrs | 5 |
| 3 | Low temp. (Operation) | -40°C, 120hrs | 5 |
| 4 | High temp. / High humidity (Operation) | 65°C, 90%RH, 120hrs | 5 |
| 5 | Thermal shock (Non-operation) | -40°C ~85°C (-40°C /30min; transit /3min; 85°C /30min; transit /3min) 1cycle: 66min, 100 cycles | 5 |
| 6 | Vibration | Frequency : 5~50HZ, 0.5G Scan rate : 1 oct/min Time : 2 hrs/axis Test axis : X, Y, Z | 1 Carton |
| 7 | Drop | Height: 120cm Sequence : 1 angle \ 3 edges and 6 faces Cycles: 1 | 1 Carton |
| 8 | ESD (Non-operation) | Air discharge model, ±8kV, 10 times | 5 |

Test and measurement conditions

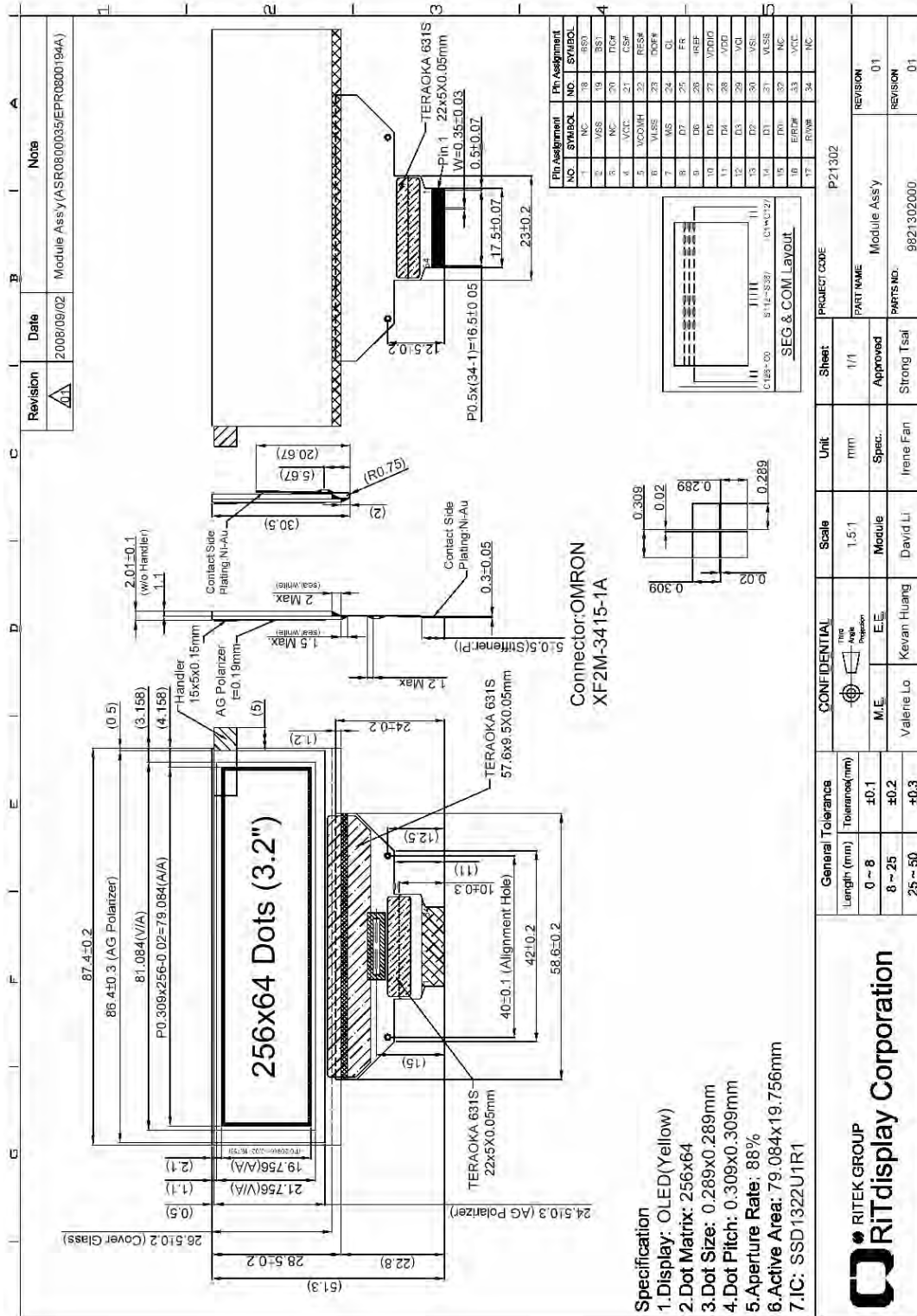
1. All measurements shall not be started until the specimens attain to temperature stability.
2. All-pixels-on is used as operation test pattern.
3. The degradation of Polarizer are ignored for item 1, 4 & 5.

Evaluation criteria

1. The function test is OK.
2. No observable defects.
3. Luminance: > 50% of initial value.
4. Current consumption: within \pm 50% of initial value.

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10. EXTERNAL DIMENSION



11. PACKING SPECIFICATION

| Revision | Date | Note |
|----------|------------|--------------------------|
| A1 | 2008/09/02 | Packing Tray Instruction |

| Item | Part No. | Description | QTY |
|------|------------|---------------------------------------|-----|
| 1 | 8821302000 | P21302 Module Assy | 360 |
| 2 | 3008000079 | Tray 330x270x8.6mm, PS, H=0.7mm | 32 |
| 3 | 3000000002 | 5G Silica dryer | 8 |
| 4 | 3003000012 | Vacuum bag 480x285x90mm | 2 |
| 5 | 3003000016 | Antistatic Bubble Bag 440x(350+450)mm | 2 |
| 6 | 3001000005 | Pizza Box 345x285x88, corrugated | 2 |
| 7 | 3000000009 | Carton 385x305x203mm | 1 |
| 8 | 3006000000 | Label | 3 |
| 9 | 3208000125 | Tape W=48mm, L=910cm | |

| General Tolerance | | Scale | | Unit | | Sheet | |
|-------------------|---------------|-------------|-------|-------------|--------------|-------|--------------------------|
| Length (mm) | Tolerance(mm) | 1:3.5 | mm | 1/1 | PROJECT CODE | | P21302 |
| 0 ~ 8 | ±0.1 | Module | Spec. | Approved: | PART NAME | | Packing Tray Instruction |
| 8 ~ 25 | ±0.2 | M.E. | Spec. | Strong Tsai | PARTS NO. | | 9921302000 |
| 25 ~ 50 | ±0.3 | Valerie Lo | Spec. | Irene Fan | REVISION | | 01 |
| | | Kevan Huang | Spec. | David Li | REVISION | | 01 |

12. APPENDIXES

APPENDIX 1: DEFINITIONS

A. DEFINITION OF CHROMATICITY COORDINATE

The chromaticity coordinate is defined as the coordinate value on the CIE 1931 color chart for R, G, B, W.

B. DEFINITION OF CONTRAST RATIO

The contrast ratio is defined as the following formula:

$$\text{Contrast Ratio} = \frac{\text{Luminance of all pixels on measurement}}{\text{Luminance of all pixels off measurement}}$$

C. DEFINITION OF RESPONSE TIME

The definition of turn-on response time T_r is the time interval between a pixel reaching 10% of steady state luminance and 90% of steady state luminance. The definition of turn-off response time T_f is the time interval between a pixel reaching 90% of steady state luminance and 10% of steady state luminance. It is shown in Figure 2.

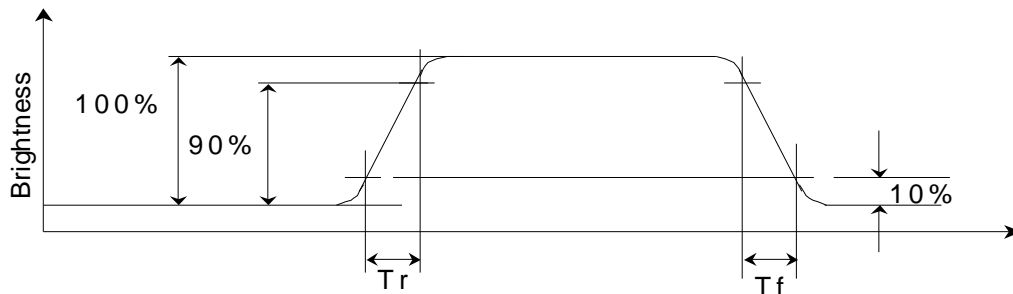


Figure 2 Response time

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D. DEFINITION OF VIEWING ANGLE

The viewing angle is defined as Figure 3. Horizontal and vertical (H & V) angles are determined for viewing directions where luminance varies by 50% of the perpendicular value.

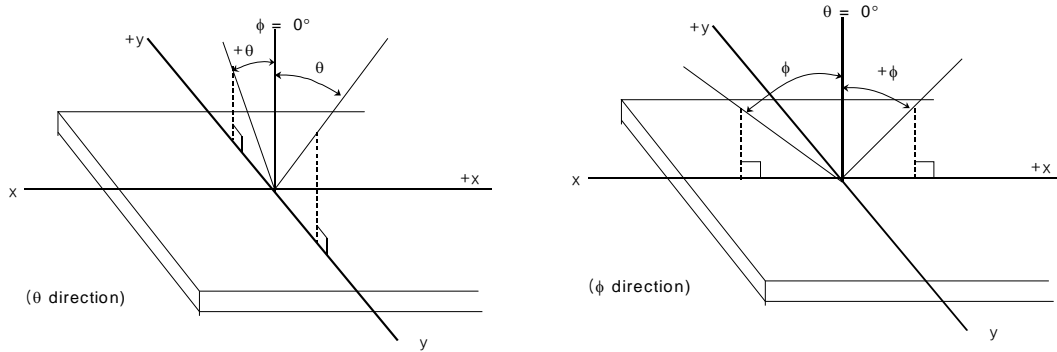


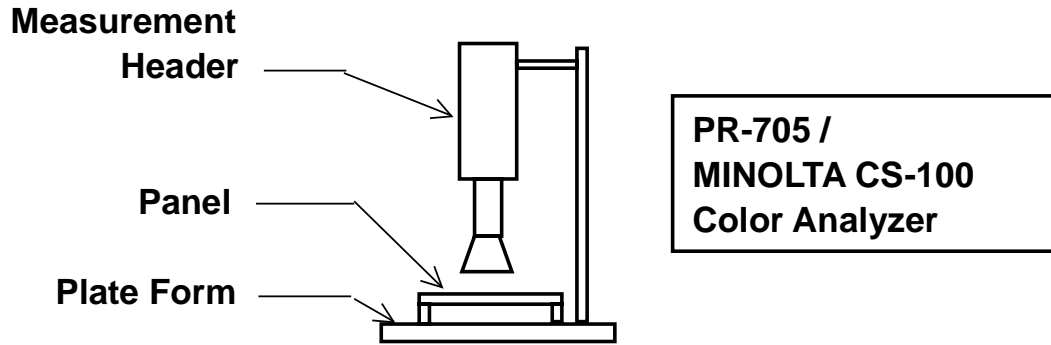
Figure 3 Viewing angle

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APPENDIX 2: MEASUREMENT APPARATUS

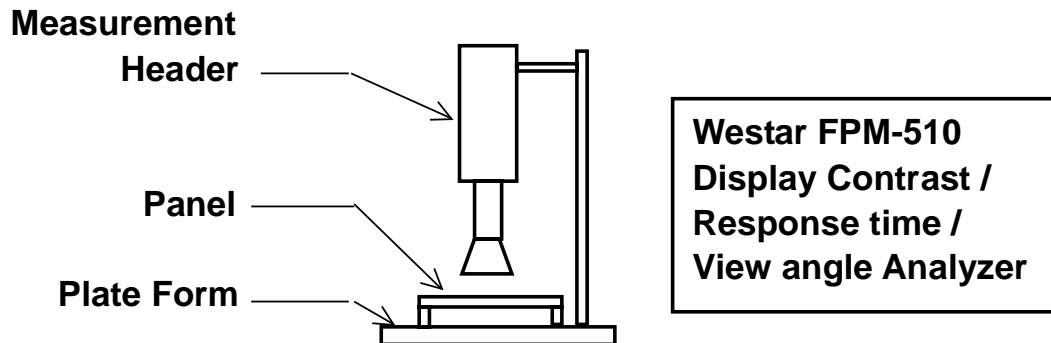
A. LUMINANCE/COLOR COORDINATE

PHOTO RESEARCH PR-705, MINOLTA CS-100



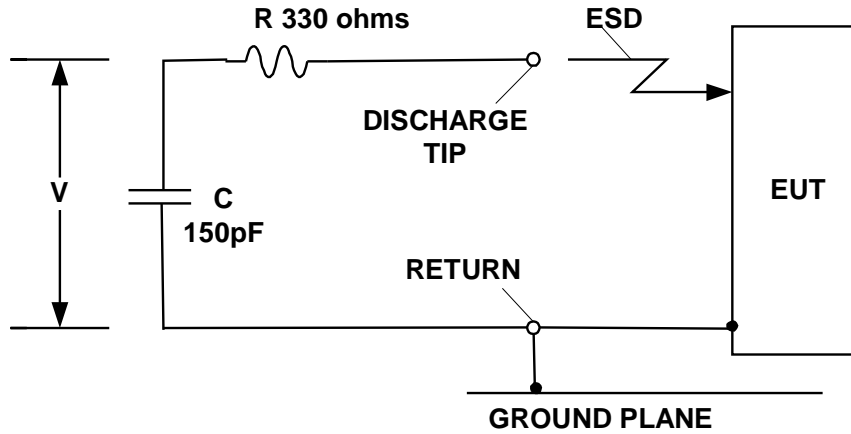
B. CONTRAST / RESPONSE TIME / VIEW ANGLE

WESTAR CORPORATION FPM-510



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C. ESD ON AIR DISCHARGE MODE



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APPENDIX 3: PRECAUTIONS

A. RESIDUE IMAGE

Because the pixels are lighted in different time, the luminance of active pixels may reduce or differ from inactive pixels. Therefore, the residue image will occur. To avoid the residue image, every pixel needs to be lighted up uniformly.

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Displays

US Micro Products is an industrial distributor specializing in engineered display solutions. We dedicate ourselves to providing the best in displays for the medical, industrial, gaming, automotive, aerospace, military and consumer markets.

OLEDs



TFT Display



Open Frame Monitors



Passive LCDs



Multitouch



Touch Screen



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Peripheral Devices

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Keyboards



Trackballs



Aerospace Trackballs



Printers

