



**US Micro Products**  
*Electronic Products for the OEM*

# OLED PRODUCT SPECIFICATION

Manufactured by:



<b>PART NUMBER:</b>	<b>USMP-P20101</b>
<b>DESCRIPTION:</b>	1.12" OLED, 262k Full Color, 96x3x96 Resolution, COG, SEPS114

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## REVISION RECORD

REV.	REVISION DESCRIPTION	REV. DATE	REMARK
X01	INITIAL RELEASE	2008.01.14	
X02	<ul style="list-style-type: none"> <li>■ Add the information of module weight</li> <li>■ Modify lifetime specification</li> <li>■ Modify panel electrical specifications</li> <li>■ Add power on / off sequence</li> <li>■ Add the application circuit</li> <li>■ Modify polarizer</li> </ul>	2008.03.20	Page 5, 6, 7, 8, 15, 16 & 18
A01	<ul style="list-style-type: none"> <li>■ Transfer from X version</li> <li>■ Add the packing specification</li> </ul>	2008.08.05	Page 19
A02	<ul style="list-style-type: none"> <li>■ Modify polarizer</li> </ul>	2008.09.12	Page 4, 5 & 18
A03	<ul style="list-style-type: none"> <li>■ Modify polarizer</li> <li>■ Modify definition of panel thickness</li> <li>■ Modify power on/off sequence</li> </ul>	2009.06.19	Page 4, 5, 6, 8, 15, 16 & 19
A04	<ul style="list-style-type: none"> <li>■ Modify seal color (white→black)</li> </ul>	2010.07.19	Page 19

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## **1. SCOPE**

The purpose of this specification is to define the general provisions and quality requirements that apply to the supply of display cells manufactured by RiTdisplay. This document, together with the Module Assembly Drawing, is the highest-level specification for this product. It describes the product, identifies supporting documents and contains specifications, which are either not addressed, or are exceptions to the supporting documents.

## **2. WARRANTY**

RiTdisplay warrants that the products delivered pursuant to this specification (or order) will conform to the agreed specifications for twelve (12) months from the shipping date ("Warranty Period"). RiTdisplay is obligated to repair or replace the products which are found to be defective or inconsistent with the specifications during the Warranty Period without charge, on condition that the products are stored or used as the conditions specified in the specifications. Nevertheless, RiTdisplay is not obligated to repair or replace the products without charge if the defects or inconsistency are caused by the force majeure or the reckless behaviors of the customer.

After the Warranty Period, all repairs or replacements of the products are subject to charge.

## **3. FEATURES**

- Small molecular organic light emitting diode.
- Color :65K colors
- Panel matrix : 96\*3\*96
- Driver IC : SEPS114A
- Excellent Quick response time : 10 $\mu$ s
- Extremely thin thickness for best mechanism design : 1.21 mm
- High contrast : 2000:1
- Wide viewing angle : 160°
- Strong environmental resistance.
- 68/80series MPU 8-bit, SPI 4-wire interface.
- Wide range of operating temperature : -40 to 70°C
- Anti-glare polarizer.

#### **4. MECHANICAL DATA**

NO	ITEM	SPECIFICATION	UNIT
1	Dot Matrix	96 (W) x (RxGxB) x 96 (H)	dot
2	Dot Size	0.045 (W) x 0.19 (H)	mm <sup>2</sup>
3	Dot Pitch	0.07 (W) x 0.21 (H)	mm <sup>2</sup>
4	Aperture Rate	58	%
5	Active Area	20.135 (W) x 20.14 (H)	mm <sup>2</sup>
6	Panel Size	27 (W) x 30.1 (H)	mm <sup>2</sup>
7*	Panel Thickness	1.02 ± 0.1	mm
8	Module Size	27 (W) x 40.1 (H) x 1.21 (D)	mm <sup>3</sup>
9	Diagonal A/A size	1.12	inch
10	Module Weight	2.05 ± 10%	gram

\* Panel thickness includes substrate glass, cover glass and UV glue thickness.

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## 5. MAXIMUM RATING

ITEM	MIN	MAX	UNIT	Condition	Remark
Supply Voltage ( $V_{DD}$ )	-0.3	4	V	$T_a = 25^\circ\text{C}$	IC maximum rating
Supply Voltage ( $V_{CC}$ )	8	18	V	$T_a = 25^\circ\text{C}$	IC maximum rating
Operating Temp.	-40	70	$^\circ\text{C}$		
Storage Temp	-40	85	$^\circ\text{C}$		
Humidity		85	%		
Life Time	10,000	-	Hrs	100 $\text{cd}/\text{m}^2$ , 50% checkerboard	Note (1)
Life Time	13,000	-	Hrs	80 $\text{cd}/\text{m}^2$ , 50% checkerboard	Note (2)
Life Time	16,000	-	Hrs	60 $\text{cd}/\text{m}^2$ , 50% checkerboard	Note (3)

Note:

(A) Under  $V_{CC} = 15\text{V}$ ,  $T_a = 25^\circ\text{C}$ , 50% RH.

(B) Life time is defined the amount of time when the luminance has decayed to less than 50% of the initial measured luminance.

(1) Setting of 100 $\text{cd}/\text{m}^2$  :

- Blue contrast setting : 0x70
- Green contrast setting : 0x57
- Red contrast setting : 0x4d
- Frame rate : 105Hz
- Duty setting : 1/96

(2) Setting of 80 $\text{cd}/\text{m}^2$  :

- Blue contrast setting : 0x59
- Green contrast setting : 0x45
- Red contrast setting : 0x3f
- Frame rate : 105Hz
- Duty setting : 1/96

(3) Setting of 60 $\text{cd}/\text{m}^2$  :

- Blue contrast setting : 0x45
- Green contrast setting : 0x35
- Red contrast setting : 0x30
- Frame rate : 105Hz
- Duty setting : 1/96

## 6. ELECTRICAL CHARACTERISTICS

### 6.1 D.C ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETERS	CONDITIONS	MIN	TYP	MAX	UNIT
VCC	Driver Power Supply (For OLED Panel)	-	14.5	15	15.5	V
VDD	Logic Power Supply	-	2.4	2.8	3.3	V
VDDIO	Logic I/O Operating Voltage	-	1.65	-	3.3	V
VIH	High logic input voltage	-	0.8*VDDIO	-	VDDIO	V
VIL	Low logic input voltage	-	0	-	0.4	V
VOH	High logic output voltage	IOH = -0.1mA	VDDIO-0.4	-	-	V
VOL	Low logic output voltage	IOL = -0.1mA	-	-	0.4	V
ILI	Input leakage current	VI = VSS or VDDIO	-1	-	1	uA
ILO	Output leakage current	VI = VSS or VDDIO	-1	-	1	uA
FOSCE	Oscillator frequency By external resistor	RF = 27KΩ	-	-	3	MHz

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## 6.2 ELECTRO-OPTICAL CHARACTERISTICS

### PANEL ELECTRICAL SPECIFICATIONS

PARAMETER	MIN	TYP.	MAX	UNITS	COMMENTS
Normal mode current		13	14	mA	All pixels on (1)
Standby mode current		2	3	mA	Standby mode 10% pixels on (2)
Normal mode power consumption		195	210	mW	All pixels on (1)
Standby mode power consumption		30	45	mW	Standby mode 10% pixels on (2)
Normal mode Luminance	60	80		cd/m <sup>2</sup>	Display Average
Standby mode Luminance		20		cd/m <sup>2</sup>	
CIE <sub>x</sub> (White)	0.24	0.28	0.32		x, y (CIE 1931)
CIE <sub>y</sub> (White)	0.28	0.32	0.36		
CIE <sub>x</sub> (Red)	0.62	0.66	0.70		
CIE <sub>y</sub> (Red)	0.29	0.33	0.37		
CIE <sub>x</sub> (Green)	0.26	0.30	0.34		
CIE <sub>y</sub> (Green)	0.59	0.63	0.67		
CIE <sub>x</sub> (Blue)	0.10	0.14	0.18		
CIE <sub>y</sub> (Blue)	0.14	0.18	0.22		
Dark Room Contrast	2000:1				
Viewing Angle	160			degree	
Response Time		10		μs	

(1) Normal mode condition :

- Driving Voltage : 15V
- Blue contrast setting : 0x59
- Green contrast setting : 0x45
- Red contrast setting : 0x3f
- Frame rate : 105Hz
- Duty setting : 1/96

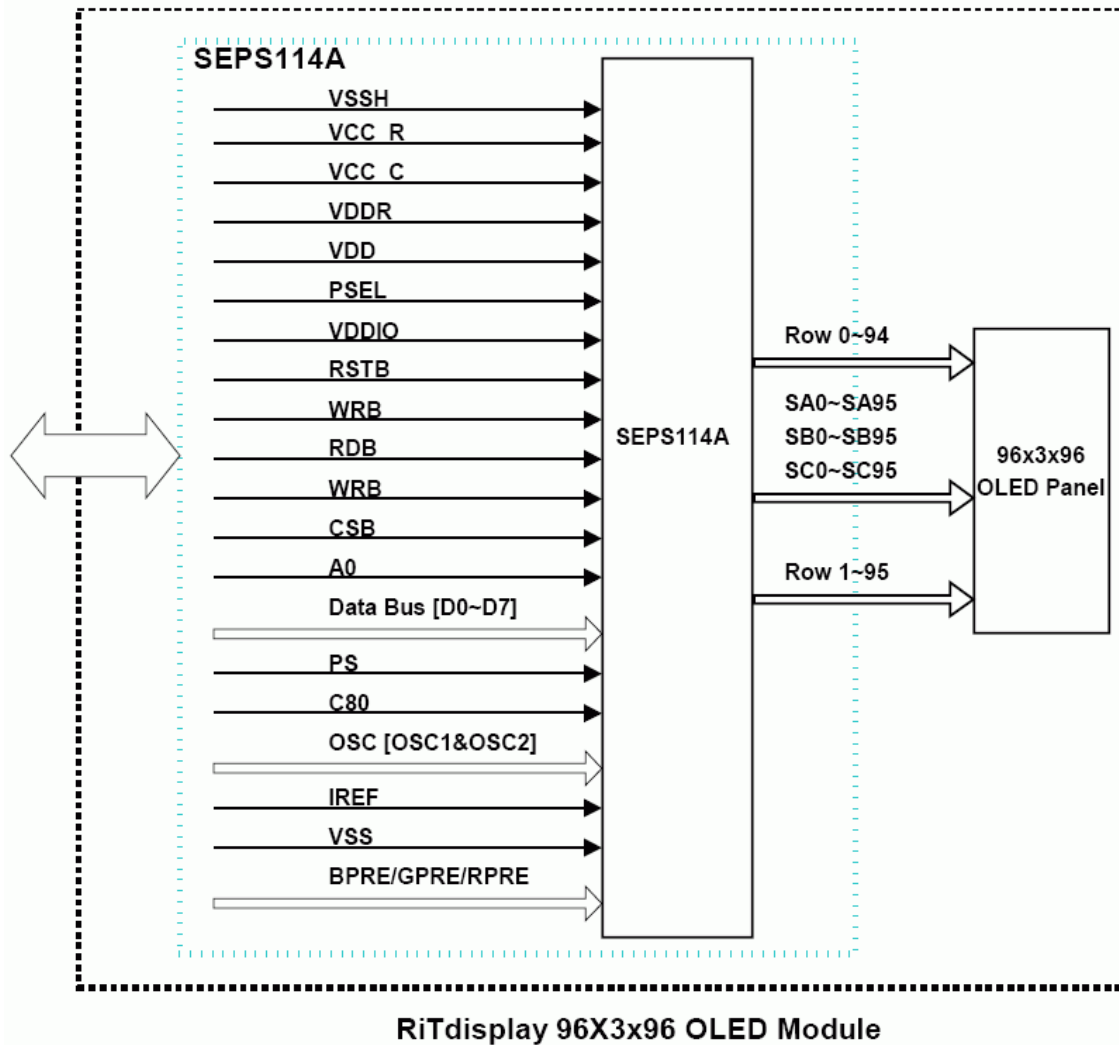
(2) Standby mode condition :

- Driving Voltage : 15V
- Blue contrast setting : 0x1f
- Green contrast setting : 0x17
- Red contrast setting : 0x16
- Frame rate : 105Hz
- Duty setting : 1/96

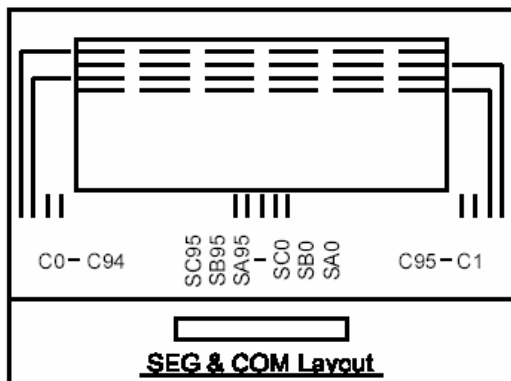


## 7. INTERFACE

### 7.1 FUNCTION BLOCK DIAGRAM



### 7.2 PANEL LAYOUT DIAGRAM



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### 7.3 PIN ASSIGNMENTS

PIN NO	PIN NAME	DESCRIPTION
1	NC	No connection.
2	VSSH	Ground for VCC_C/VCC_R
3	VCC_R	Power Supply for Scan Driver
4	VCC_C	Data Driver Power Supply
5	VDDR	Logic Power Supply2
6	VDD	Logic Power Supply
7	PSEL	Regulator Enable/Disable for Logic Power Supply2
8	VDDIO	MPU I/F PAD Power Supply VDDIO should be lower than VDD or the same as VDD.
9	RSTB	Reset Signal Input (active low)
10	WRB	For an 80-serise bus interface, write strobe signal (active low) For an 68-serise bus interface, read/write select Low: Write, High: Read When using SPI, fix it to VDDIO or VSS level
11	RDB	For an 80-serise bus interface, read strobe signal (active low) For an 68-serise bus interface, bus enable strobe (active high) When using SPI, fix it to VDDIO or VSS level
12	CSB	Selects the chip Low: chip is selected and can be accessed High: chip is not selected and cannot be accessed
13	A0	Selects the data / command Low: command, High: parameter / data
14	D0	bi- directional data bus
15	D1	bi- directional data bus
16	D2	bi- directional data bus
17	D3	bi- directional data bus
18	D4	bi- directional data bus
19	D5	bi- directional data bus
20	D6	bi- directional data bus
21	D7	bi- directional data bus
22	PS	Selects parallel/Serial interface type Low: serial, High: parallel
23	C80	Selects the MPU type Low: 80- Series Interface, High: 68- Series Interface
24	OSC1	Please connect external resistor between OSC1 and OSC2.
25	OSC2	
26	IREF	Tie resistor to VSS
27	VSS	Ground for VDD/VDDR
28	BPRE	Pre- Charge Voltage for Blue

29	GPRES	Pre- Charge Voltage for Green
30	RPRE	Pre- Charge Voltage for Red
31	VCC_C	Data Driver Power Supply
32	VCC_R	Power Supply for Scan Driver
33	VSSH	Ground for VCC_C/VCC_R
34	NC	No connection.

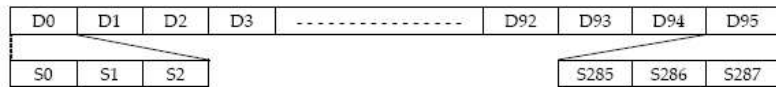
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### 7.4 GRAPHIC DISPLAY DATA RAM ADDRESS MAP

The DDRAM stores pixel data for the display. It is composed of 96 -row by 96 -column x 16 -bit addressable array. Address counter provides row and column address to DDRAM for access display pixel data from MPU.

#### Relationship between DDRAM Address and Display Position

G0	G95	00h											
G1	G94	01h											
G2	G93	02h											
G3	G92	03h											
G4	G91	04h											
G5	G90	05h											
⋮	⋮	⋮											
⋮	⋮	⋮											
⋮	⋮	⋮											
⋮	⋮	⋮											
G90	G5	59h											
G91	G4	5Ah											
G92	G3	5Bh											
G93	G2	5Ch											
G94	G1	5Eh											
G95	G0	5Fh											
SCAND=0	SCAND=2	Column Data	0	1	2	3	⋮	92	93	94	95		



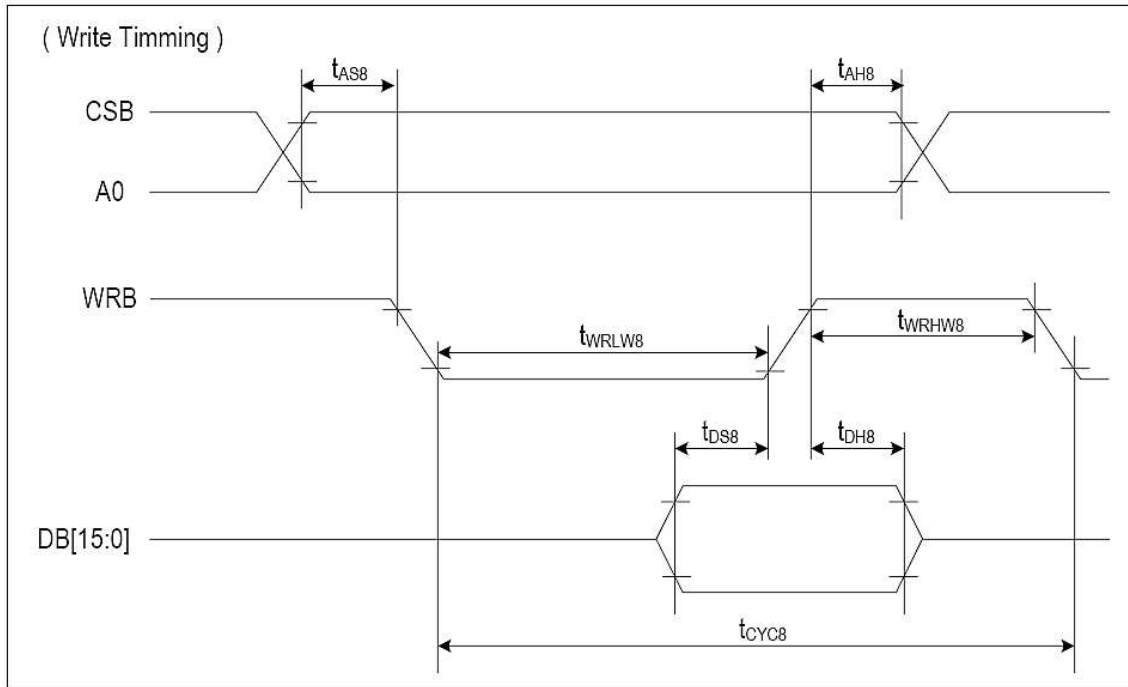
SCAND[1:0] : Row scan direction register(09h).

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### 7.5 INTERFACE TIMING CHART

System BUS Read/Write Timing (80 series CPU interface)

#### Write Timing



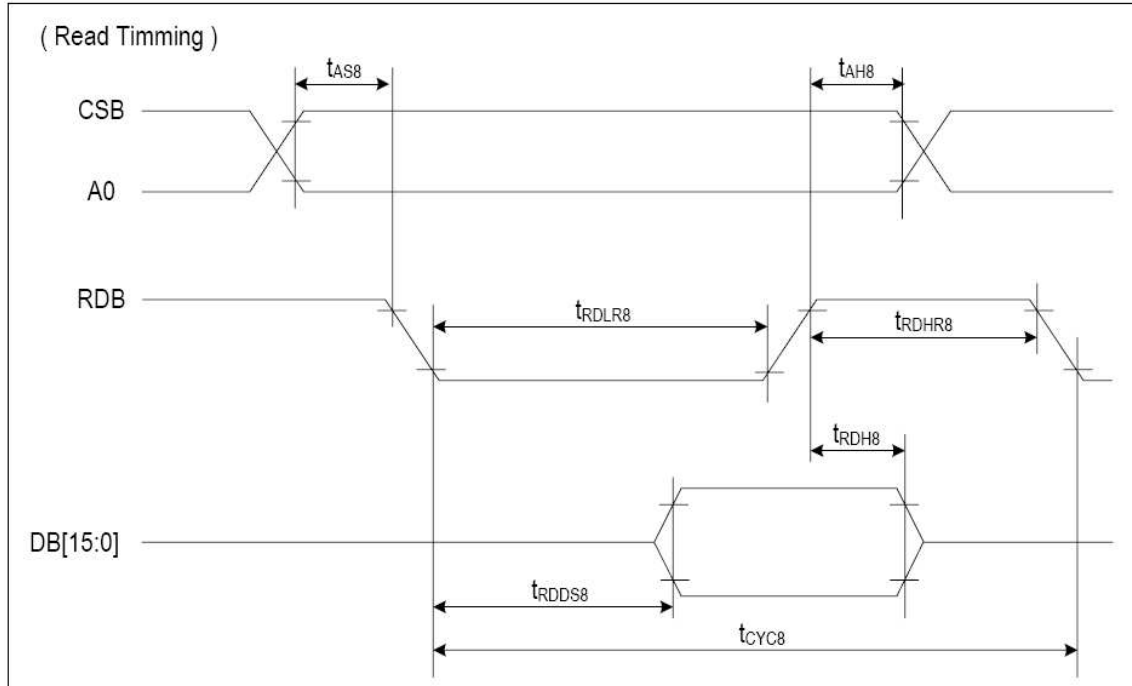
(VDD = 2.8V, Ta = 25°C)

ITEM	SYMBOL	CONDITION	MIN	MAX	UNIT	PORT
Address hold timing	$t_{AH8}$	-	5	-	ns	CSB
Address setup timing	$t_{AS8}$	-	5	-	ns	A0
System cycle timing	$t_{CYC8}$	-	100	-	ns	
Write "L" pulse width	$t_{WRLW8}$	-	45	-	ns	WRB
Write "H" pulse width	$t_{WRHW8}$	-	45	-	ns	
Data setup timing	$t_{DS8}$	-	30	-	ns	DB[15:0]
Data hold timing	$t_{DH8}$	-	10	-	ns	

notice ) All the timing reference is 10% and 90% of VDDIO.

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**Read Timing**



(VDD = 2.8V, Ta = 25°C)

ITEM	SYMBOL	CONDITION	MIN	MAX	UNIT	PORT
Address hold timing	$t_{AH8}$	-	5	-	ns	CSB
Address setup timing	$t_{AS8}$	-	5	-	ns	A0
System cycle timing	$t_{CYC8}$	-	200	-	ns	
Read "L" pulse width	$t_{RDLR8}$	-	90	-	ns	RDB
Read "H" pulse width	$t_{RDHR8}$	-	90	-	ns	
Read data output delay time	$t_{RDH8}$	CL = 15 pF	-	60	ns	DB[15:0]
Data hold timing	$t_{RDDS8}$	CL = 15 pF	0	-	ns	

Notice) All the timing reference is 10% and 90% of VDDIO.

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## **8. POWER ON / OFF SEQUENCE & APPLICATION CIRCUIT**

### **8.1 POWER ON / OFF SEQUENCE**

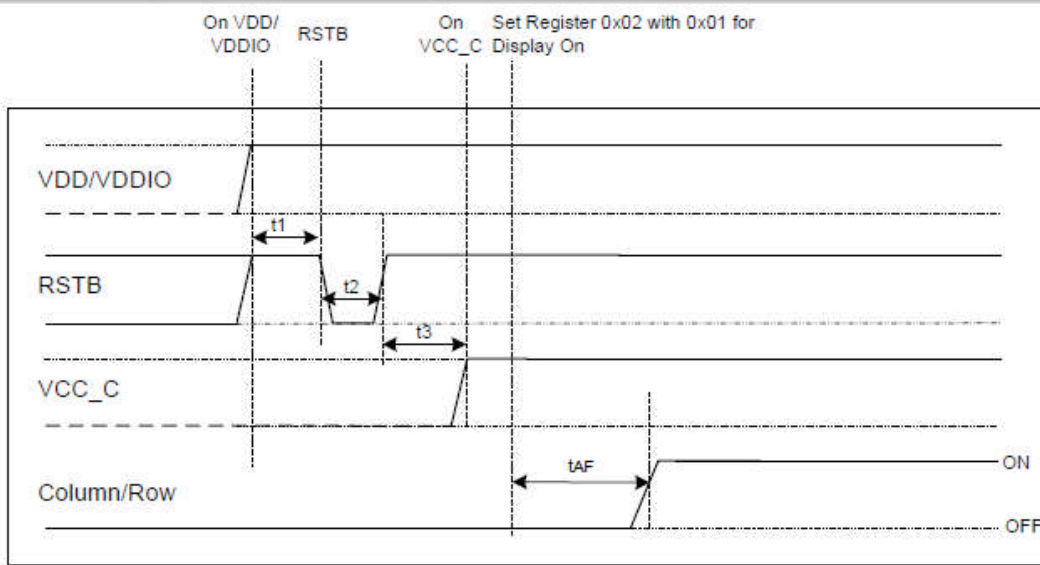
The following figures illustrate the recommended power ON and OFF sequence of SEPS114A.

#### **Power ON sequence**

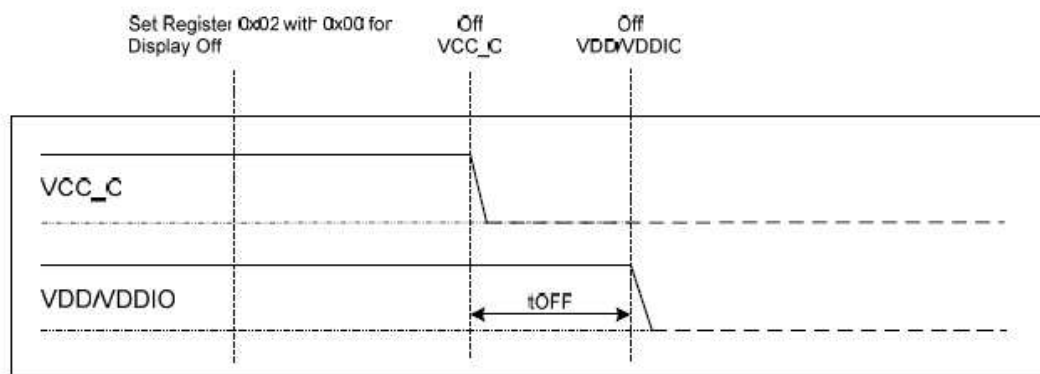
1. Power ON VDD, VDDIO.
2. After VDD, VDDIO become stable and wait for 100ms( $t_1$ ), set RSTB pin LOW (logic low) for at least 1ms ( $t_2$ ) and then HIGH(logic high).
3. After set RSTB pin HIGH (logic high), wait for at least 50ms ( $t_3$ ). Then Power ON VCC\_C
4. After VCC\_C become stable, set register 0x02 with value 0x01 for display ON.  
Data/Scan will be ON after 200ms ( $t_{AF}$ ).

#### **Power OFF sequence**

1. Set register 0x02 with value 0x00 for display OFF.
2. Power OFF VCC\_C.
3. Wait for  $t_{OFF}$ . Power OFF VDD, VDDIO (where Minimum  $t_{OFF}$ =0ms, Typical  $t_{OFF}$ =100ms)



<Power On Sequence>



<Power Off Sequence>

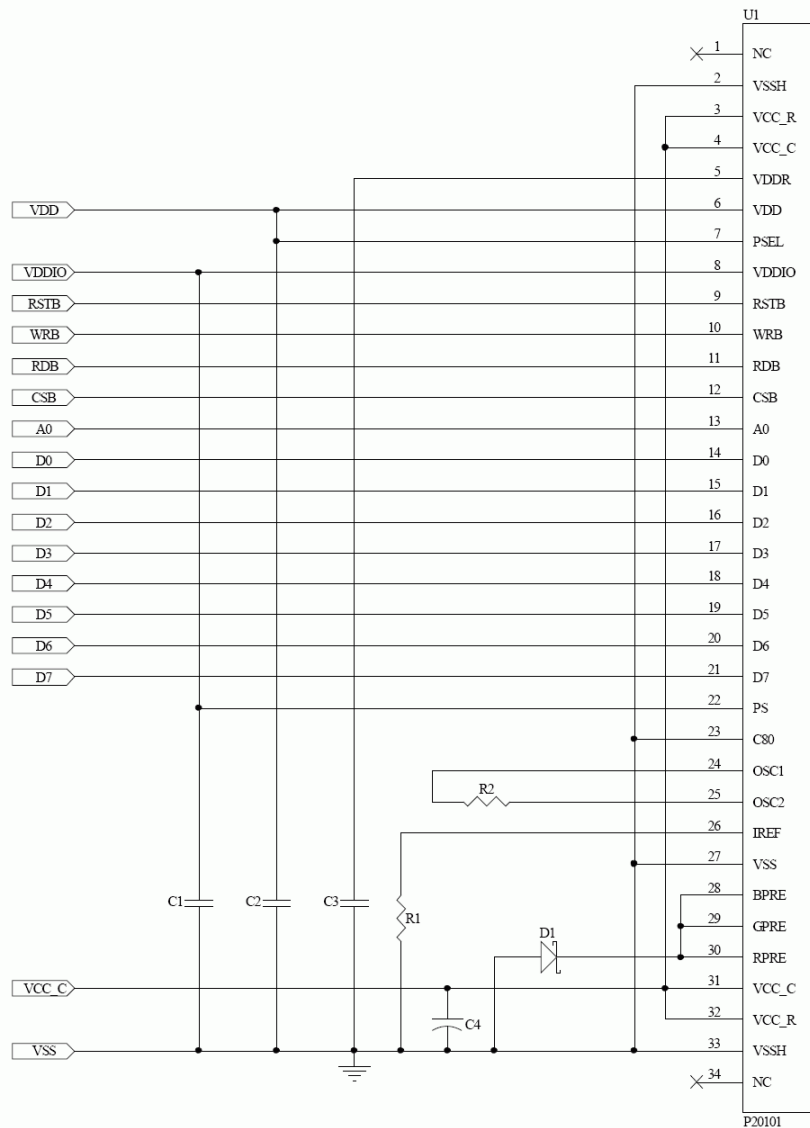
**Note:**

Since ESD protection circuit is connected between VDD, VDDIO and VCC\_C, VCC\_C becomes lower than VDD whenever VDD, VDDIO is ON and VCC\_C is OFF. VCC\_C should be disabled when it is OFF.

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## 8.2 APPLICATION CIRCUIT



### Recommend components:

C1, C2, C3: 1uF/16V(0603)

C4: 4.7uF/25V or 35V (Tantalum type) or VISHAY (572D475X0025A2T)

R1: 39K ohm (0603) 1%

R2: 27K ohm (0603) 1%

D1: UDZSTE-172.7B (zener diode)

**This circuit is for 8080 8bits interface.**

## 8.3 COMMAND TABLE

Refer to IC Spec.: SEPS114A

## **9. RELIABILITY TEST CONDITIONS**

No.	Items	Specification	Quantity
1	High temp. (Non-operation)	85°C, 240hrs	5
2	High temp. (Operation)	70°C, 120hrs	5
3	Low temp. (Operation)	-40°C, 120hrs	5
4	High temp. / High humidity (Operation)	65°C, 90%RH, 96hrs	5
5	Thermal shock (Non-operation)	-40°C ~85°C (-40°C /30min; transit /3min; 85°C /30min; transit /3min) 1cycle: 66min, 20 cycles	5
6	Vibration	Frequency : 5~50HZ, 0.5G Scan rate : 1 oct/min Time : 2 hrs/axis Test axis : X, Y, Z	1 Carton
7	Drop	Height: 120cm Sequence : 1 angle 、 3 edges and 6 faces  Cycles: 1	1 Carton
8	ESD (Non-operation)	Air discharge model, ±8kV, 10 times	5

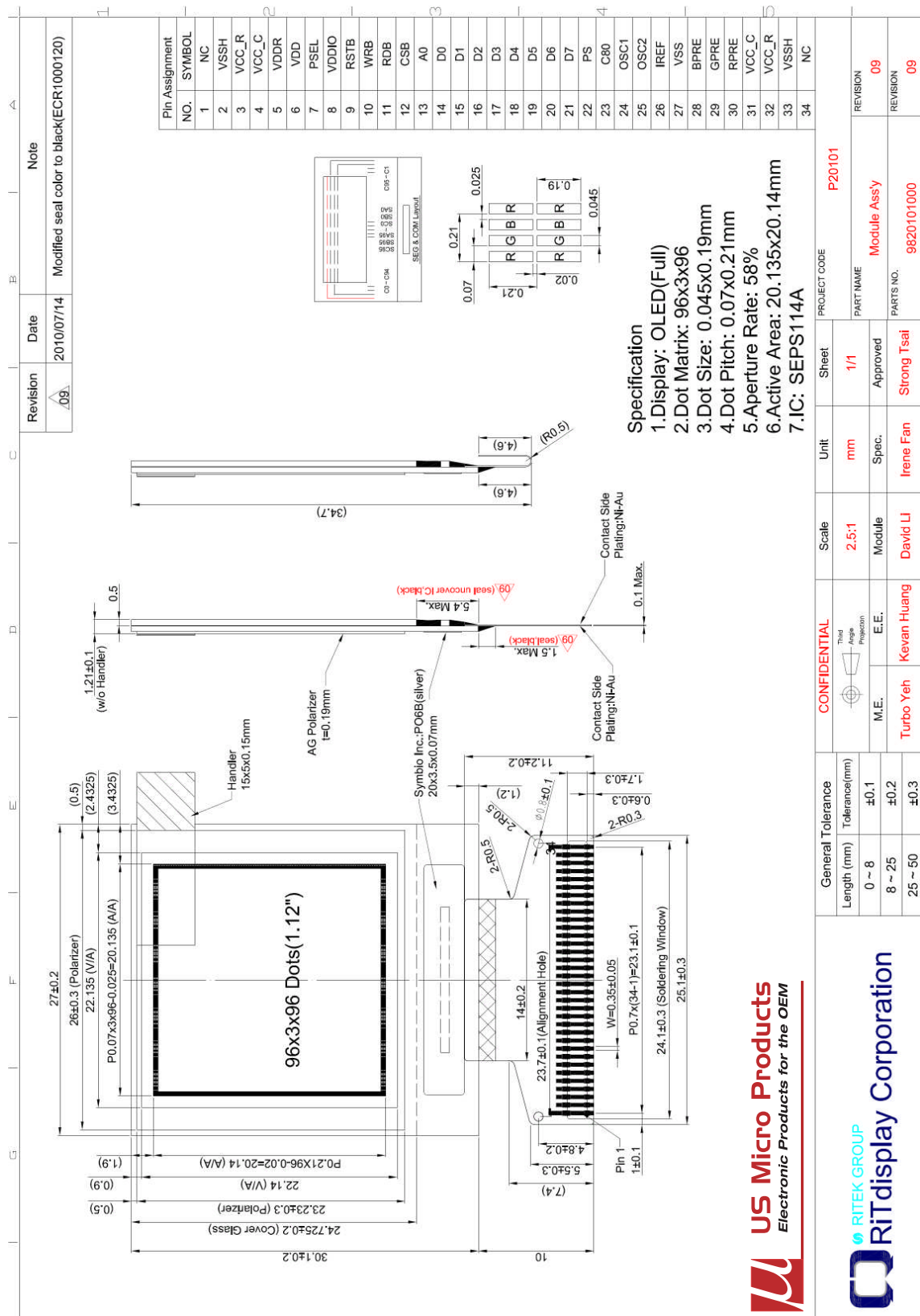
### **Test and measurement conditions**

1. All measurements shall not be started until the specimens attain to temperature stability.
2. All-pixels-on is used as operation test pattern.
3. The degradation of Polarizer are ignored for item 1, 4 & 5.

### **Evaluation criteria**

1. The function test is OK.
2. No observable defects.
3. Luminance: > 50% of initial value.
4. Current consumption: within ± 50% of initial value.

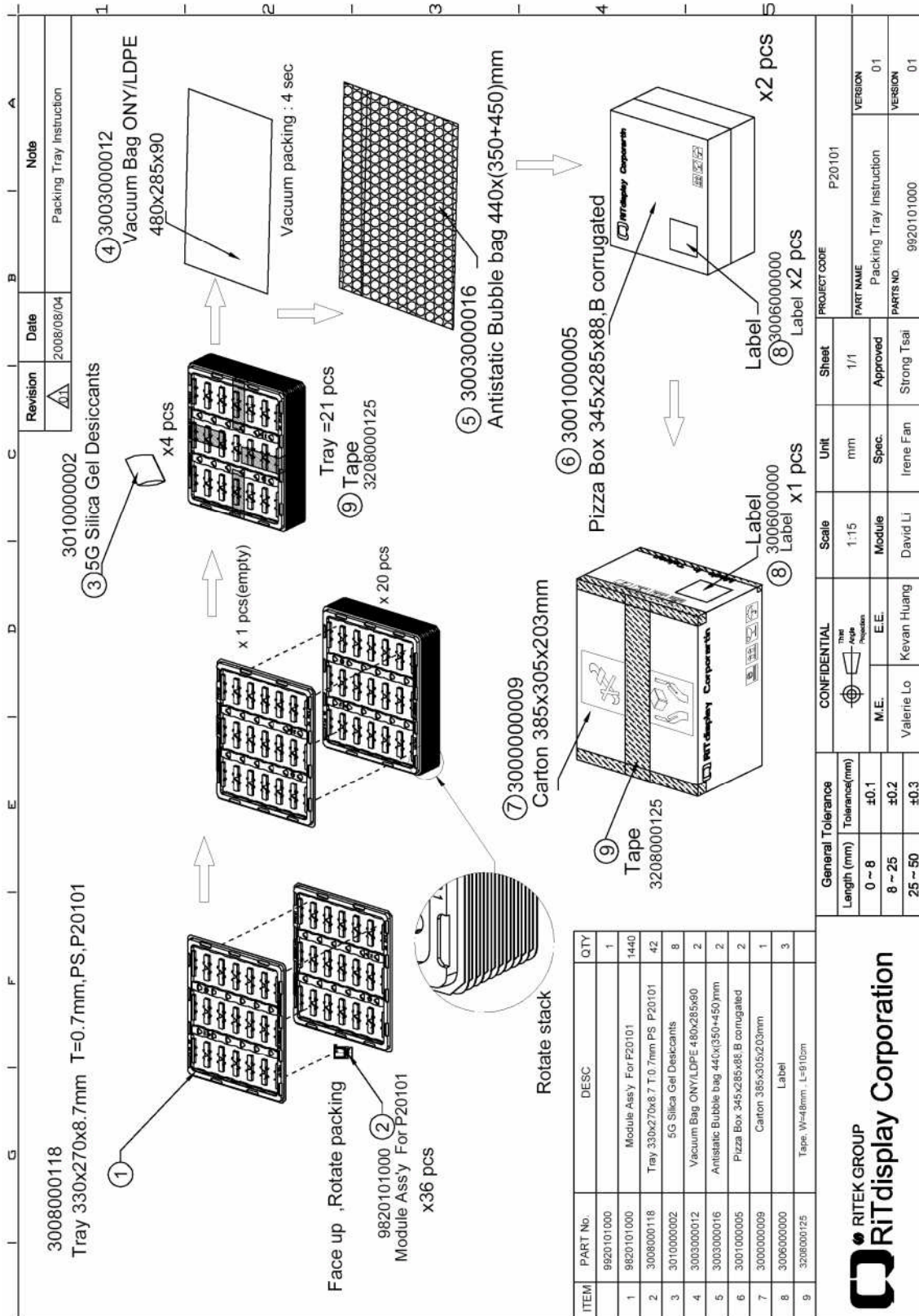
### 10. EXTERNAL DIMENSION



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**11. PACKING SPECIFICATION**



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**12. APPENDIXES**

**APPENDIX 1: DEFINITIONS**

**A. DEFINITION OF CHROMATICITY COORDINATE**

The chromaticity coordinate is defined as the coordinate value on the CIE 1931 color chart for R, G, B, W.

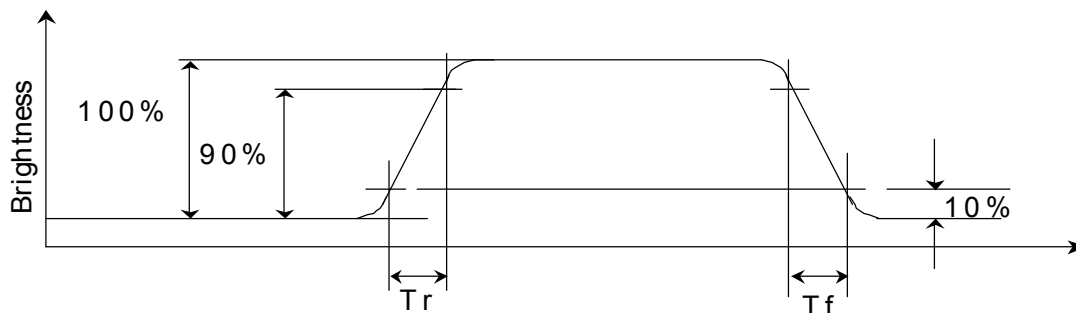
**B. DEFINITION OF CONTRAST RATIO**

The contrast ratio is defined as the following formula:

$$\text{Contrast Ratio} = \frac{\text{Luminance of all pixels on measurement}}{\text{Luminance of all pixels off measurement}}$$

**C. DEFINITION OF RESPONSE TIME**

The definition of turn-on response time  $T_r$  is the time interval between a pixel reaching 10% of steady state luminance and 90% of steady state luminance. The definition of turn-off response time  $T_f$  is the time interval between a pixel reaching 90% of steady state luminance and 10% of steady state luminance. It is shown in Figure 2.

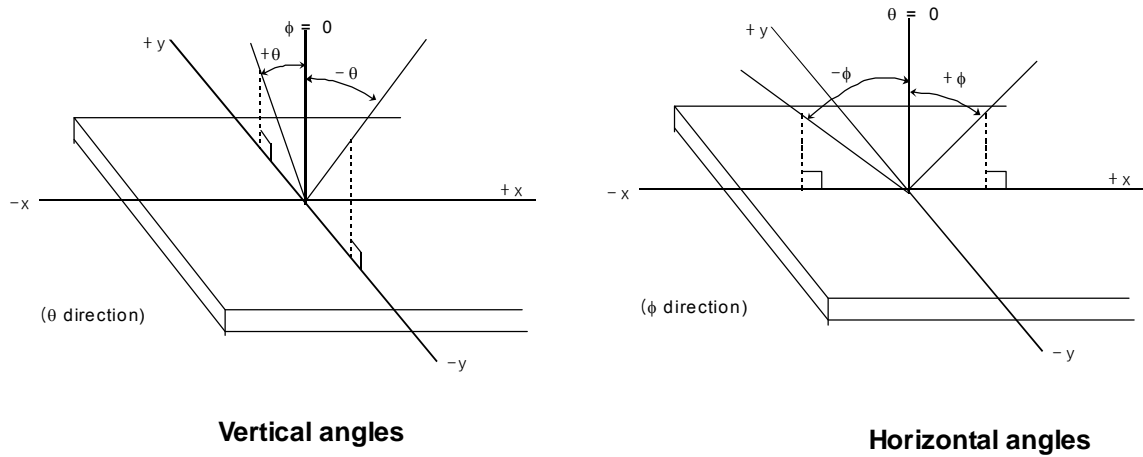


**Figure 2: Response time**

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**D. DEFINITION OF VIEWING ANGLE**

The viewing angle is defined as Figure 3. Horizontal and vertical (H & V) angles are determined for viewing directions where luminance varies by 50% of the perpendicular value.



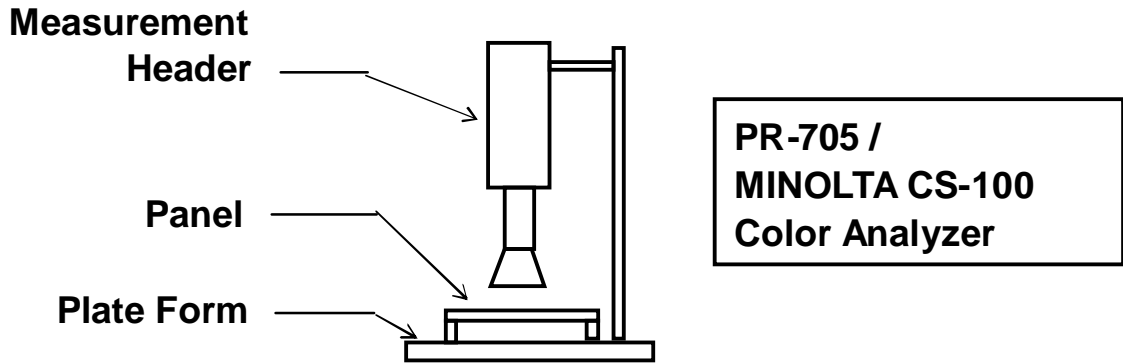
**Figure 3: Viewing Angle**

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**APPENDIX 2: MEASUREMENT APPARATUS**

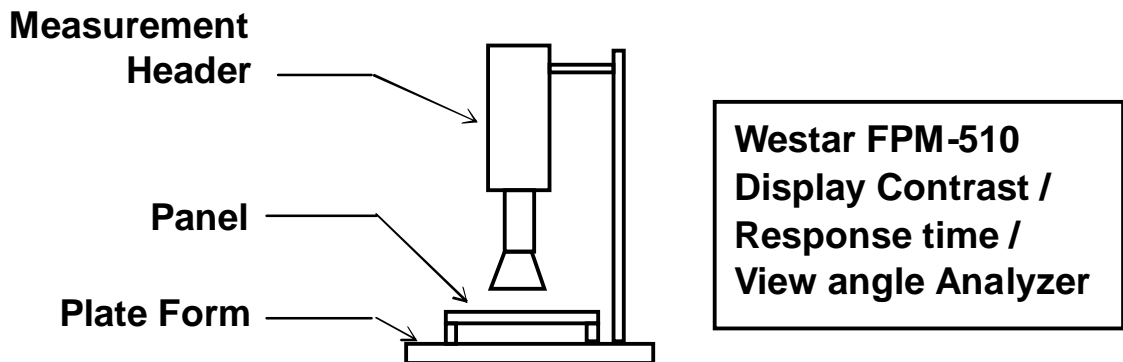
**A. LUMINANCE/COLOR COORDINATE**

PHOTO RESEARCH PR-705, MINOLTA CS-100



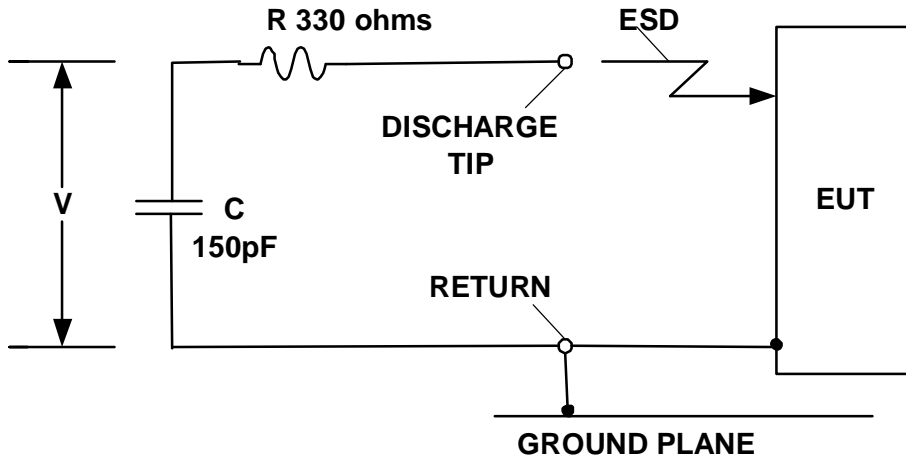
**B. CONTRAST / RESPONSE TIME / VIEW ANGLE**

WESTAR CORPORATION FPM-510



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**C. ESD ON AIR DISCHARGE MODE**



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## APPENDIX 3: PRECAUTIONS

### A. RESIDUE IMAGE

Because the pixels are lighted in different time, the luminance of active pixels may reduce or differ from inactive pixels. Therefore, the residue image will occur. To avoid the residue image, every pixel needs to be lighted up uniformly.

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