



**US Micro Products**  
*Electronic Products for the OEM*

# OLED PRODUCT SPECIFICATION

Manufactured by:



<b>PART NUMBER:</b>	<b>USMP-P19101</b>
<b>DESCRIPTION:</b>	<b>3.1", 256x32, Monochrome White, COF, SSD1326 IC</b>

<b>ISSUE DATE</b>	<b>APPROVED BY (Customer Use Only)</b>	<b>CHECKED BY</b>	<b>PREPARED BY</b>
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## REVISION RECORD

REV.	REVISION DESCRIPTION	REV. DATE	REMARK
X01	INITIAL RELEASE	2007. 10. 18	
X02	<ul style="list-style-type: none"> <li>■ Add the operating conditions for different luminance</li> <li>■ Add the panel electrical specifications</li> <li>■ Modify power off sequence</li> <li>■ Add the application circuit</li> </ul>	2007. 12. 26	Page 6, 7, 8, 16 & 17
X03	<ul style="list-style-type: none"> <li>■ Modify tape &amp; polarizer dimension</li> </ul>	2008. 02. 13	Page 19
A01	<ul style="list-style-type: none"> <li>■ Transfer from X version</li> <li>■ Add the information of module weight</li> <li>■ Add the packing specification</li> </ul>	2008. 04. 15	Page 5 & 20
A02	<ul style="list-style-type: none"> <li>■ Add alignment line on FPC</li> </ul>	2008. 06. 06	Page 19

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## **1. SCOPE**

The purpose of this specification is to define the general provisions and quality requirements that apply to the supply of display cells manufactured by RiTdisplay. This document, together with the Module Assembly Drawing, is the highest-level specification for this product. It describes the product, identifies supporting documents and contains specifications.

## **2. WARRANTY**

RiTdisplay warrants that the products delivered pursuant to this specification (or order) will conform to the agreed specifications for twelve (12) months from the shipping date ("Warranty Period"). RiTdisplay is obligated to repair or replace the products which are found to be defective or inconsistent with the specifications during the Warranty Period without charge, on condition that the products are stored or used as the conditions specified in the specifications. Nevertheless, RiTdisplay is not obligated to repair or replace the products without charge if the defects or inconsistency are caused by the force majeure or the reckless behaviors of the customer.

After the Warranty Period, all repairs or replacements of the products are subject to charge.

## **3. FEATURES**

- Small molecular organic light emitting diode.
- Color : White
- Panel matrix : 256\*32
- Driver IC : SSD1326
- Excellent quick response time.
- Extremely thin thickness for best mechanism design : 1.61mm
- High contrast : 2000:1
- Wide viewing angle : 160°
- 8-bit 6800-series Parallel Interface, 8-bit 8080-series Parallel Interface, Serial Peripheral Interface and I<sup>2</sup>C Interface.
- Wide range of operating temperature : -40 to 70 °C
- Anti-glare polarizer.

#### 4. MECHANICAL DATA

NO	ITEM	SPECIFICATION	UNIT
1	Dot Matrix	256 (W) x 32 (H)	dot
2	Dot Size	0.289 (W) x 0.289 (H)	mm <sup>2</sup>
3	Dot Pitch	0.309 (W) x 0.309 (H)	mm <sup>2</sup>
4	Aperture Rate	87	%
5	Active Area	79.084 (W) x 9.868 (H)	mm <sup>2</sup>
6	Panel Size	83.8 (W) x 18 (H)	mm <sup>2</sup>
7	Panel Thickness	1.61 ± 0.1	mm
8	Module Size	83.8 (W) x 41.2 (H) x 1.61 (D)	mm <sup>3</sup>
9	Diagonal A/A size	3.1	inch
10	Module Weight	5.28 ± 10%	gram

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## 5. MAXIMUM RATINGS

ITEM	MIN	MAX	UNIT	Condition	Remark
Supply Voltage ( $V_{DD}$ )	2.4	3.5	V	$T_a = 25^\circ\text{C}$	IC maximum rating
Supply Voltage ( $V_{CC}$ )	9	15	V	$T_a = 25^\circ\text{C}$	IC maximum rating
Operating Temp.	-40	70	$^\circ\text{C}$		
Storage Temp	-40	85	$^\circ\text{C}$		
Humidity	-	85	%		
Life Time	13,000	-	Hrs	120 $\text{cd}/\text{m}^2$ , 50% checkerboard	Note (1)
Life Time	16,000	-	Hrs	100 $\text{cd}/\text{m}^2$ , 50% checkerboard	Note (2)
Life Time	20,000	-	Hrs	80 $\text{cd}/\text{m}^2$ , 50% checkerboard	Note (3)

Note:

(A) Under  $V_{CC} = 12\text{V}$ ,  $T_a = 25^\circ\text{C}$ , 50% RH.

(B) Life time is defined the amount of time when the luminance has decayed to less than 50% of the initial measured luminance.

(1) Setting of 120 $\text{cd}/\text{m}^2$  :

- Contrast setting : D0H
- Frame rate : 105HZ
- Duty setting : 1/32

(2) Setting of 100 $\text{cd}/\text{m}^2$  :

- Contrast setting : B0H
- Frame rate : 105Hz
- Duty setting : 1/32

(3) Setting of 80 $\text{cd}/\text{m}^2$  :

- Contrast setting : 90H
- Frame rate : 105Hz
- Duty setting : 1/32

## 6. ELECTRICAL CHARACTERISTICS

### 6.1 D.C ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETERS	TEST CONDITION	MIN	TYP	MAX	UNIT
$V_{CC}$	Driver power supply (for OLED panel)	Ta=-20°C to +70°C	11.5	12	12.5	V
$V_{DD}$	Logic operating voltage	Ta=-20°C to +70°C	2.4	2.7	3.5	V
$V_{OH}$	Hi logic output level	I <sub>out</sub> =100 uA, 3.3MHZ	0.9*V <sub>DD</sub>		V <sub>DD</sub>	V
$V_{OL}$	Low logic output level	I <sub>out</sub> =100uA, 3.3MHZ	0		0.1*V <sub>DD</sub>	V
$V_{IH}$	Hi logic input level	I <sub>out</sub> =100uA, 3.3MHZ	0.8*V <sub>DD</sub>		V <sub>DD</sub>	V
$V_{IL}$	Low logic input level	I <sub>out</sub> =100uA, 3.3MHZ	0		0.2*V <sub>DD</sub>	V
$I_{CC}$	Operating current for V <sub>CC</sub> (No panel attached)	Contrast=FF		550		uA
$I_{DD}$	Operating current for V <sub>DD</sub> (No panel attached)	Contrast=FF		190		uA
$I_{SEG}$	Segment output current (No panel attached)	Contrast=FF		100		uA
		Contrast=AF		69		uA
		Contrast=3F		25		uA
		Contrast=0F		6		uA

Note : V<sub>DD</sub>=2.7 Volts ; V<sub>CC</sub>=12VDC ; Frame rate=105Hz ; No panel attached.

## 6.2 ELECTRO-OPTICAL CHARACTERISTICS

### PANEL ELECTRICAL SPECIFICATIONS

PARAMETER	MIN	TYP.	MAX	UNITS	COMMENTS
Normal mode current		24	26	mA	All pixels on (1)
Standby mode current		1	3	mA	Standby mode 10% pixels on (2)
Normal mode power consumption		288	312	mW	All pixels on (1)
Standby mode power consumption		12	36	mW	Standby mode 10% pixels on (2)
Normal Luminance	80	100		cd/m <sup>2</sup>	Display Average
Standby Luminance		10		cd/m <sup>2</sup>	Display Average
CIE <sub>x</sub> (White)	0.24	0.28	0.32		x, y (CIE 1931)
CIE <sub>y</sub> (White)	0.28	0.32	0.36		
Dark Room Contrast	2000:1				
Viewing Angle	160			degree	
Response Time		10		μs	

(1) Normal mode condition :

- Driving Voltage : 12V
- Contrast setting : 0xB0
- Frame rate : 105Hz
- Duty setting : 1/32

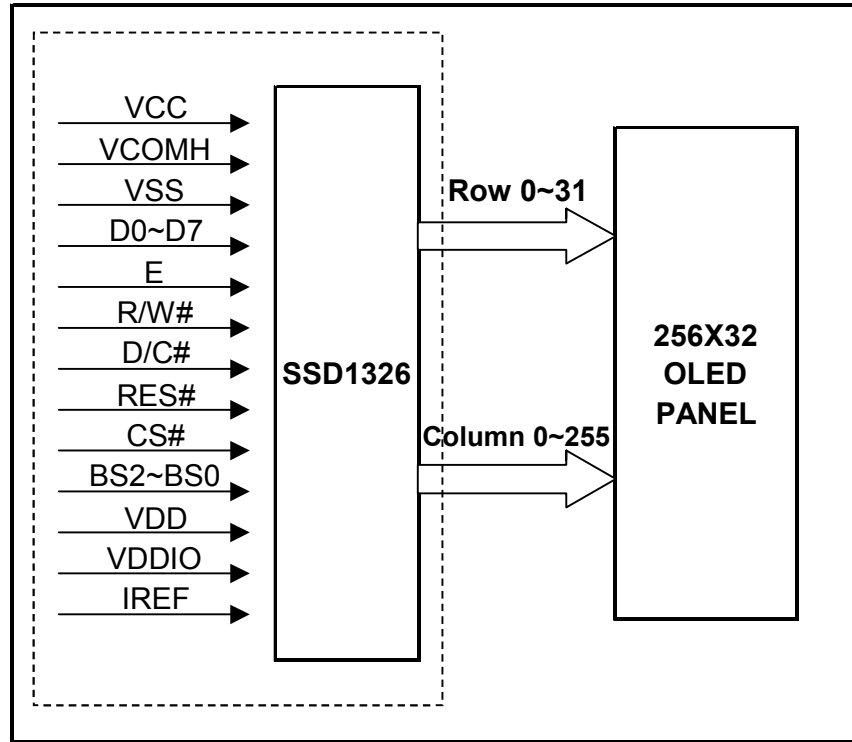
(2) Standby mode condition :

- Driving Voltage : 12V
- Contrast setting : 0x02
- Frame rate : 105Hz
- Duty setting : 1/32



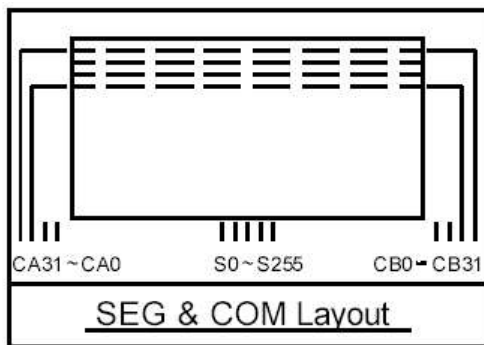
**7. INTERFACE**

**7.1 FUNCTION BLOCK DIAGRAM**



**RiTdisplay 256x32**

**7.2 PANEL LAYOUT DIAGRAM**



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### 7.3 PIN ASSIGNMENTS

PIN NAME	PIN NO.	TYPE	DESCRIPTION
NC	1		No connection
VCC	2	P	Positive OLED high voltage power supply
VCOMH	3	O	A capacitor should be connected between this pin and VSS.
VSS	4	P	This is a ground pin.
D7	5	I/O	This pin is bi-direction data signal.
D6	6	I/O	This pin is bi-direction data signal.
D5	7	I/O	This pin is bi-direction data signal.
D4	8	I/O	This pin is bi-direction data signal.
D3	9	I/O	This pin is bi-direction data signal.
D2	10	I/O	This pin is bi-direction data signal.
D1	11	I/O	This pin is bi-direction data signal.
D0	12	I/O	This pin is bi-direction data signal.
E	13	I	Data read operation is initiated when it's pull low.
R/W#	14	I	Data write operation is initiated when it's pull low.
D/C#	15	I	Data/ Command control. Pull high for write/read display data. Pull low for write command or read status.
RES#	16	I	Reset signal input. When it's low, initialization of SSD1326 is executed.
CS#	17	I	Chip selection input.
BS2	18	I	MPU bus interface selection pins.
BS1	19	I	
BS0	20	I	
VDDIO	21	I	Power supply pin of I/O buffer. It should be connected to VDD or external source.
VDD	22	P	Voltage power supply for logic
VSS	23	P	This is a ground pin.
IREF	24	I	A resistor should be connected between this pin and VSS.
VCC	25	P	Positive OLED high voltage power supply
NC	26		No connection

#### 7.4 GRAPHIC DISPLAY DATA RAM ADDRESS MAP

The GDDRAM is a bit mapped static RAM holding the bit pattern to be displayed.

The size of the RAM is 256 x 32 bits.

For mechanical flexibility, re-mapping on both Segment and Common outputs can be selected by software.

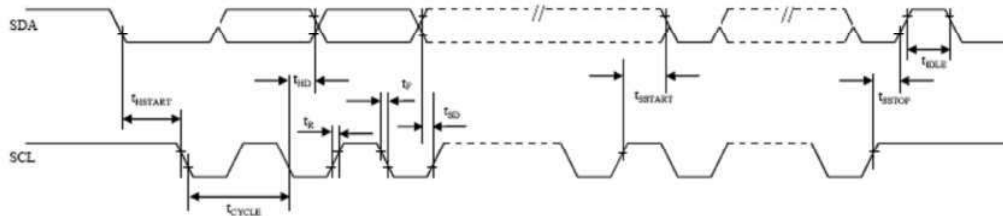
Display Data RAM Map

Column	0~7								8~15								.....	248~255									
ROW	D7	D6	D5	D4	D3	D2	D1	D0	D7	D6	D5	D4	D3	D2	D1	D0		D7	D6	D5	D4	D3	D2	D1	D0		
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## 7.5 INTERFACE TIMING CHART

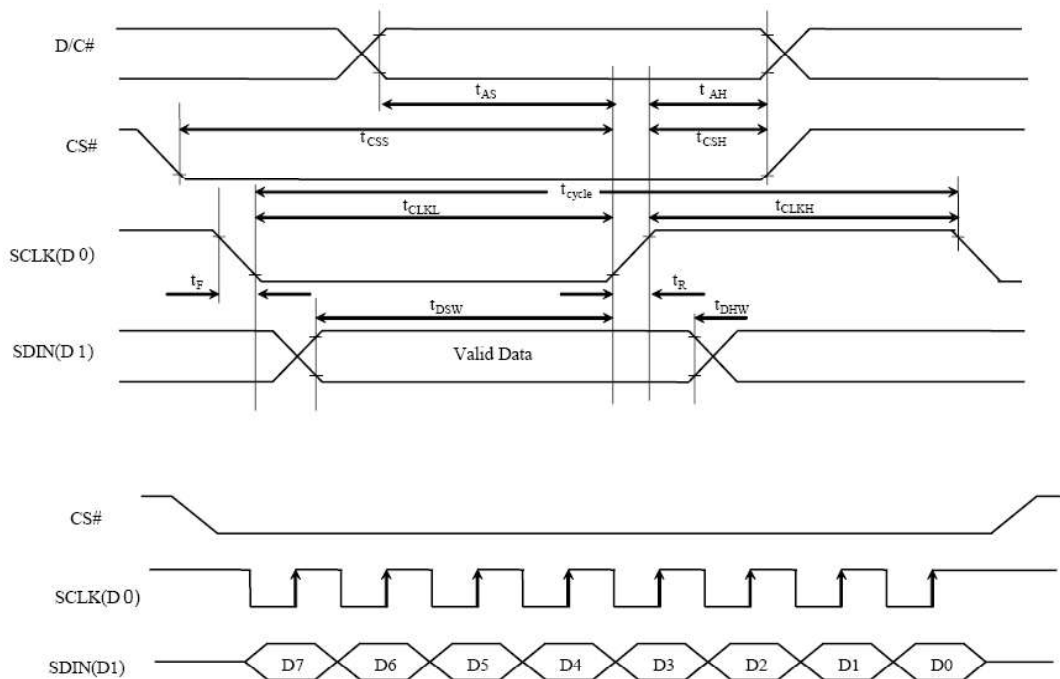
Symbol	Parameter	Min	Typ	Max	Unit
$t_{\text{cycle}}$	Clock Cycle Time	2.5	-	-	$\mu\text{s}$
$t_{\text{HSTART}}$	Start condition Hold Time	0.6	-	-	$\mu\text{s}$
$t_{\text{HD}}$	Data Hold Time	300	-	-	ns
$t_{\text{SD}}$	Data Setup Time	100	-	-	ns
$t_{\text{SSTART}}$	Start condition Setup Time (Only relevant for a repeated Start condition)	0.6	-	-	$\mu\text{s}$
$t_{\text{SSTOP}}$	Stop condition Setup Time	0.6	-	-	$\mu\text{s}$
$t_{\text{R}}$	Rise Time for data and clock pin	-	-	300	ns
$t_{\text{F}}$	Fall Time for data and clock pin	-	-	300	ns
$t_{\text{IDLE}}$	Idle Time before a new transmission can start	1.3	-	-	$\mu\text{s}$

I<sup>2</sup>C interface characteristics



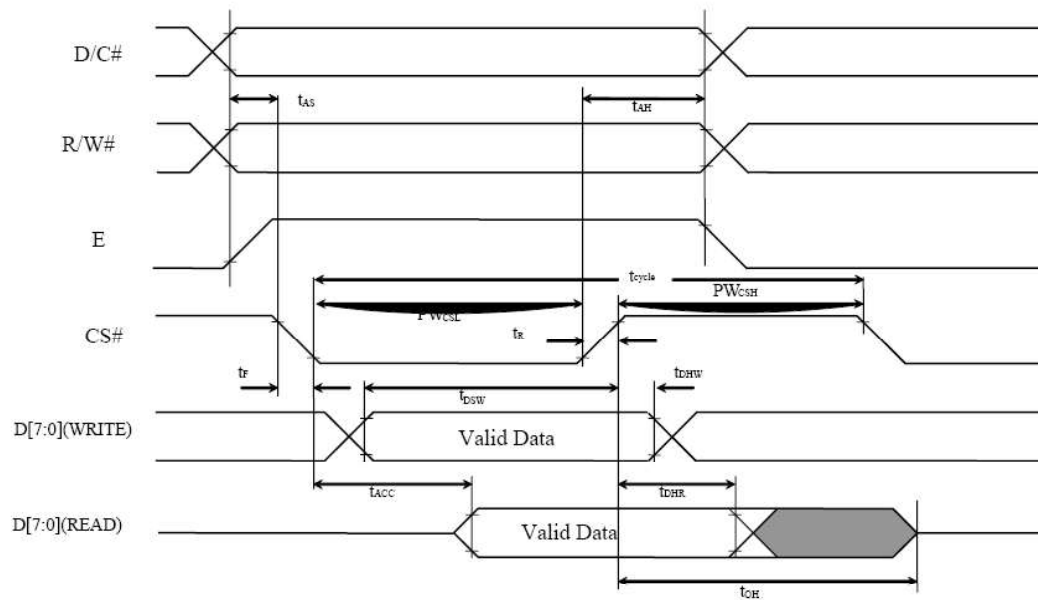
Symbol	Parameter	Min	Typ	Max	Unit
$t_{\text{cycle}}$	Clock Cycle Time	250	-	-	ns
$t_{\text{AS}}$	Address Setup Time	150	-	-	ns
$t_{\text{AH}}$	Address Hold Time	150	-	-	ns
$t_{\text{CSS}}$	Chip Select Setup Time	120	-	-	ns
$t_{\text{CSH}}$	Chip Select Hold Time	60	-	-	ns
$t_{\text{DSW}}$	Write Data Setup Time	100	-	-	ns
$t_{\text{DHW}}$	Write Data Hold Time	100	-	-	ns
$t_{\text{CLKL}}$	Clock Low Time	100	-	-	ns
$t_{\text{CLKH}}$	Clock High Time	100	-	-	ns
$t_{\text{R}}$	Rise Time	-	-	15	ns
$t_{\text{F}}$	Fall Time	-	-	15	ns

Serial interface characteristics



Symbol	Parameter	Min	Typ	Max	Unit
$t_{\text{cycle}}$	Clock Cycle Time	300	-	-	ns
$t_{\text{AS}}$	Address Setup Time	0	-	-	ns
$t_{\text{AH}}$	Address Hold Time	0	-	-	ns
$t_{\text{DSW}}$	Write Data Setup Time	40	-	-	ns
$t_{\text{DHW}}$	Write Data Hold Time	7	-	-	ns
$t_{\text{DHR}}$	Read Data Hold Time	20	-	-	ns
$t_{\text{OH}}$	Output Disable Time	-	-	70	ns
$t_{\text{ACC}}$	Access Time	-	-	140	ns
$PW_{\text{CSL}}$	Chip Select Low Pulse Width (read)	120	-	-	ns
	Chip Select Low Pulse Width (write)	60	-	-	ns
$PW_{\text{CSH}}$	Chip Select High Pulse Width (read)	60	-	-	ns
	Chip Select High Pulse Width (write)	60	-	-	ns
$t_{\text{R}}$	Rise Time	-	-	15	ns
$t_{\text{F}}$	Fall Time	-	-	15	ns

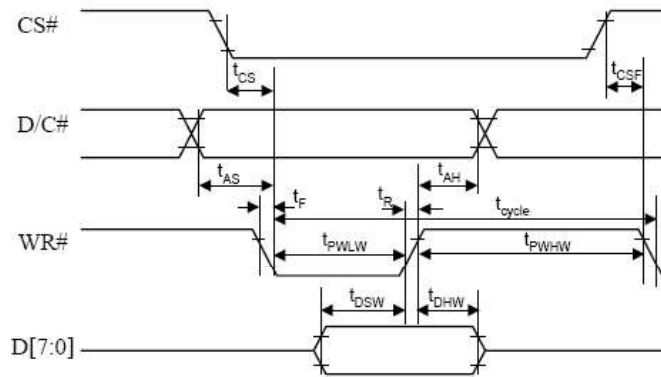
6800-series MCU parallel interface characteristics



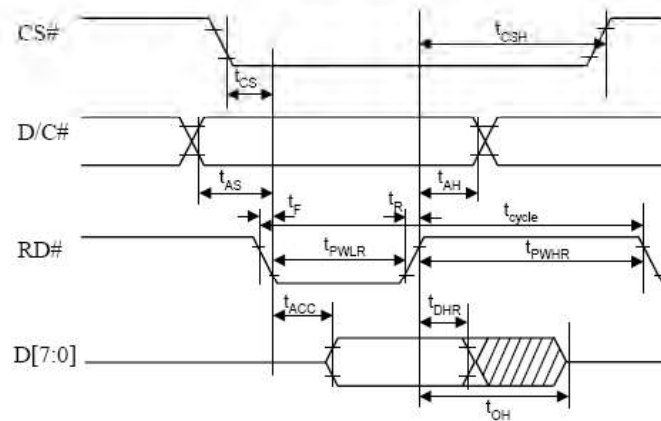
Symbol	Parameter	Min	Typ	Max	Unit
$t_{cclk}$	Clock Cycle Time	300	-	-	ns
$t_{AS}$	Address Setup Time	10	-	-	ns
$t_{AH}$	Address Hold Time	0	-	-	ns
$t_{DSW}$	Write Data Setup Time	40	-	-	ns
$t_{DHW}$	Write Data Hold Time	7	-	-	ns
$t_{DHR}$	Read Data Hold Time	20	-	-	ns
$t_{OH}$	Output Disable Time	-	-	70	ns
$t_{ACC}$	Access Time	-	-	140	ns
$t_{PWLr}$	Read Low Time	120	-	-	ns
$t_{PWLW}$	Write Low Time	60	-	-	ns
$t_{PWHr}$	Read High Time	60	-	-	ns
$t_{PWHW}$	Write High Time	60	-	-	ns
$t_r$	Rise Time	-	-	15	ns
$t_f$	Fall Time	-	-	15	ns
$t_{CS}$	Chip select setup time	0	-	-	ns
$t_{CSH}$	Chip select hold time to read signal	0	-	-	ns
$t_{CSF}$	Chip select hold time	20	-	-	ns

8080-series MCU parallel interface characteristics

Write cycle



Read cycle



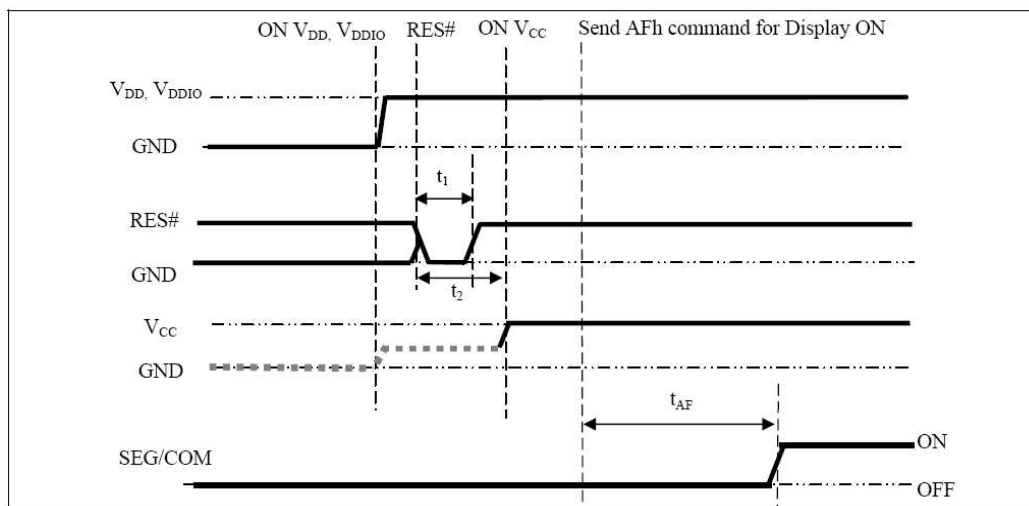
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## 8. POWER ON / OFF SEQUENCE & APPLICATION CIRCUIT

### 8.1 POWER ON / OFF SEQUENCE

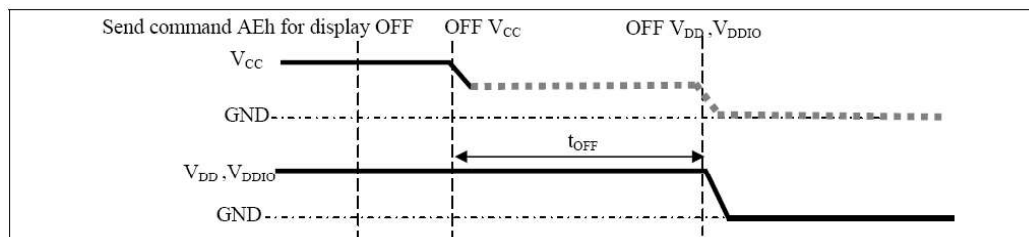
#### Power ON sequence:

1. Power ON  $V_{DD}$ ,  $V_{DDIO}$ .
2. After  $V_{DD}$ ,  $V_{DDIO}$  become stable, set RES# pin LOW (logic low) for at least  $2\mu s(t_1)$  and then HIGH (logic HIGH).
3. After set RES# pin LOW (logic LOW ), wait for at least  $2\mu s(t_2)$ . Then Power ON  $V_{CC}$ .(1)
4. After  $V_{CC}$  become stable, send command AFh for display ON. SEG/COM will be ON after  $100ms(t_{AF})$ .



#### Power OFF sequence:

1. Send command AEh for display OFF.
2. Power OFF  $V_{CC}$ . (1), (2)
3. Wait for  $t_{OFF}$ . Power OFF  $V_{DD}$ ,  $V_{DDIO}$ . (where Minimum  $t_{OFF}=80ms$ , Typical  $t_{OFF}=100ms$  )

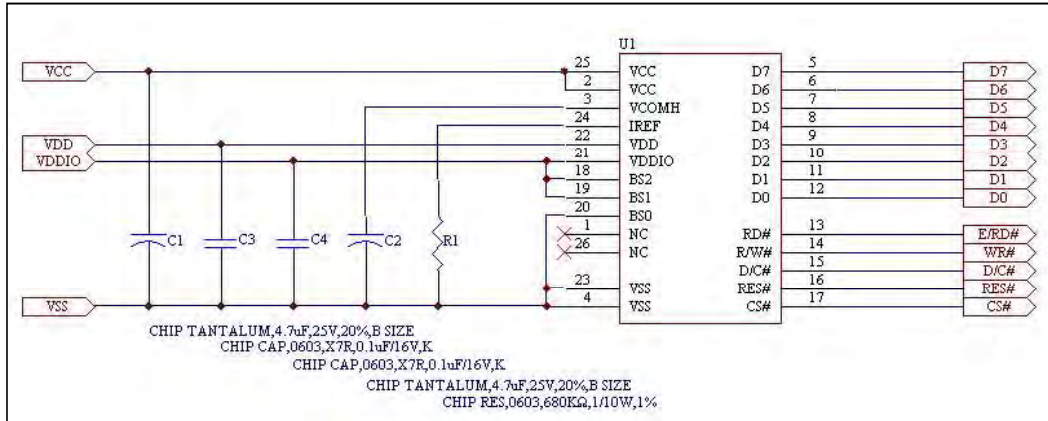


#### Note:

- (1) Since an ESD protection circuit is connected between  $V_{DD}$ ,  $V_{DDIO}$  and  $V_{CC}$ ,  $V_{CC}$  becomes lower than  $V_{DD}$ ,  $V_{DDIO}$  whenever  $V_{DD}$ ,  $V_{DDIO}$  is ON and  $V_{CC}$  is OFF as shown in the dotted line of  $V_{CC}$  in above figures.
- (2)  $V_{CC}$  should be disabled when it is OFF.



**8.2 APPLICATION CIRCUIT**



**8.3 COMMAND TABLE**

Refer to SSD1326 IC Spec.

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## 9. RELIABILITY TEST CONDITIONS

No.	Items	Specification	Quantity
1	High temp. (Non-operation)	85°C, 240hrs	5
2	High temp. (Operation)	70°C, 120hrs	5
3	Low temp. (Operation)	-40°C, 120hrs	5
4	High temp. / High humidity (Operation)	65°C, 90%RH, 120hrs	5
5	Thermal shock (Non-operation)	-40°C ~85°C (-40°C /30min; transit /3min; 85°C /30min; transit /3min) 1cycle: 66min, 100 cycles	5
6	Vibration	Frequency : 5~50HZ, 0.5G Scan rate : 1 oct/min Time : 2 hrs/axis Test axis : X, Y, Z	1 Carton
7	Drop	Height: 120cm Sequence : 1 angle 、 3 edges and 6 faces Cycles: 1	1 Carton
8	ESD (Non-operation)	Air discharge model, ±8kV, 10 times	5

### Test and measurement conditions

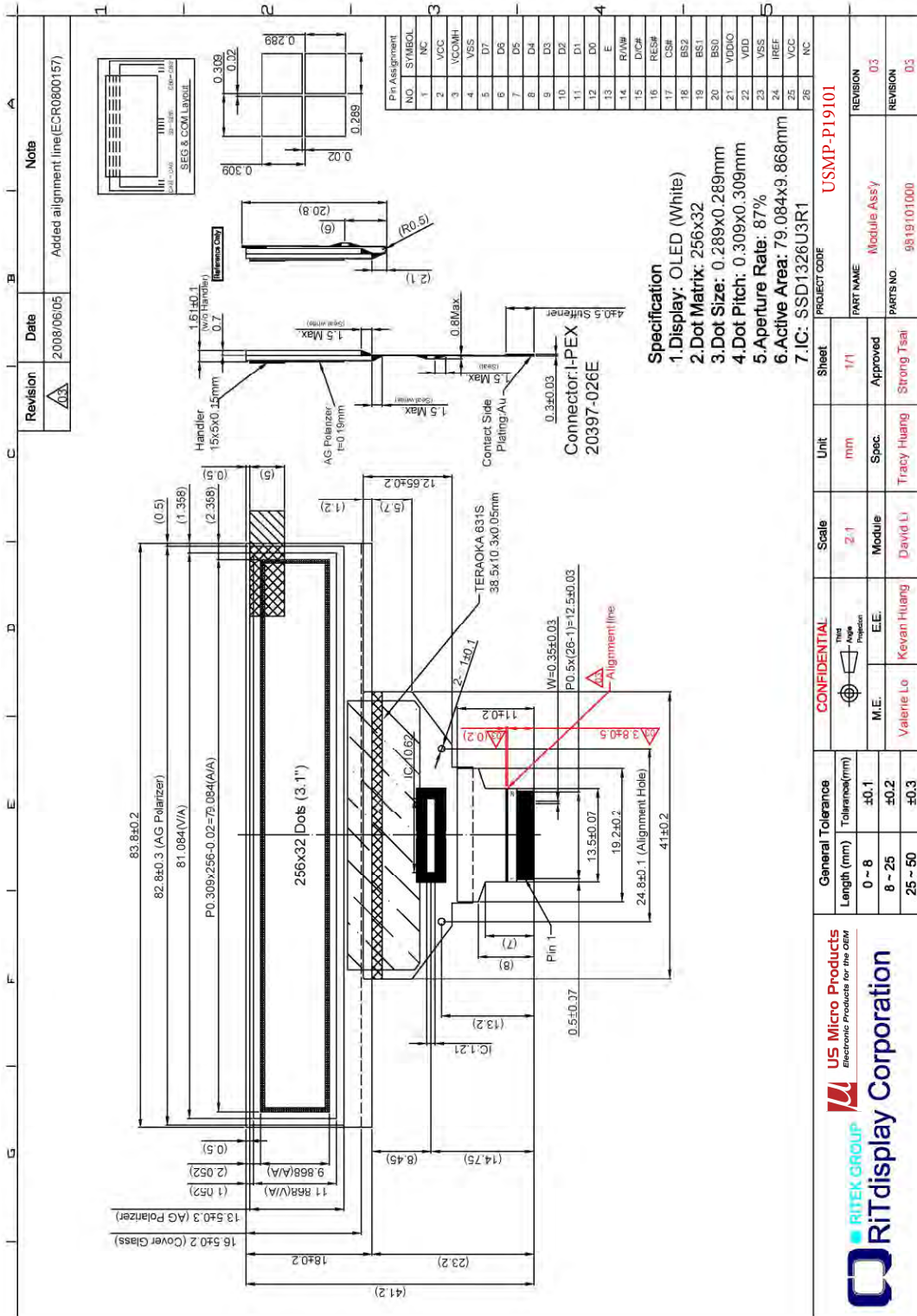
- All measurements shall not be started until the specimens attain to temperature stability.
- All-pixels-on is used as operation test pattern.
- The degradation of Polarizer are ignored for item 1, 4 & 5.

### Evaluation criteria

- The function test is OK.
- No observable defects.
- Luminance: > 50% of initial value.
- Current consumption: within  $\pm$  50% of initial value.

**10. EXTERNAL DIMENSION**

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- Specification**
1. Display: OLED (White)
  2. Dot Matrix: 256x32
  3. Dot Size: 0.289x0.289mm
  4. Dot Pitch: 0.309x0.309mm
  5. Aperture Rate: 87%
  6. Active Area: 79.084x9.868mm
  7. IC: SSD1326U3R1

Revision	Date	Note
A3	2008/06/05	Added alignment line(ECR0800157)

Sheet	1/1	PROJECT CODE	USMP-P19101
Unit	mm	PART NAME	Module Assy
Scale	2:1	Spec.	Tracy Huang
Module	David Lu	Approved	Strong Tsai
M.E.	Valerie Lo	Parts No.	9819101000
M.E. Projection	Keven Huang	REVISION	03
M.E.	Valerie Lo	REVISION	03

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**11. PACKING SPECIFICATION**

Revision	Date	Note
▲▲	2008/04/14	Packing Tray Instruction

**1** P19101 Module P/N:9819101000 旋轉放置

**2** Packing Tray P/N:3008000114 330x270x8.7mm, t=0.7mm

**3** 5G 乾燥膜 P/N:3010000002 x4

**4** 真空包裝袋 ONLY/DPE P/N:3003000012 480x285x90mm 抽真空6秒, 壓力170

**5** Antistatic Bubble Bag P/N:3003000016 440x(350+450)mm

**6** Pizza Box P/N:3001000005 345x285x88, B袋

**7** 單色 Carton P/N:3006000009 385x305x203mm

**8** Label P/N:3006000000

**9** 封箱膠帶, W=48mm, L=910cm

**Quantity:** x 21 pcs 以膠帶固定, x 20 pcs 旋轉堆疊, x 1 pcs (empty)

Item	Part No.	Description	QTY
1	9819101000	P19101 Module Assy	720
2	3008000114	Tray 330x270x8.7mm, PS, t=0.7mm	42
3	3000000002	5G 乾燥膜	8
4	3009000012	真空包裝袋 480x285x90mm	2
5	3003000016	Antistatic Bubble Bag 440x(350+450)mm	2
6	3001000005	Pizza Box 345x285x88, B袋	2
7	3006000009	單色 Carton, 385x305x203mm	1
8	3006000000	Label	3
9	3208000125	封箱膠帶, W=48mm, L=910cm	

CONFIDENTIAL		PROJECT CODE	USMP-P19101
General Tolerance	Scale	Unit	Sheet
Length (mm)	1:3.5	mm	1/1
0 ~ 8	Module	Spec.	Approved
8 ~ 25	Valerie Lo	Tracy Huang	Strong Tsai
25 ~ 50	Iven Lee	Kevan Huang	Packing Tray Instruction
		PARTS NO.	9819101000
		REVISION	01

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## 12. APPENDIXES

### APPENDIX 1: DEFINITIONS

#### A. DEFINITION OF CHROMATICITY COORDINATE

The chromaticity coordinate is defined as the coordinate value on the CIE 1931 color chart for R, G, B, W.

#### B. DEFINITION OF CONTRAST RATIO

The contrast ratio is defined as the following formula:

$$\text{Contrast Ratio} = \frac{\text{Luminance of all pixels on measurement}}{\text{Luminance of all pixels off measurement}}$$

#### C. DEFINITION OF RESPONSE TIME

The definition of turn-on response time  $T_r$  is the time interval between a pixel reaching 10% of steady state luminance and 90% of steady state luminance. The definition of turn-off response time  $T_f$  is the time interval between a pixel reaching 90% of steady state luminance and 10% of steady state luminance. It is shown in Figure 2.

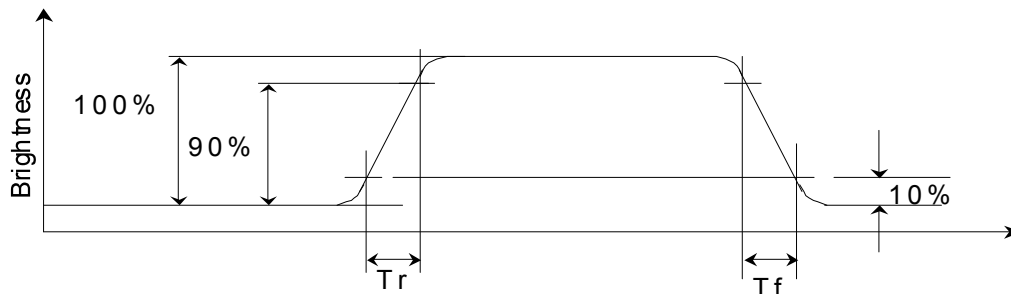


Figure 2: Response time

#### D. DEFINITION OF VIEWING ANGLE

The viewing angle is defined as Figure 3. Horizontal and vertical (H & V) angles are determined for viewing directions where luminance varies by 50% of the perpendicular value.

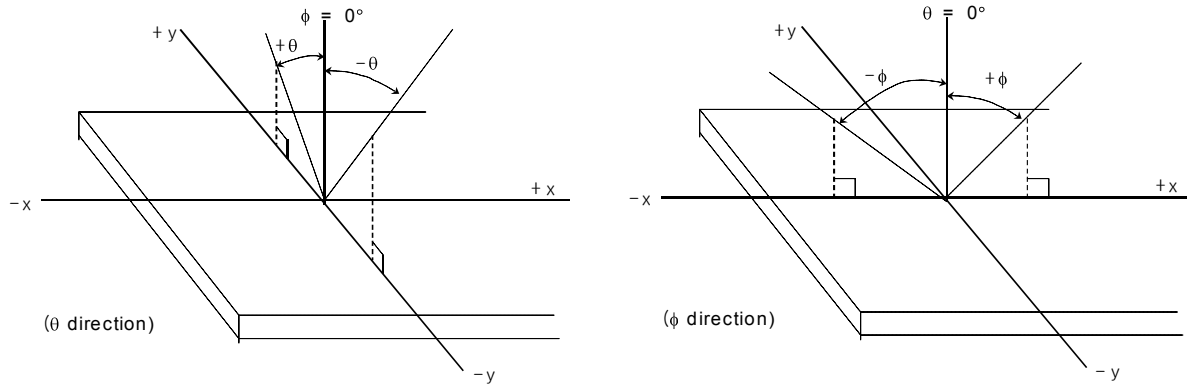
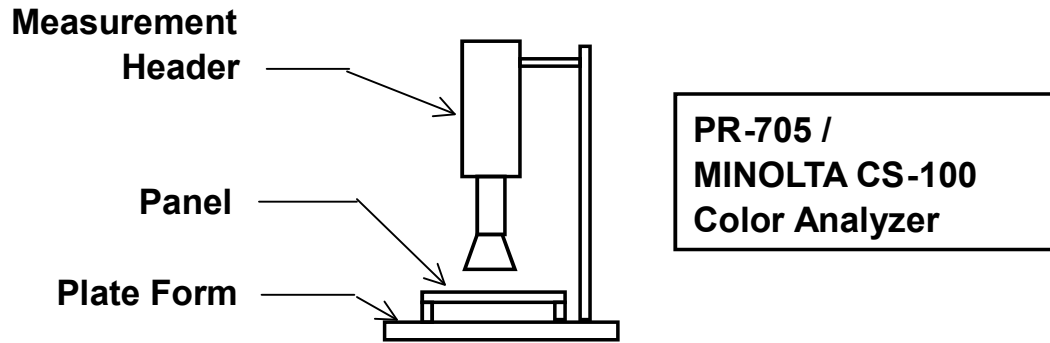


Figure 3: Viewing Angle

## APPENDIX 2: MEASUREMENT APPARATUS

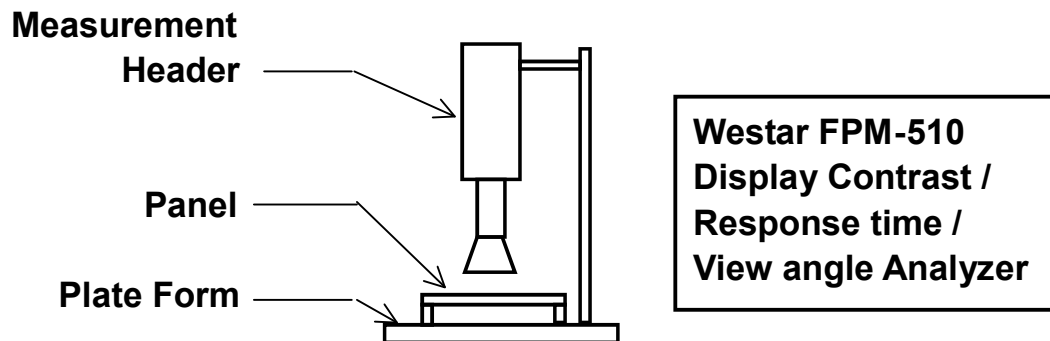
### A. LUMINANCE/COLOR COORDINATE

PHOTO RESEARCH PR-705, MINOLTA CS-100

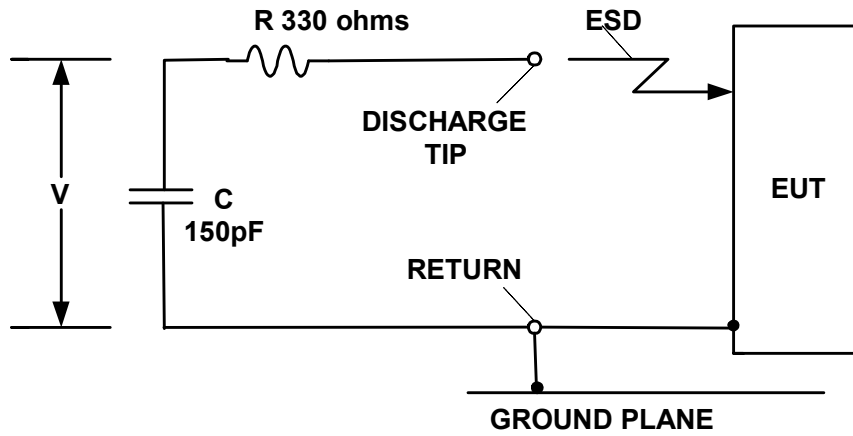


### B. CONTRAST / RESPONSE TIME / VIEW ANGLE

WESTAR CORPORATION FPM-510



### C. ESD ON AIR DISCHARGE MODE



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**APPENDIX 3: PRECAUTIONS****A. RESIDUE IMAGE**

Because the pixels are lighted in different time, the luminance of active pixels may reduce or differ from inactive pixels. Therefore, the residue image will occur. To avoid the residue image, every pixel needs to be lighted up uniformly.

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