



US Micro Products
Electronic Products for the OEM

OLED PRODUCT SPECIFICATION

Manufactured by:



PART NUMBER:	USMP-P14203
DESCRIPTION:	1.3" OLED, Blue, 128x96 Resolution, COF, SSD1329

ISSUE DATE	APPROVED BY (Customer Use Only)	CHECKED BY	PREPARED BY
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REVISION RECORD

REV.	REVISION DESCRIPTION	REV. DATE	REMARK
X01	INITIAL RELEASE	2006. 07. 04	
A01	<ul style="list-style-type: none"> ■ Modify product name (RGC13128096BH000→ RGS13128096BH000) ■ Add panel electrical specifications of standby mode ■ Add packing specification 	2006. 09. 26	Page 1, 8 & 20
A02	<ul style="list-style-type: none"> ■ Modify specification of dark room contrast ■ Modify power on/off sequence ■ Modify packing specification 	2007. 11. 13	Page 4, 8, 16 & 20
A03	<ul style="list-style-type: none"> ■ Modify definition of panel thickness ■ Modify power off sequence ■ Modify packing specification 	2009. 04. 07	Page 5, 16 & 20
A04	<ul style="list-style-type: none"> ■ Modify panel thickness ■ Modify polarizer thickness ■ Modify IC dimension 	2009. 11. 26	Page 4, 5 & 19

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CONTENTS

ITEM	PAGE
<u>1. SCOPE</u>	4
<u>2. WARRANTY</u>	4
<u>3. FEATURES</u>	4
<u>4. MECHANICAL DATA</u>	5
<u>5. MAXIMUM RATINGS</u>	6
<u>6. ELECTRICAL CHARACTERISTICS</u>	7
6.1 D.C ELECTRICAL CHARACTERISTICS	
6.2 ELECTRO-OPTICAL CHARACTERISTICS	
<u>7. INTERFACE</u>	9
7.1 FUNCTION BLOCK DIAGRAM	
7.2 PANEL LAYOUT DIAGRAM	
7.3 PIN ASSIGNMENTS	
7.4 GRAPHIC DISPLAY DATA RAM ADDRESS MAP	
7.5 INTERFACE TIMING CHART	
<u>8. POWER ON / OFF SEQUENCE & APPLICATION CIRCUIT</u>	16
8.1 POWER ON / OFF SEQUENCE	
8.2 APPLICATION CIRCUIT	
8.3 COMMAND TABLE	
<u>9. RELIABILITY TEST CONDITIONS</u>	18
<u>10. EXTERNAL DIMENSION</u>	19
<u>11. PACKING SPECIFICATION</u>	20
<u>12. APPENDIXES</u>	21

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1. SCOPE

The purpose of this specification is to define the general provisions and quality requirements that apply to the supply of display cells manufactured by RiTdisplay. This document, together with the Module Ass'y Drawing, is the highest-level specification for this product. It describes the product, identifies supporting documents and contains specifications.

2. WARRANTY

RiTdisplay warrants that the products delivered pursuant to this specification (or order) will conform to the agreed specifications for twelve (12) months from the shipping date ("Warranty Period"). RiTdisplay is obligated to repair or replace the products which are found to be defective or inconsistent with the specifications during the Warranty Period without charge, on condition that the products are stored or used as the conditions specified in the specifications. Nevertheless, RiTdisplay is not obligated to repair or replace the products without charge if the defects or inconsistency are caused by the force majeure or the reckless behaviors of the customer.

After the Warranty Period, all repairs or replacements of the products are subject to charge.

3. FEATURES

- Small molecular organic light emitting diode.
- Color : Blue
- Panel matrix : 128*96
- Driver IC : SSD1329U2
- Excellent Quick response time : 10 μ s
- Extremely thin thickness for best mechanism design : 1.61mm.
- High contrast : 2000:1
- Wide viewing angle : 160°
- 8-bit 6800-series Parallel Interface, 8-bit 8080-series Parallel Interface, Serial Peripheral Interface.
- Wide range operating temperature : -40 to 70 °C
- Anti-glare polarizer.

4. MECHANICAL DATA

NO	ITEM	SPECIFICATION	UNIT
1	Dot Matrix	128 (W) x 96 (H)	dot
2	Dot Size	0.19 (W) x 0.19 (H)	mm ²
3	Dot Pitch	0.21 (W) x 0.21 (H)	mm ²
4	Aperture Rate	82	%
5	Active Area	26.86 (W) x 20.14 (H)	mm ²
6	Panel Size	33 (W) x 26.8 (H)	mm ²
7*	Panel Thickness	1.42 ± 0.1	mm
8	Module Size	33 (W) x 41.6 (H) x 1.61 (T)	mm ³
9	Diagonal A/A size	1.3	inch
10	Module Weight	2.88 ± 10%	gram

* Panel thickness includes substrate glass, cover glass and UV glue thickness.

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5. MAXIMUM RATINGS

ITEM	MIN	MAX	UNIT	Condition	Remark
Supply Voltage (V_{DD})	-0.3	3.5	V	$T_a = 25^\circ\text{C}$	IC maximum rating
Supply Voltage (V_{CC})	8	16	V	$T_a = 25^\circ\text{C}$	IC maximum rating
Operating Temp.	-40	70	$^\circ\text{C}$		
Storage Temp	-40	85	$^\circ\text{C}$		
Humidity		85	%		
Life Time	5,200	-	Hrs	100 cd/m^2 , 50% checkerboard	Note (1)
Life Time	6,500	-	Hrs	80 cd/m^2 , 50% checkerboard	Note (2)
Life Time	8,600	-	Hrs	60 cd/m^2 , 50% checkerboard	Note (3)

Note:

(A) Under $V_{CC} = 15\text{V}$, $T_a = 25^\circ\text{C}$, 50% RH.

(B) Life time is defined the amount of time when the luminance has decayed to less than 50% of the initial measured luminance.

(1) Setting of 100 cd/m^2 :

- Contrast setting : 0xB4
- Frame rate : 85Hz
- Duty setting : 1/96

(2) Setting of 80 cd/m^2 :

- Contrast setting : 0x7F
- Frame rate : 85Hz
- Duty setting : 1/96

(3) Setting of 60 cd/m^2 :

- Contrast setting : 0x4A
- Frame rate : 85Hz
- Duty setting : 1/96

6. ELECTRICAL CHARACTERISTICS

6.1 D.C ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETERS	TEST CONDITION	MIN	TYP	MAX	UNIT
V _{CC}	Driver power supply (for OLED panel)	Ta=-20°C to +70°C	14.5	15	15.5	V
V _{DD}	Logic operating voltage	Ta=-20°C to +70°C	2.4	2.7	3.5	V
V _{OH}	Hi logic output level	I _{out} =100 uA, 3.3MHz	0.9* V _{DD}	-	V _{DD}	V
V _{OL}	Low logic output level	I _{out} =100uA, 3.3MHZ	0	-	0.1* V _{DD}	V
V _{IH}	Hi logic input level	I _{out} =100uA, 3.3MHZ	0.8* V _{DD}	-	V _{DD}	V
V _{IL}	Low logic input level	I _{out} =100uA, 3.3MHZ	0	-	0.2* V _{DD}	V
I _{CC}	Operating current for V _{CC}	Contrast=7F	-	750	850	uA
I _{DD}	Operating current for V _{DD}	Contrast=7F	-	72	200	uA
I _{SEG}	Segment output current	Contrast=7F	250	300	370	uA
		Contrast=5F	-	225	-	uA
		Contrast=3F	-	150	-	uA
		Contrast=1F	50	75	100	uA

Note : V_{DD}=2.7 V ; V_{CC}= 15 V ; Frame rate= 85 Hz ; No panel attached.

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6.2 ELECTRO-OPTICAL CHARACTERISTICS

PANEL ELECTRICAL SPECIFICATIONS

PARAMETER	MIN	TYP.	MAX	UNITS	COMMENTS
Normal mode current	-	23	25	mA	All pixels on (1)
Standby mode current	-	2	4	mA	Standby mode 10% pixels on (2)
Normal mode power consumption	-	345	375	mW	All pixels on (1)
Standby mode power consumption	-	30	60	mW	Standby mode 10% pixels on (2)
Normal mode Luminance	60	80		cd/m ²	Display Average
Standby mode Luminance		30		cd/m ²	Display Average
CIE _x (Blue)	0.10	0.14	0.18		x, y (CIE 1931)
CIE _y (Blue)	0.20	0.24	0.28		
Dark Room Contrast	2000:1				
Viewing Angle	160			degree	
Response Time		10		μs	

(1) Normal mode condition :

- Driving Voltage : 15V
- Contrast setting : 0x7F
- Frame rate : 85Hz
- Duty setting : 1/96

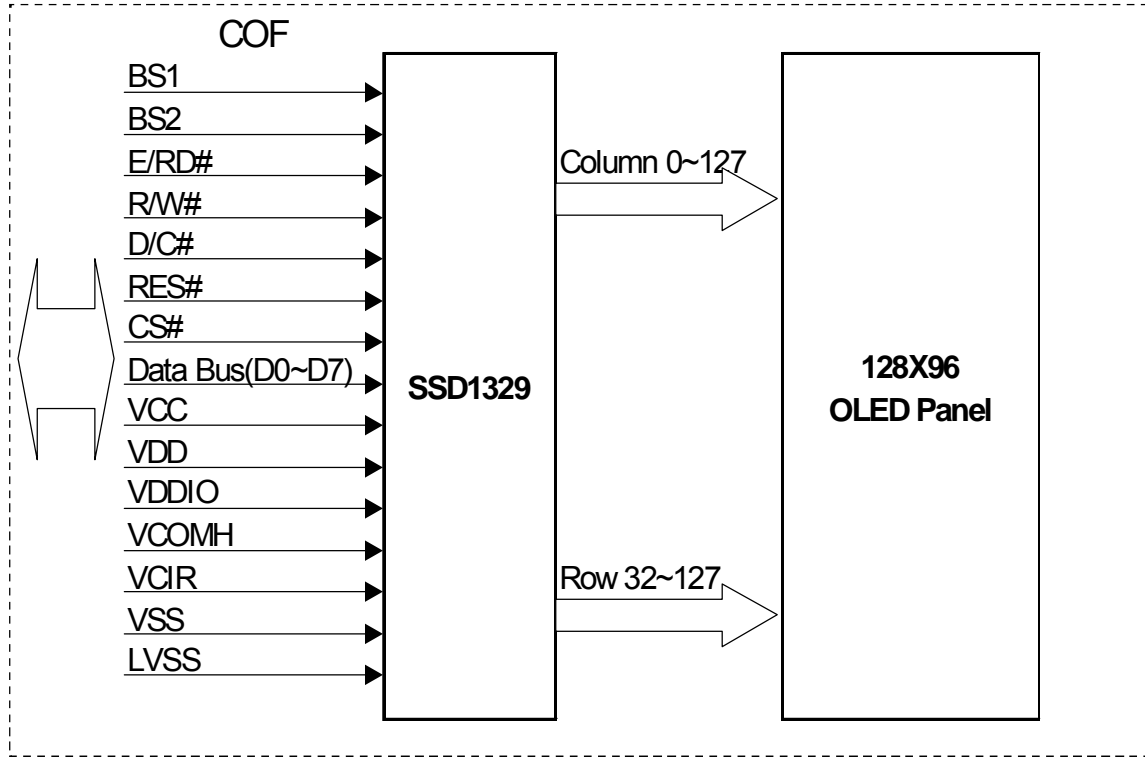
(2) Standby mode condition :

- Driving Voltage : 15V
- Contrast setting : 0x00
- Frame rate : 85Hz
- Duty setting : 1/96

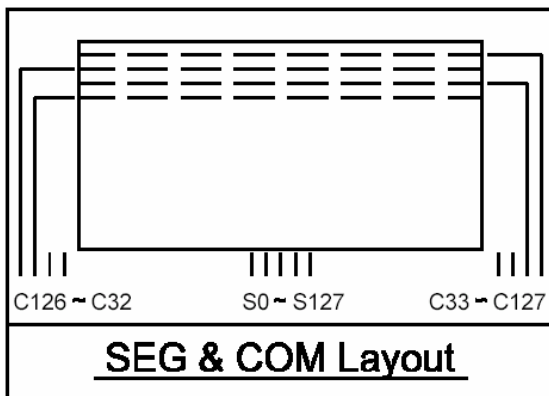
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7. INTERFACE

7.1 FUNCTION BLOCK DIAGRAM



7.2 PANEL LAYOUT DIAGRAM



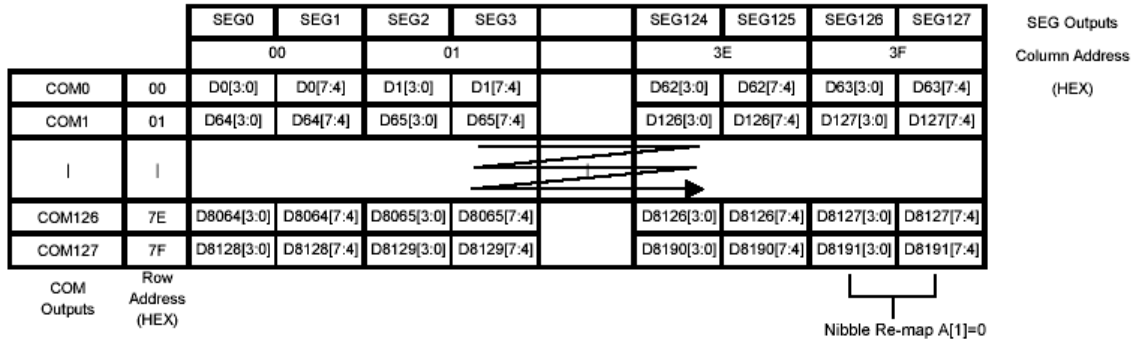
7.3 PIN ASSIGNMENTS

PIN NAME	PIN NO	DESCRIPTION												
NC	1	No connection.												
VCIR	2	No connection and left float.												
VCOMH	3	Com Voltage Output. A capacitor should be connected between this pin and V_{SS} .												
LVSS	4	Ground.												
VSS	5	Ground.												
BS1	6	MCU parallel interface selection input.												
		<table border="1"> <thead> <tr> <th></th> <th>6800-parallel interface</th> <th>8080-parallel interface</th> <th>Serial interface</th> </tr> </thead> <tbody> <tr> <td>BS1</td> <td>0</td> <td>1</td> <td>0</td> </tr> <tr> <td>BS2</td> <td>1</td> <td>1</td> <td>0</td> </tr> </tbody> </table>		6800-parallel interface	8080-parallel interface	Serial interface	BS1	0	1	0	BS2	1	1	0
	6800-parallel interface	8080-parallel interface	Serial interface											
BS1	0	1	0											
BS2	1	1	0											
BS2	7													
IREF	8	Reference current input pin. A resistor should be connected between this pin and V_{DD} .												
CS#	9	Chip select input.												
RES#	10	Reset signal input. When it's low, initialization of SSD1329 is executed.												
D/C#	11	Data/ Command control. Pull high for write/read display data. Pull low for write command or read status.												
RW#	12	MCU interface input. Data write operation is initiated when it's pull low.												
E	13	MCU interface input. Data read operation is initiated when it's pull low.												
D0	14	Data bus(for parallel interface)												
D1	15	Data bus(for parallel interface)												
D2	16	Data bus(for parallel interface)												
D3	17	Data bus(for parallel interface)												
D4	18	Data bus(for parallel interface)												
D5	19	Data bus(for parallel interface)												
D6	20	Data bus(for parallel interface)												
D7	21	Data bus(for parallel interface)												
VDDIO	22	This pin is a power supply pin of I/O buffer.												
VDD	23	Power supply for logic.												
VCC	24	Power supply for analog circuit.												
NC	25	No connection.												

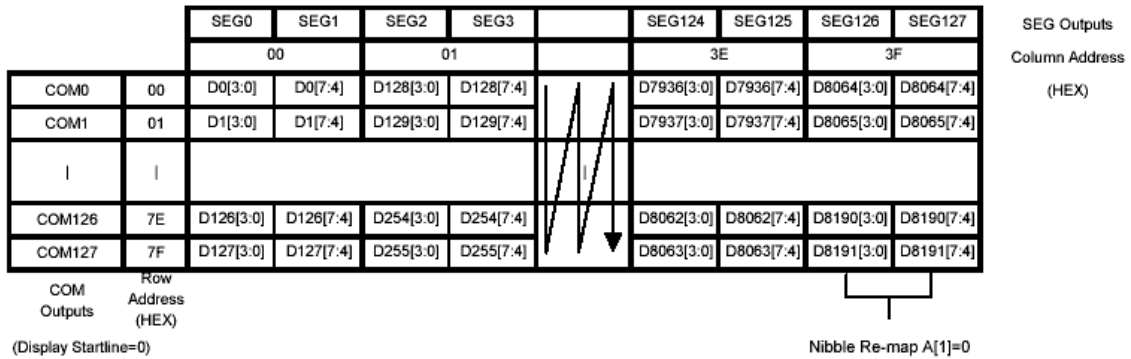
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7.4 GRAPHIC DISPLAY DATA RAM ADDRESS MAP

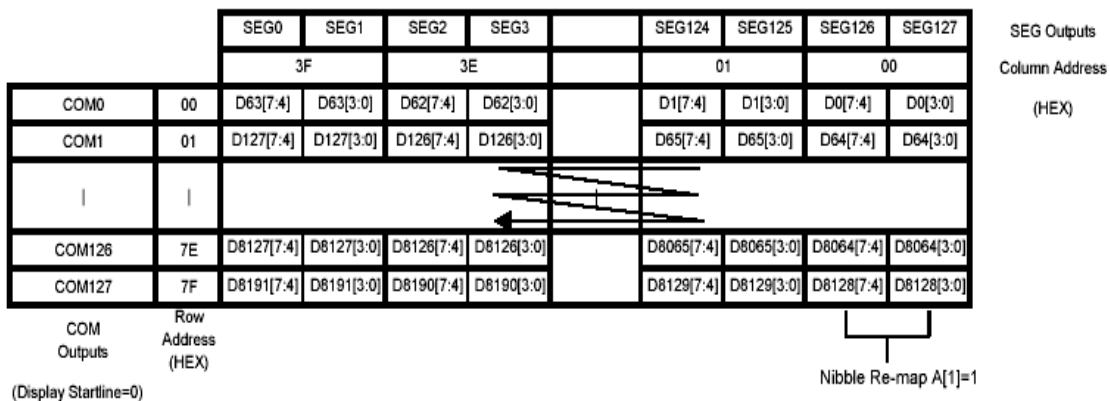
GDDRAM Address Map - Horizontal Address Increment $A[2]=0$, Column Address Re-map $A[0]=0$, Nibble Re-map $A[1]=0$, COM Re-map $A[4]=0$, Display Start Line=00H (Data byte sequence: D0, D1, D2 ... D8191)



GDDRAM Address Map - Vertical Address Increment $A[2]=1$, Column Address Re-map $A[0]=0$, Nibble Re-map $A[1]=0$, COM Re-map $A[4]=0$, Display Start Line=00H (Data byte sequence: D0, D1, D2 ... D8191)



GDDRAM Address Map - Horizontal Address Increment $A[2]=0$, Column Address Re-map $A[0]=1$, Nibble Re-map $A[1]=1$, COM Re-map $A[4]=0$, Display Start line=00H (Data byte sequence: D0, D1, D2 ... D8191)



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GDDRAM Address Map - Horizontal Address Increment A[2]=0, Column Address Re-map A[0]=0, Nibble Re-map A[1]=0, COM Re-map A[4]=1, Display Start Line=78H (Data byte sequence: D0, D1, D2 ... D8191)

		SEG0	SEG1	SEG2	SEG3		SEG124	SEG125	SEG126	SEG127	SEG Outputs Column Address (HEX)
		00		01			3E		3F		
COM119	00	D0[3:0]	D0[7:4]	D1[3:0]	D1[7:4]		D62[3:0]	D62[7:4]	D63[3:0]	D63[7:4]	
COM118	01	D1[3:0]	D64[7:4]	D65[3:0]	D65[7:4]		D126[3:0]	D126[7:4]	D127[3:0]	D127[7:4]	
COM121	7E	D126[3:0]	D8064[7:4]	D8065[3:0]	D8065[7:4]		D8126[3:0]	D8126[7:4]	D8127[3:0]	D8127[7:4]	
COM120	7F	D127[3:0]	D8128[7:4]	D8129[3:0]	D8129[7:4]		D8190[3:0]	D8190[7:4]	D8191[3:0]	D8191[7:4]	

COM Outputs Row Address (HEX)
 (Display Startline=78H)

GDDRAM Address Map - Horizontal Address Increment A[2]=0, Column Address Re-map A[0]=0, Nibble Re-map A[1]=0, COM Re-map A[4]=0, Display Start Line=00H (Data byte sequence: D0, D1, D2 ... D7811), Column Start Address = 01H, Column End Address = 3EH, Row Start Address = 01H, Row End Address = 7EH

		SEG0	SEG1	SEG2	SEG3		SEG124	SEG125	SEG126	SEG127	SEG Outputs Column Address (HEX)
		00		01			3E		3F		
COM0	00										
COM1	01			D0[3:0]	D0[7:4]		D61[3:0]	D61[7:4]			
COM126	7E			D7750[3:0]	D7750[7:4]		D7811[3:0]	D7811[7:4]			
COM127	7F										

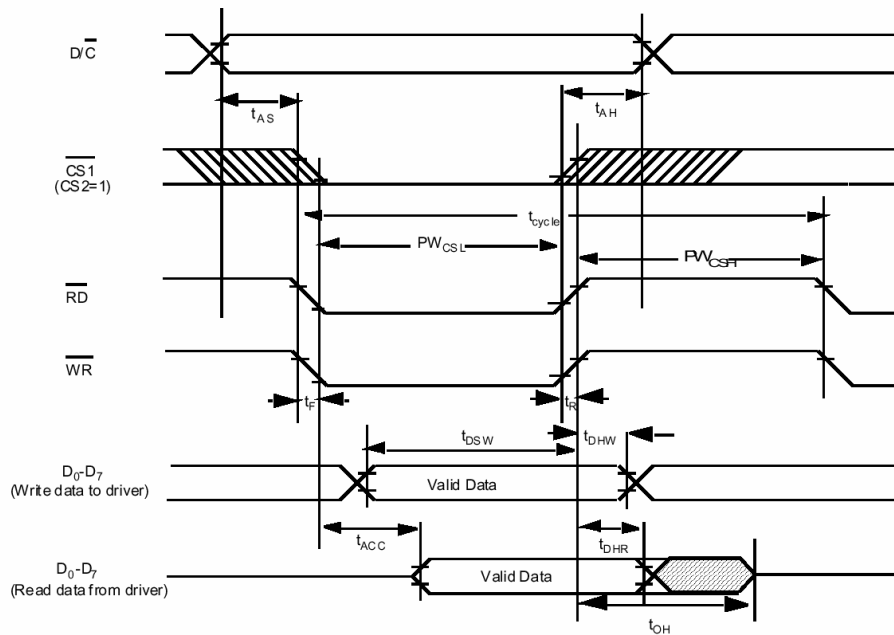
COM Outputs Row Address (HEX)
 (Display Startline=0)

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7.5 INTERFACE TIMING CHART

8080-Series MPU Parallel Interface Timing Characteristics ($V_{DD}-V_{SS} = 2.4$ to $3.5V$, $T_A = -30$ to $85^\circ C$)

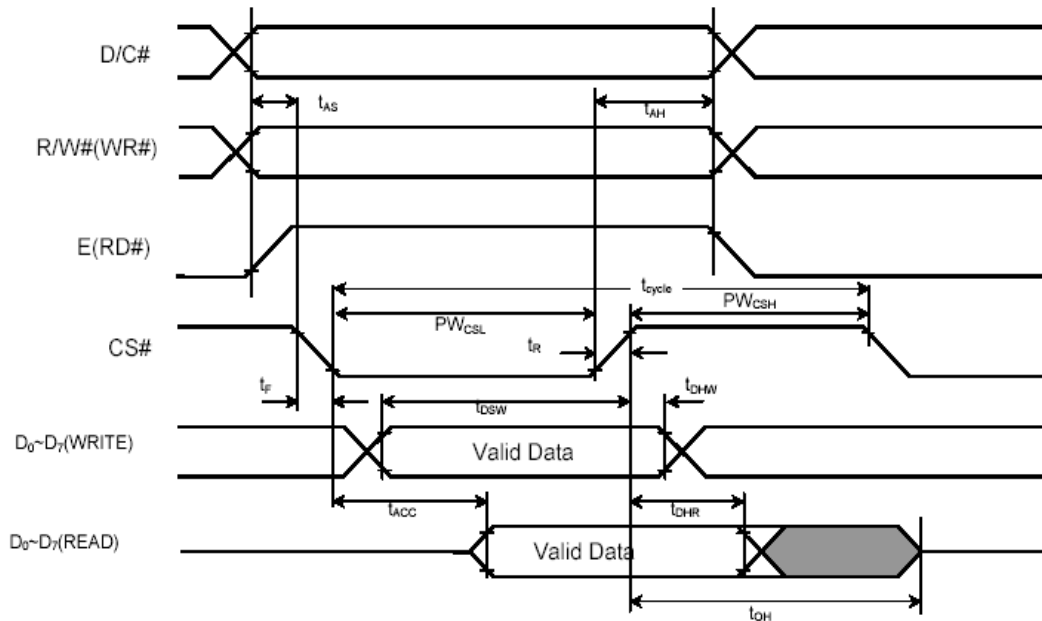
Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time	300	-	-	ns
t_{AS}	Address Setup Time	0	-	-	ns
t_{AH}	Address Hold Time	0	-	-	ns
t_{DSW}	Write Data Setup Time	40	-	-	ns
t_{DHW}	Write Data Hold Time	15	-	-	ns
t_{DHR}	Read Data Hold Time	20	-	-	ns
t_{OH}	Output Disable Time	-	-	70	ns
t_{ACC}	Access Time	-	-	140	ns
PW_{CSL}	Chip Select Low Pulse Width (read) Chip Select Low Pulse Width (write)	120 60	-	-	ns
PW_{CSH}	Chip Select High Pulse Width (read) Chip Select High Pulse Width (write)	60 60	-	-	ns
t_R	Rise Time	-	-	15	ns
t_F	Fall Time	-	-	15	ns



8080-series MPU Parallel Interface Characteristics

6800-Series MPU Parallel Interface Timing Characteristics (V_{DD} - V_{SS} = 2.4 to 3.5V, T_A = 25°C)

Symbol	Parameter	Min	Typ	Max	Unit
t _{cycle}	Clock Cycle Time	300	-	-	ns
t _{AS}	Address Setup Time	0	-	-	ns
t _{AH}	Address Hold Time	0	-	-	ns
t _{DSW}	Write Data Setup Time	40	-	-	ns
t _{DHW}	Write Data Hold Time	15	-	-	ns
t _{DHR}	Read Data Hold Time	20	-	-	ns
t _{OH}	Output Disable Time	-	-	70	ns
t _{ACC}	Access Time	-	-	140	ns
PW _{CSL}	Chip Select Low Pulse Width (read) Chip Select Low Pulse Width (write)	120 60	-	-	ns
PW _{CSH}	Chip Select High Pulse Width (read) Chip Select High Pulse Width (write)	60 60	-	-	ns
t _R	Rise Time	-	-	15	ns
t _F	Fall Time	-	-	15	ns

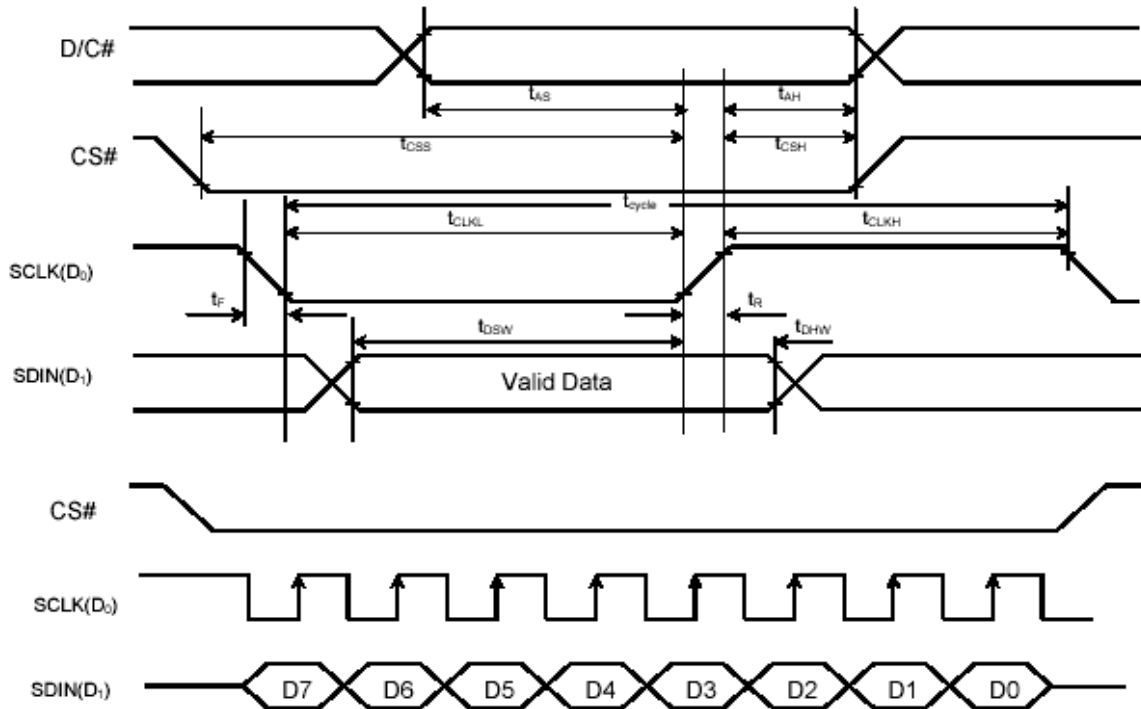


6800-series MPU Parallel Interface Characteristics

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Serial Interface Timing Characteristics ($V_{DD} - V_{SS} = 2.4$ to $3.5V$, $T_A = 25^\circ C$)

Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time	250	-	-	ns
t_{AS}	Address Setup Time	150	-	-	ns
t_{AH}	Address Hold Time	150	-	-	ns
t_{CSS}	Chip Select Setup Time	120	-	-	ns
t_{CSH}	Chip Select Hold Time	60	-	-	ns
t_{DSW}	Write Data Setup Time	100	-	-	ns
t_{DHW}	Write Data Hold Time	100	-	-	ns
t_{CLKL}	Clock Low Time	100	-	-	ns
t_{CLKH}	Clock High Time	100	-	-	ns
t_R	Rise Time	-	-	15	ns
t_F	Fall Time	-	-	15	ns



Serial Interface Characteristics

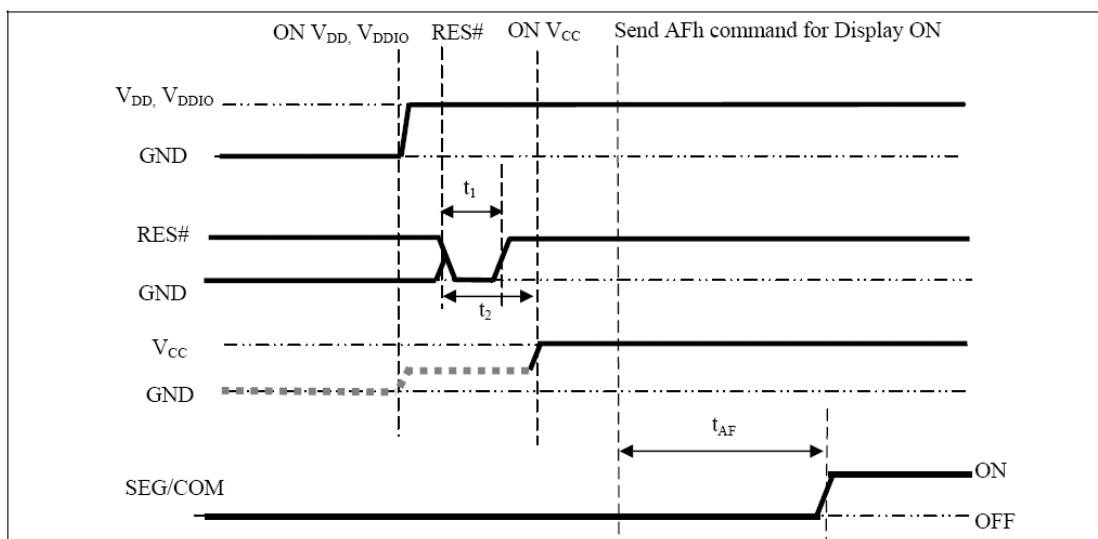
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8. POWER ON / OFF SEQUENCE & APPLICATION CIRCUIT

8.1 POWER ON / OFF SEQUENCE

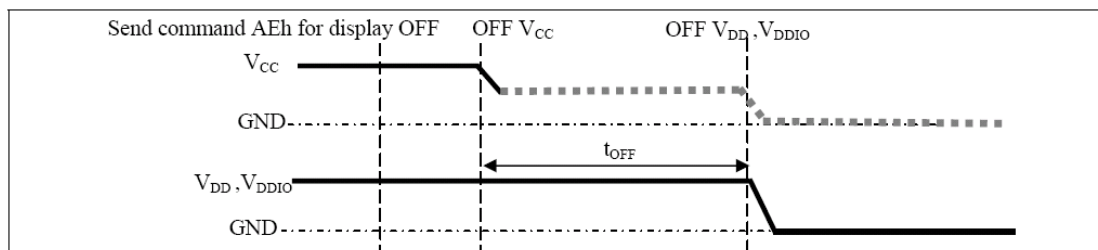
Power ON sequence:

1. Power ON V_{DD}, V_{DDIO}.
2. After V_{DD}, V_{DDIO} become stable, set RES# pin LOW (logic low) for at least 3 μ s(t_1) and then HIGH (logic high).
3. After set RES# pin LOW (logic low), wait for at least 3 μ s(t_2). Then Power ON V_{CC}.(1)
4. After V_{CC} become stable, send command AFh for display ON. SEG/COM will be ON after 100ms(t_{AF}).



Power OFF sequence:

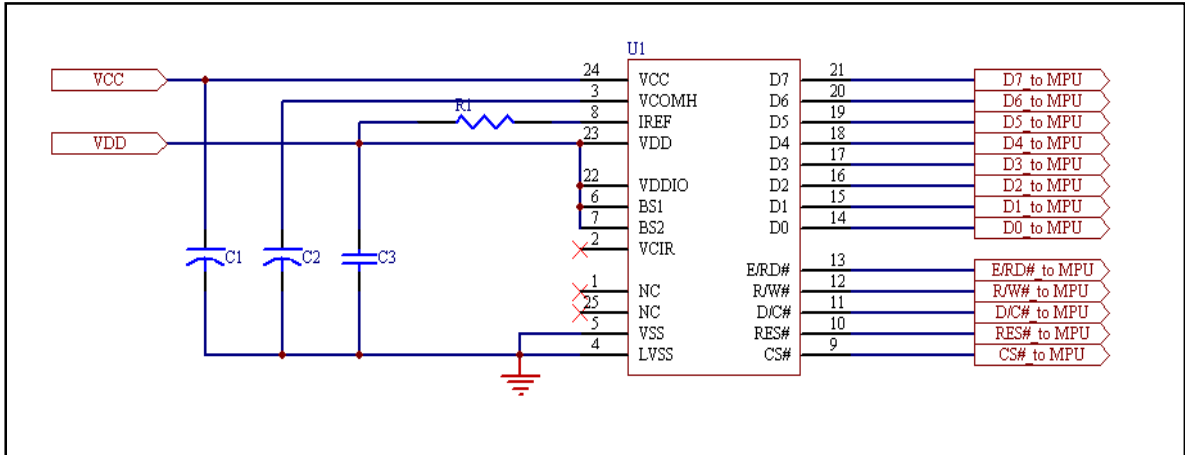
1. Send command AEh for display OFF.
2. Power OFF V_{CC}. (1), (2)
3. Wait for t_{OFF} . Power OFF V_{DD}, V_{DDIO}. (where Minimum t_{OFF} =80ms, Typical t_{OFF} =100ms)



Note:

- (1) Since an ESD protection circuit is connected between V_{DD}, V_{DDIO} and V_{CC}, V_{CC} becomes lower than V_{DD} whenever V_{DD}, V_{DDIO} is ON and V_{CC} is OFF as shown in the dotted line of V_{CC} in above figures.
- (2) V_{CC} should be disabled when it is OFF.

8.2 APPLICATION CIRCUIT



U1: 128x96 OLED module

C1: 4.7uF, tantalum type

C2: 1uF, tantalum type

C3: 0.1uF

R1: 200 K ohm, tolerance 1%

8.3 COMMAND TABLE

Refer to IC Spec.: SSD1329

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9. RELIABILITY TEST CONDITIONS

No.	Items	Specification	Quantity
1	High temp. (Non-operation)	85°C, 240hrs	5
2	High temp. (Operation)	70°C, 120hrs	5
3	Low temp. (Operation)	-40°C, 120hrs	5
4	High temp. / High humidity (Operation)	65°C, 90%RH, 120hrs	5
5	Thermal shock (Non-operation)	-40°C ~85°C (-40°C /30min; transit /3min; 85°C /30min; transit /3min) 1cycle: 66min, 100 cycles	5
6	Vibration	Frequency : 5~50HZ, 0.5G Scan rate : 1 oct/min Time : 2 hrs/axis Test axis : X, Y, Z	1 Carton
7	Drop	Height: 120cm Sequence : 1 angle · 3 edges and 6 faces Cycles: 1	1 Carton
8	ESD (Non-operation)	Air discharge model, ±8kV, 10 times	5

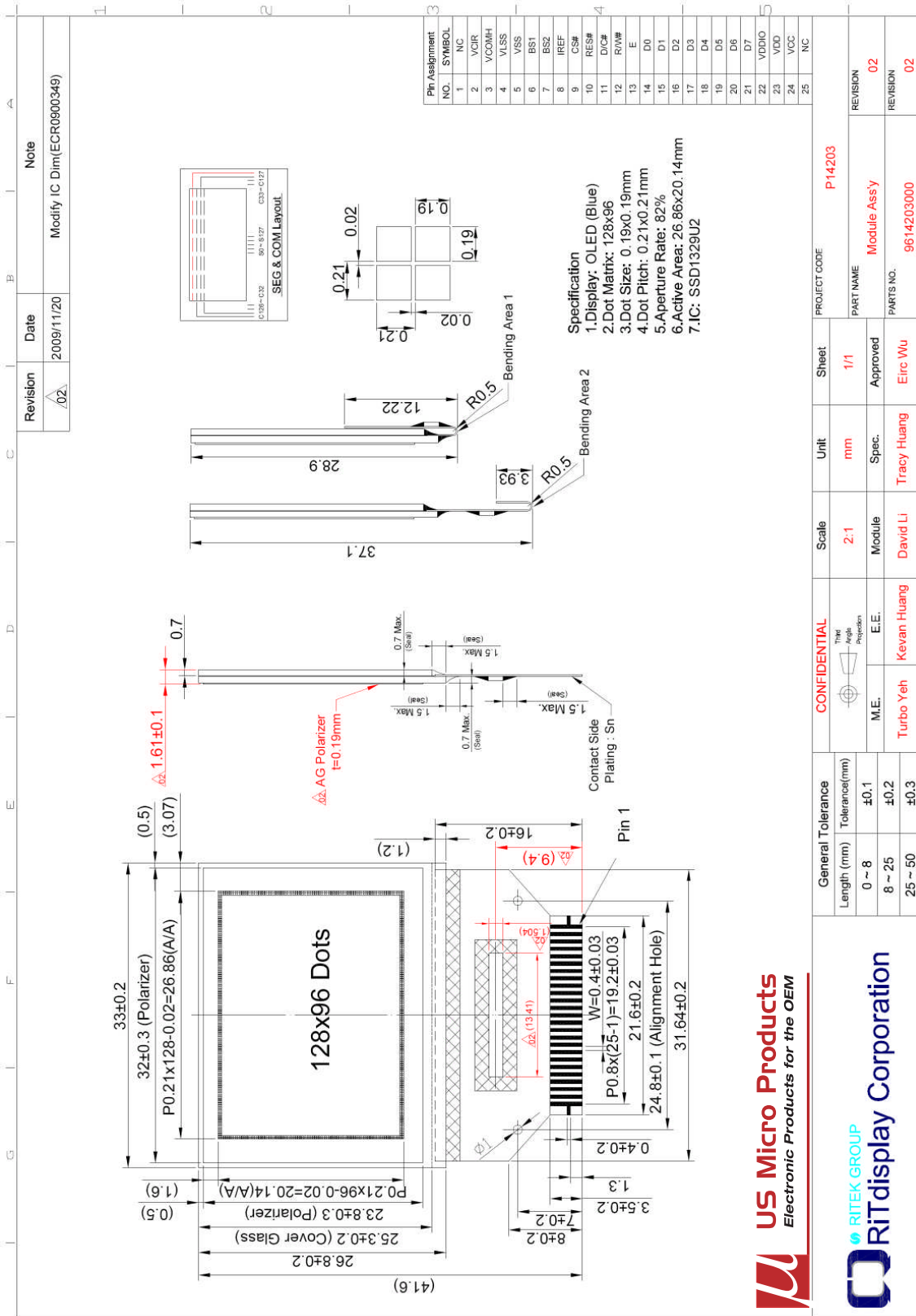
Test and measurement conditions

1. All measurements shall not be started until the specimens attain to temperature stability.
2. All-pixels-on is used as operation test pattern.
3. The degradation of Polarizer are ignored for item 1, 4 & 5.

Evaluation criteria

1. The function test is OK.
2. No observable defects.
3. Luminance: > 50% of initial value.
4. Current consumption: within \pm 50% of initial value.

10. EXTERNAL DIMENSION



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11. PACKING SPECIFICATION

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	Revision A.3	Date 2009/03/24	Note Modify Tray & Packing Amount
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① P14203 Module
P/N:9614203000
Face up, rotate packing
面朝上, 旋轉堆疊

② Packing Tray
P/N:3008000234
330x270x8.7mm, t=0.7mm

③ 5G Silica Gel Desiccants
5G 矽膠乾吸劑
P/N:3010000002

④ Vacuum Bag ONY/LDPE
真空包裝袋 ONY/LDPE
P/N:3003000012
480x285x60mm
Vacuum Packing:4 sec
抽真空4秒

⑤ Antistatic Bubble Bag
抗靜電氣泡袋
P/N:3003000016
440x(350~450)mm

⑥ Pizza Box
P/N:3001000005
345x285x88 B corrugated
B 款

⑦ 單色 Carton
P/N:3000000009
380x294x175mm

⑧ Label
標籤
P/N:3006000000
x2 pcs

⑨ Tape
封箱膠帶
P/N:3208000125

⑩ Label
標籤
P/N:3006000000
x1 pcs

x 1 pcs(empty)

x 20 pcs

x 21 pcs

x 2 pcs

rotate stack
旋轉堆疊

Item	Part No.	Description	QTY
1	9614203000	P14203 Module Assy	1360
2	3008000234	Tray 330x270x8.7mm, PS, t=0.7mm	42
3	3010000002	5G Silica Gel Desiccants	8
4	3003000012	Vacuum Bag ONY/LDPE	2
5	3003000016	Antistatic Bubble Bag 440x(350~450)mm	2
6	3001000005	Pizza Box 345x285x88 B corrugated	2
7	3000000009	Carton , 385x305x203mm	1
8	3006000000	Label	3
9	3208000125	Tape ,W=48mm, L=910cm	

General Tolerance		Scale	Unit	Sheet	PROJECT CODE
Length (mm)	Tolerances(mm)	1:3.5	mm	1/1	P14203
0 ~ 8	±0.1			Approved	PART NAME
8 ~ 25	±0.2			Strong Tsal	Packing Tray Instruction
25 ~ 50	±0.3				PARTS NO.
					9914203000
					VERSION
					03



12. APPENDIXES

APPENDIX 1: DEFINITIONS

A. DEFINITION OF CHROMATICITY COORDINATE

The chromaticity coordinate is defined as the coordinate value on the CIE 1931 color chart for R, G, B, W.

B. DEFINITION OF CONTRAST RATIO

The contrast ratio is defined as the following fomula:

$$\text{Contrast Ratio} = \frac{\text{Luminance of all pixels on measurement}}{\text{Luminance of all pixels off measurement}}$$

C. DEFINITION OF RESPONSE TIME

The definition of turn-on response time T_r is the time interval between a pixel reaching 10% of steady state luminance and 90% of steady state luminance. The definition of turn-off response time T_f is the time interval between a pixel reaching 90% of steady state luminance and 10% of steady state luminance. It is shown in Figure 2.

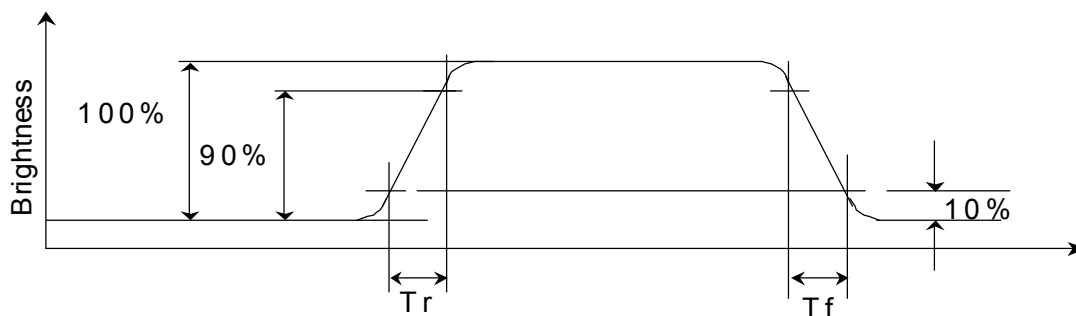


Figure 2 Response time

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D. DEFINITION OF VIEWING ANGLE

The viewing angle is defined as Figure 3. Horizontal and vertical (H & V) angles are determined for viewing directions where luminance varies by 50% of the perpendicular value.

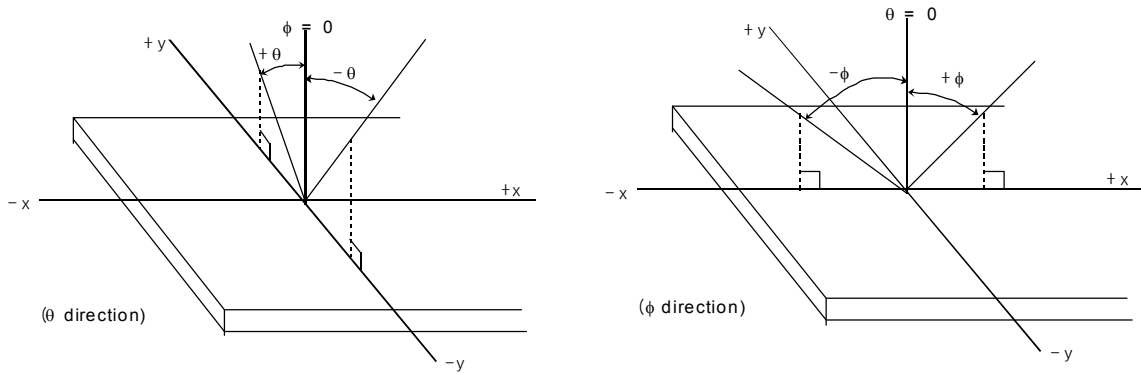


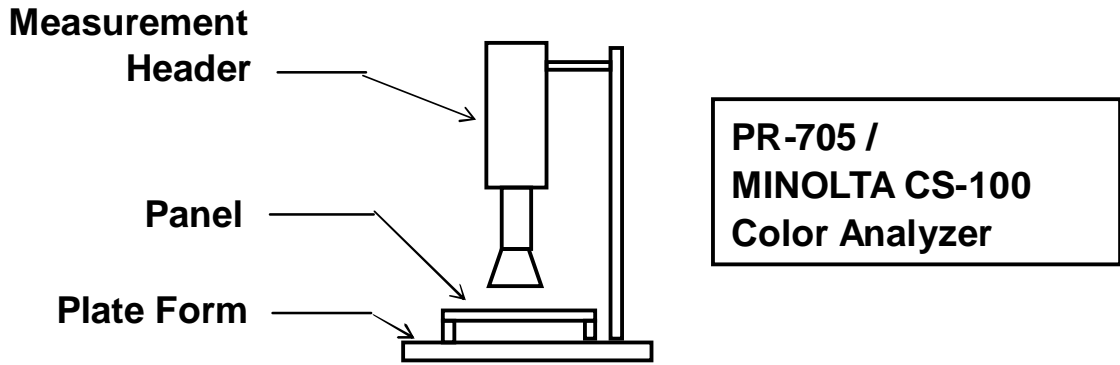
Figure 3 Viewing angle

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APPENDIX 2: MEASUREMENT APPARATUS

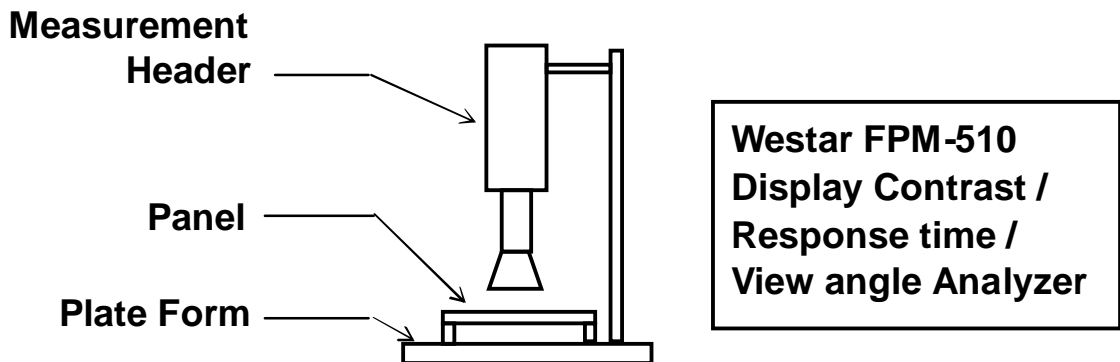
A. LUMINANCE/COLOR COORDINATE

PHOTO RESEARCH PR-705, MINOLTA CS-100



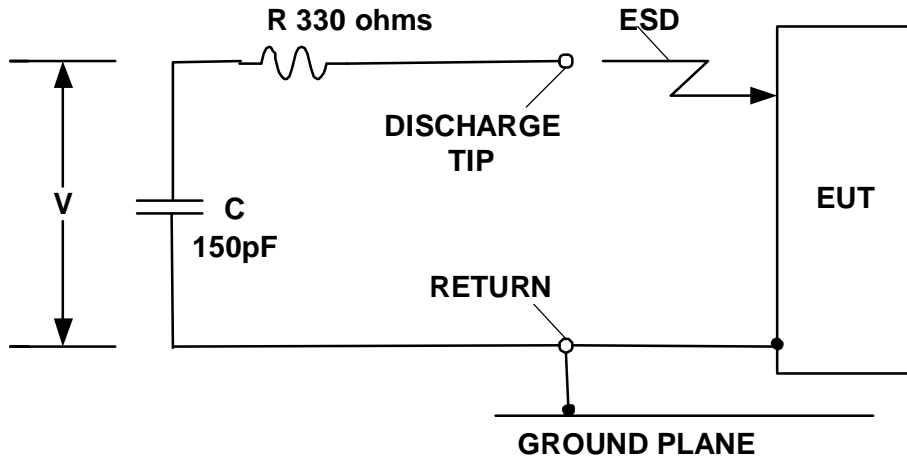
B. CONTRAST / RESPONSE TIME / VIEW ANGLE

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C. ESD ON AIR DISCHARGE MODE



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APPENDIX 3: PRECAUTIONS

A. RESIDUE IMAGE

Because the pixels are lighted in different time, the luminance of active pixels may reduce or differ from inactive pixels. Therefore, the residue image will occur. To avoid the residue image, every pixel needs to be lighted up uniformly.

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