

# PMOLED SPECIFICATION

Part Number	USMP-P024-128064WBI-B0
Display Size	2.4"
Resolution	128 x 64
Color	White
Panel Size	60.5 (W) x 37 (H)
Active Area	55.01 (W) x 27.49 (H)
IC	SPD0301
Interface	Parallel, SPI, I <sup>2</sup> C
Operating Temp.	-40 to 70°C

FOR ADDITIONAL INFORMATION  
PLEASE CONTACT:  
[engineering@usmicroproducts.com](mailto:engineering@usmicroproducts.com)

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## REVISION RECORD

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## **1. SCOPE**

The purpose of this specification is to define the general provisions and quality requirements that apply to the supply of display cells manufactured by USMP. This document, together with the Module Assembly Drawing, is the highest-level specification for this product. It describes the product, identifies supporting documents and contains specifications.

## **2. WARRANTY**

USMP warrants that the products delivered pursuant to this specification (or order) will conform to the agreed specifications for twelve (12) months from the shipping date ("Warranty Period"). USMP is obligated to repair or replace the products which are found to be defective or inconsistent with the specifications during the Warranty Period without charge, on condition that the products are stored or used as the conditions specified in the specifications. Nevertheless, USMP is not obligated to repair or replace the products without charge if the defects or inconsistency are caused by the force majeure or the reckless behaviors of the customer.

After the Warranty Period, all repairs or replacements of the products are subject to charge.

## **3. FEATURES**

- Small molecular organic light emitting diode.
- Color : White
- Panel resolution : 128\*64
- Driver IC : SPD0301
- Excellent Quick response time : 10 $\mu$ s
- Extremely thin thickness for best mechanism design : 2.027 mm
- High contrast : 2000:1
- Wide viewing angle : 160°
- Strong environmental resistance.
- 8-bit 6800/8080-series parallel interface, Serial Peripheral Interface, I<sup>2</sup>C Interface.
- Wide range of operating temperature : -40 to 70 °C
- Anti-glare polarizer.

#### **4. MECHANICAL DATA**

NO	ITEM	SPECIFICATION	UNIT
1	Dot Matrix	128 x 64	dot
2	Dot Size	0.4 (W) x 0.4 (H)	mm <sup>2</sup>
3	Dot Pitch	0.43 (W) x 0.43 (H)	mm <sup>2</sup>
4	Aperture Rate	86	%
5	Active Area	55.01 (W) x 27.49 (H)	mm <sup>2</sup>
6	Panel Size	60.5 (W) x 37 (H)	mm <sup>2</sup>
7	Panel Thickness	1.82 ± 0.1	mm
8	Module Size	60.5 (W) x 47 (H) x 2.027 (T)	mm <sup>3</sup>
9	Diagonal A/A size	2.4	inch
10	Module Weight	8.95 ± 10%	gram

\* Panel thickness includes substrate glass, cover glass and UV glue thickness.

## 5. MAXIMUM RATINGS

ITEM	MIN	MAX	UNIT	Condition	Remark
Supply Voltage ( $V_{DD}$ )	-0.3	4	V	$T_a = 25^\circ\text{C}$	IC maximum rating
Supply Voltage ( $V_{CC}$ )	8	17	V	$T_a = 25^\circ\text{C}$	IC maximum rating
Operating Temp.	-40	70	$^\circ\text{C}$		
Storage Temp	-40	85	$^\circ\text{C}$		
Humidity	-	85	%		
Life Time	14,000	-	Hrs	80cd/m <sup>2</sup> , 50% checkerboard	Note (1)
Life Time	16,000	-	Hrs	70cd/m <sup>2</sup> , 50% checkerboard	Note (2)
Life Time	18,000	-	Hrs	60cd/m <sup>2</sup> , 50% checkerboard	Note (3)

Note:

(A) Under  $V_{CC} = 14\text{V}$

(B) Life time is defined the amount of time when the luminance has decayed to less than 50% of the initial measured luminance.

(1) Setting of 80 cd/m<sup>2</sup> :

- Contrast setting : 0xba
- Frame rate : 105Hz
- Duty setting : 1/64

(2) Setting of 70 cd/m<sup>2</sup> :

- Contrast setting : 0xa0
- Frame rate : 105Hz
- Duty setting : 1/64

(3) Setting of 60 cd/m<sup>2</sup> :

- Contrast setting : 0x83
- Frame rate : 105Hz
- Duty setting : 1/64

## 6. ELECTRICAL CHARACTERISTICS

### 6.1 D.C ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
$V_{CC}$	Operating Voltage	-	13.5	14	14.5	V
$V_{DD}$	Logic Supply Voltage	-	1.65	-	3.3	V
$V_{OH}$	High Logic Output Level	$I_{OUT} = 100\mu A$ , 3.3MHz	$0.9 * V_{DD}$	-	-	V
$V_{OL}$	Low Logic Output Level	$I_{OUT} = 100\mu A$ , 3.3MHz	-	-	$0.1 * V_{DD}$	V
$V_{IH}$	High Logic Input Level	-	$0.8 * V_{DD}$	-	-	V
$V_{IL}$	Low Logic Input Level	-	-	-	$0.2 * V_{DD}$	V
$I_{DD, SLEEP}$	Sleep mode Current	$V_{DD} = 1.65V \sim 3.3V$ , $V_{CC} = 7V \sim 16V$ Display OFF, No panel attached	-	-	10	$\mu A$
$I_{CC, SLEEP}$	Sleep mode Current	$V_{DD} = 1.65V \sim 3.3V$ , $V_{CC} = 7V \sim 16V$ Display OFF, No panel attached	-	-	10	$\mu A$
$I_{CC}$ (No Panel attached)	$V_{CC}$ Supply Current $V_{DD} = 2.8V$ , $V_{CC} = 12$ , $I_{REF} = 10\mu A$ , No Panel attached, Display ON, All ON	Contrast = FFh	-	450	580	$\mu A$
$I_{DD}$ (No Panel attached)	$V_{DD}$ Supply Current $V_{DD} = 2.8V$ , $V_{CC} = 12$ , $I_{REF} = 10\mu A$ , No Panel attached, Display ON, All ON,		-	90	110	$\mu A$
$I_{SEG}$	Segment Output Current, $V_{DD} = 2.8V$ , $V_{CC} = 12V$ , $I_{REF} = 10\mu A$ , Display ON.	Contrast=FFh	280	310	340	$\mu A$
		Contrast=AFh	-	215	-	
		Contrast=7Fh	-	155	-	
		Contrast=3Fh	-	78	-	
		Contrast=0Fh	-	20	-	

## 6.2 ELECTRO-OPTICAL CHARACTERISTICS

### PANEL ELECTRICAL SPECIFICATIONS

PARAMETER	MIN	TYP.	MAX	UNITS	COMMENTS
Normal mode current consumption	-	35	37	mA	All (100%) pixels on
Standby mode current consumption	-	2	3	mA	Standby mode 10% pixels on
Normal mode power consumption	-	490	518	mW	All pixels on
Standby mode power consumption	-	28	42	mW	Standby mode 10% pixels on
Pixel Luminance	50	70		cd/m <sup>2</sup>	Display Average
Standby Luminance		15		cd/m <sup>2</sup>	
CIE <sub>x</sub> (White)	0.26	0.30	0.34		CIE1931
CIE <sub>y</sub> (White)	0.29	0.33	0.37		CIE1931
Dark Room Contrast	2000:1				
Viewing Angle	160			degree	
Response Time		10		μs	

(1) Normal mode condition :

- Driving Voltage : 14V
- Contrast setting : 0xa0
- Frame rate : 105Hz
- Duty setting : 1/64

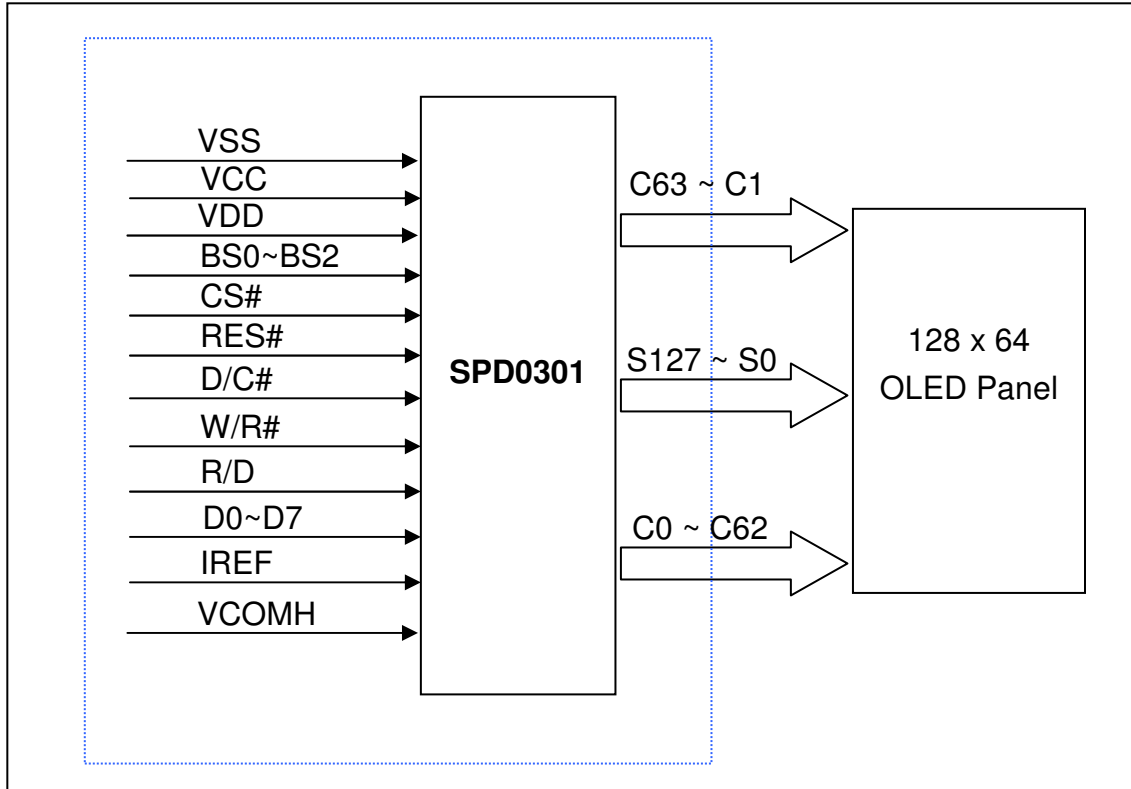
(2) Standby mode condition :

- Driving Voltage : 14V
- Contrast setting : 0x0a
- Frame rate : 105Hz
- Duty setting : 1/64

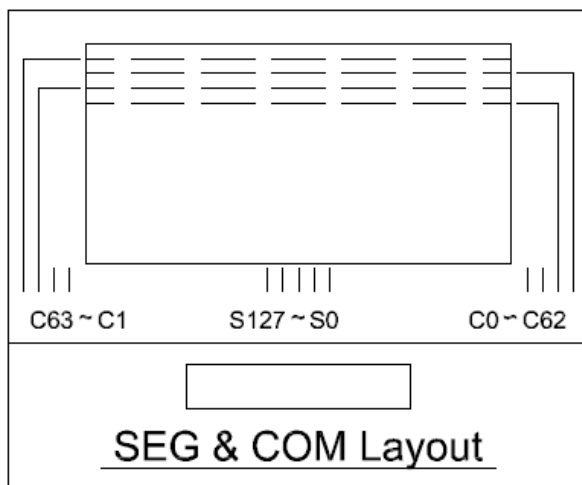


## 7. INTERFACE

### 7.1 FUNCTION BLOCK DIAGRAM



### 7.2 PANEL LAYOUT DIAGRAM



### 7.3 PIN ASSIGNMENTS

PIN NAME	PIN NO	DESCRIPTION
VSS	1	Ground pin.
VCC	2	Power supply for panel driving voltage.
VDD	3	Power supply pin for core logic operation.
BS0	4	MCU bus interface selection pins.
BS1	5	
BS2	6	
CS#	7	This pin is the chip select input connecting to the MCU.
RES#	8	This pin is reset signal input.
D/C#	9	This pin is Data/Command control pin connecting to the MCU.
W/R#	10	This pin is read / write control input pin connecting to the MCU interface.
R/D	11	This pin is MCU interface input.
D0	12	<p>These pins are bi-directional data bus connecting to the MCU data bus. Unused pins are recommended to tie LOW.</p> <p>When serial interface mode is selected, D0 will be the serial clock input: SCLK; D1 will be the serial data input: SDIN and D2 should be kept NC.</p> <p>When I2C mode is selected, D2, D1 should be tied together and serve as SDAout, SDAin in application and D0 is the serial clock input, SCL.</p>
D1	13	
D2	14	
D3	15	
D4	16	
D5	17	
D6	18	
D7	19	
IREF	20	
VCOMH	21	COM signal deselected voltage level. A capacitor should be connected between this pin and VSS.
VCC	22	Power supply for panel driving voltage.
VSS	23	Ground pin.

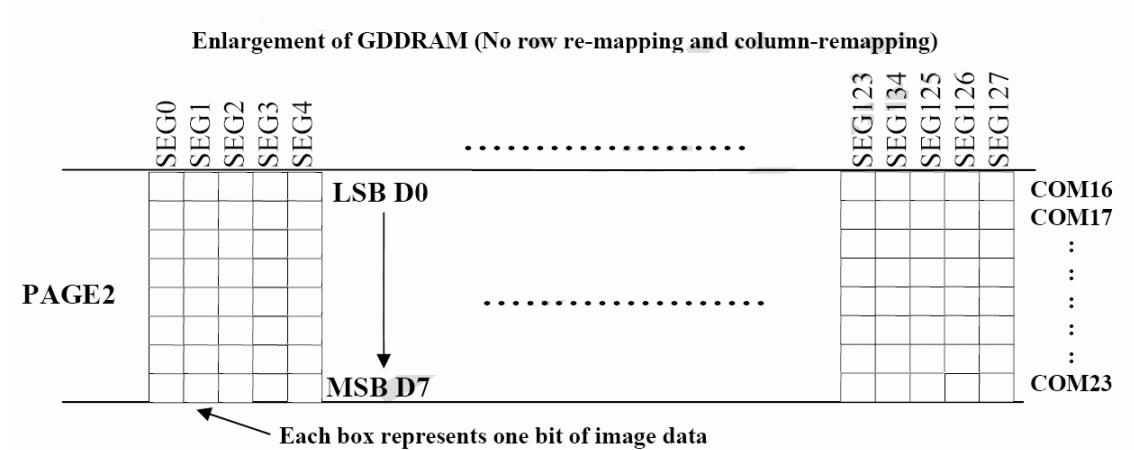
### 7.4 GRAPHIC DISPLAY DATA RAM ADDRESS MAP

The GDDRAM is a bit mapped static RAM holding the bit pattern to be displayed. The size of the RAM is 128 x 64 bits and the RAM is divided into eight pages, from PAGE0 to PAGE7, which are used for monochrome 128x64 dot matrix display, as shown in below figures.

GDDRAM pages structure of SPD0301

		Row re-mapping
PAGE0 (COM0-COM7)	Page 0	PAGE0 (COM 63-COM56)
PAGE1 (COM8-COM15)	Page 1	PAGE1 (COM 55-COM48)
PAGE2 (COM16-COM23)	Page 2	PAGE2 (COM47-COM40)
PAGE3 (COM24-COM31)	Page 3	PAGE3 (COM39-COM32)
PAGE4 (COM32-COM39)	Page 4	PAGE4 (COM31-COM24)
PAGE5 (COM40-COM47)	Page 5	PAGE5 (COM23-COM16)
PAGE6 (COM48-COM55)	Page 6	PAGE6 (COM15-COM8)
PAGE7 (COM56-COM63)	Page 7	PAGE7 (COM 7-COM0)
	SEG0 -----SEG127	
Column re-mapping	SEG127 -----SEG0	

When one data byte is written into GDDRAM, all the rows image data of the same page of the current column are filled (i.e. the whole column (8 bits) pointed by the column address pointer is filled.). Data bit D0 is written into the top row, while data bit D7 is written into bottom row as shown in below figures.



For mechanical flexibility, re-mapping on both Segment and Common outputs can be selected by software.

For vertical shifting of the display, an internal register storing the display start line can be set to control the portion of the RAM data to be mapped to the display (command D3h).

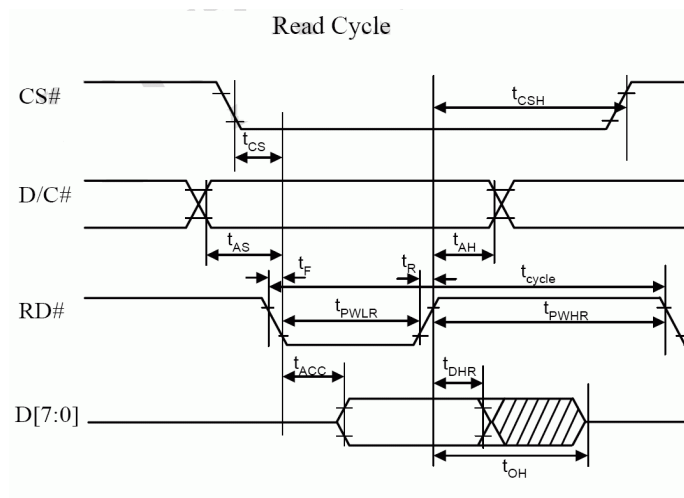
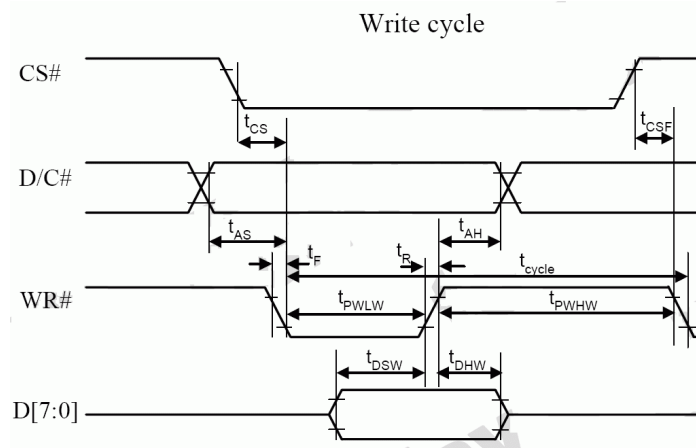
## 7.5 INTERFACE TIMING CHART

8080-Series MCU Parallel Interface Timing Characteristics

( $V_{DD} - V_{SS} = 1.65V \sim 3.3V$ ,  $T_A = 25^\circ C$ )

Symbol	Parameter	Min	Typ	Max	Unit
$t_{cycle}$	Clock Cycle Time	300	-	-	ns
$t_{AS}$	Address Setup Time	10	-	-	ns
$t_{AH}$	Address Hold Time	0	-	-	ns
$t_{DSW}$	Write Data Setup Time	40	-	-	ns
$t_{DHW}$	Write Data Hold Time	7	-	-	ns
$t_{DHR}$	Read Data Hold Time	20	-	-	ns
$t_{OH}$	Output Disable Time	-	-	70	ns
$t_{ACC}$	Access Time	-	-	140	ns
$t_{PWL R}$	Read Low Time	120	-	-	ns
$t_{PWL W}$	Write Low Time	60	-	-	ns
$t_{PWH R}$	Read High Time	60	-	-	ns
$t_{PWH W}$	Write High Time	60	-	-	ns
$t_R$	Rise Time	-	-	40	ns
$t_F$	Fall Time	-	-	40	ns
$t_{CS}$	Chip select setup time	0	-	-	ns
$t_{CSH}$	Chip select hold time to read signal	0	-	-	ns
$t_{CSF}$	Chip select hold time	20	-	-	ns

8080-series parallel interface characteristics



## 8. POWER ON / OFF SEQUENCE & APPLICATION CIRCUIT

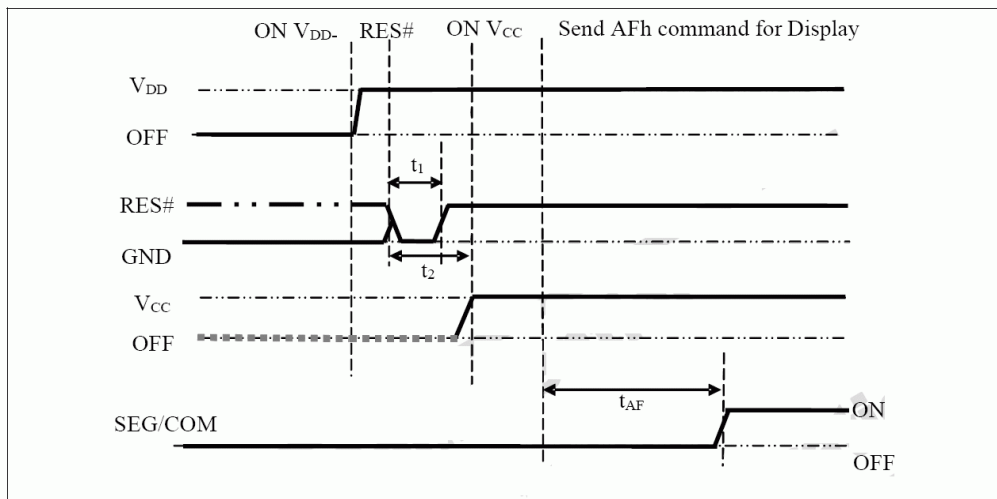
### 8.1 POWER ON / OFF SEQUENCE

The following figures illustrate the recommended power ON and power OFF sequence of SPD0301

#### **Power ON sequence:**

1. Power ON  $V_{DD}$
2. After  $V_{DD}$  become stable, set RES# pin LOW (logic low) for at least 3 $\mu$ s ( $t_1$ )<sup>(3)</sup> and then HIGH (logic high).
3. After set RES# pin LOW (logic low), wait for at least 3 $\mu$ s ( $t_2$ ). Then Power ON  $V_{CC}$ .<sup>(1)</sup>
4. After  $V_{CC}$  become stable, send command AFh for display ON. SEG/COM will be ON after 100ms ( $t_{AF}$ ).

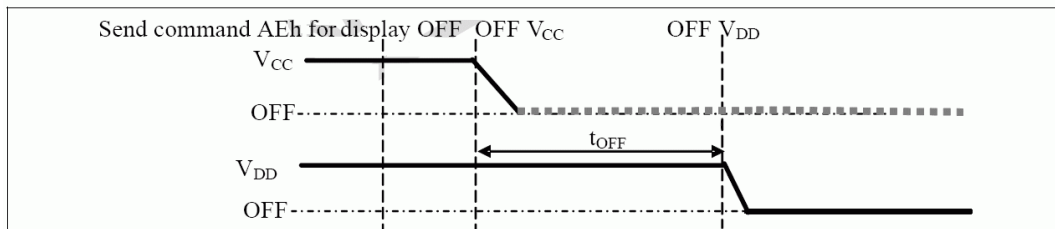
The Power ON sequence



#### **Power OFF sequence:**

1. Send command AEh for display OFF.
2. Power OFF  $V_{CC}$  <sup>(1), (2)</sup>
3. Power OFF  $V_{DD}$  after  $t_{OFF}$ .<sup>(4)</sup> (where Minimum  $t_{OFF}$ =80ms, Typical  $t_{OFF}$ =100ms)

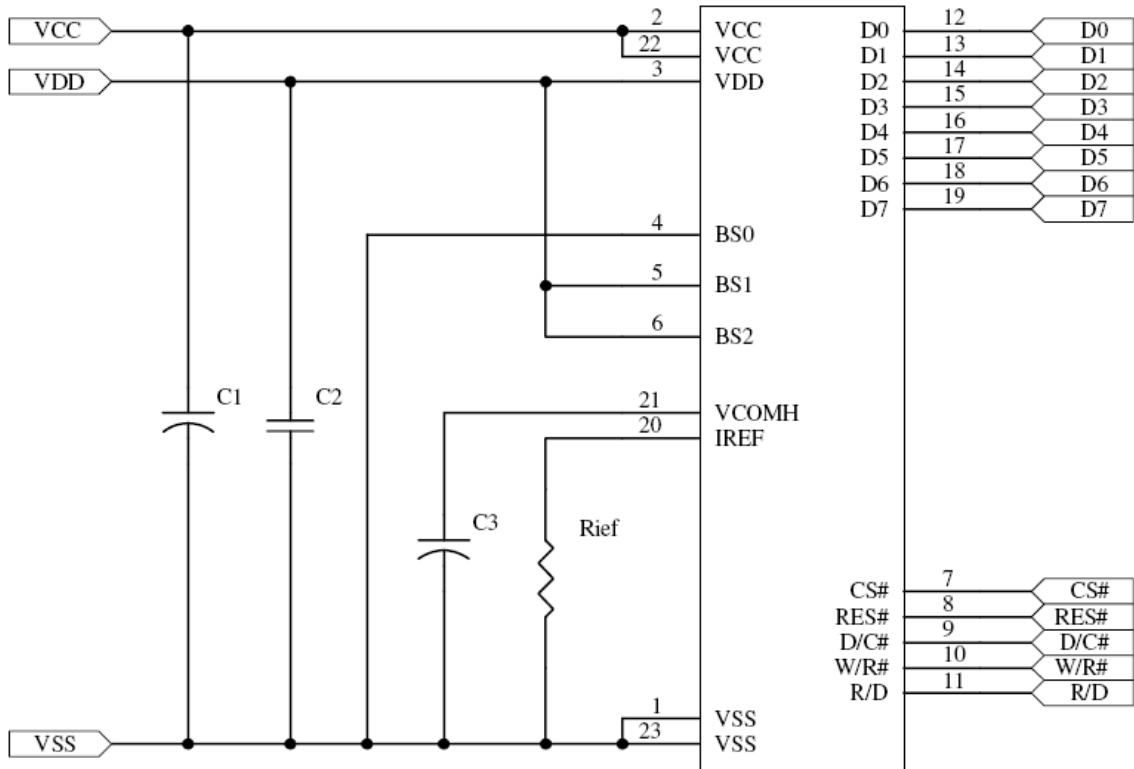
The Power OFF sequence



#### **Note:**

- (1)  $V_{CC}$  should be disabled when it is OFF.
- (2) Power Pins ( $V_{DD}$ ,  $V_{CC}$ ) can never be pulled to ground under any circumstance.
- (3) The register values are reset after  $t_1$ .
- (4)  $V_{DD}$  should not be Power OFF before  $V_{CC}$  Power OFF.

## 8.2 APPLICATION CIRCUIT



### Component:

C1, C3: 4.7uF/35V(Tantalum type) or VISHAY (572D475X0025A2T)

C2: 1uF/16V

Rief: 1M ohm (0603) 1%

**This circuit is for 8080 8bits interface**

## 8.3 COMMAND TABLE

Refer to IC Spec.: SPD0301

## 9. RELIABILITY TEST CONDITIONS

No.	Items	Specification	Quantity
1	High temp. (Non-operation)	85 °C, 240hrs	5
2	High temp. (Operation)	70 °C, 120hrs	5
3	Low temp. (Operation)	-40 °C, 120hrs	5
4	High temp. / High humidity (Operation)	65 °C, 90%RH, 120hrs	5
5	Thermal shock (Non-operation)	-40 °C ~85 °C (-40 °C /30min; transit /3min; 85 °C /30min; transit /3min) 1cycle: 66min, 100 cycles	5
6	Vibration	Frequency : 5~50HZ, 0.5G Scan rate : 1 oct/min Time : 2 hrs/axis Test axis : X, Y, Z	1 Carton
7	Drop	Height: 120cm Sequence : 1 angle 、 3 edges and 6 faces Cycles: 1	1 Carton
8	ESD (Non-operation)	Air discharge model, ±8kV, 10 times	5

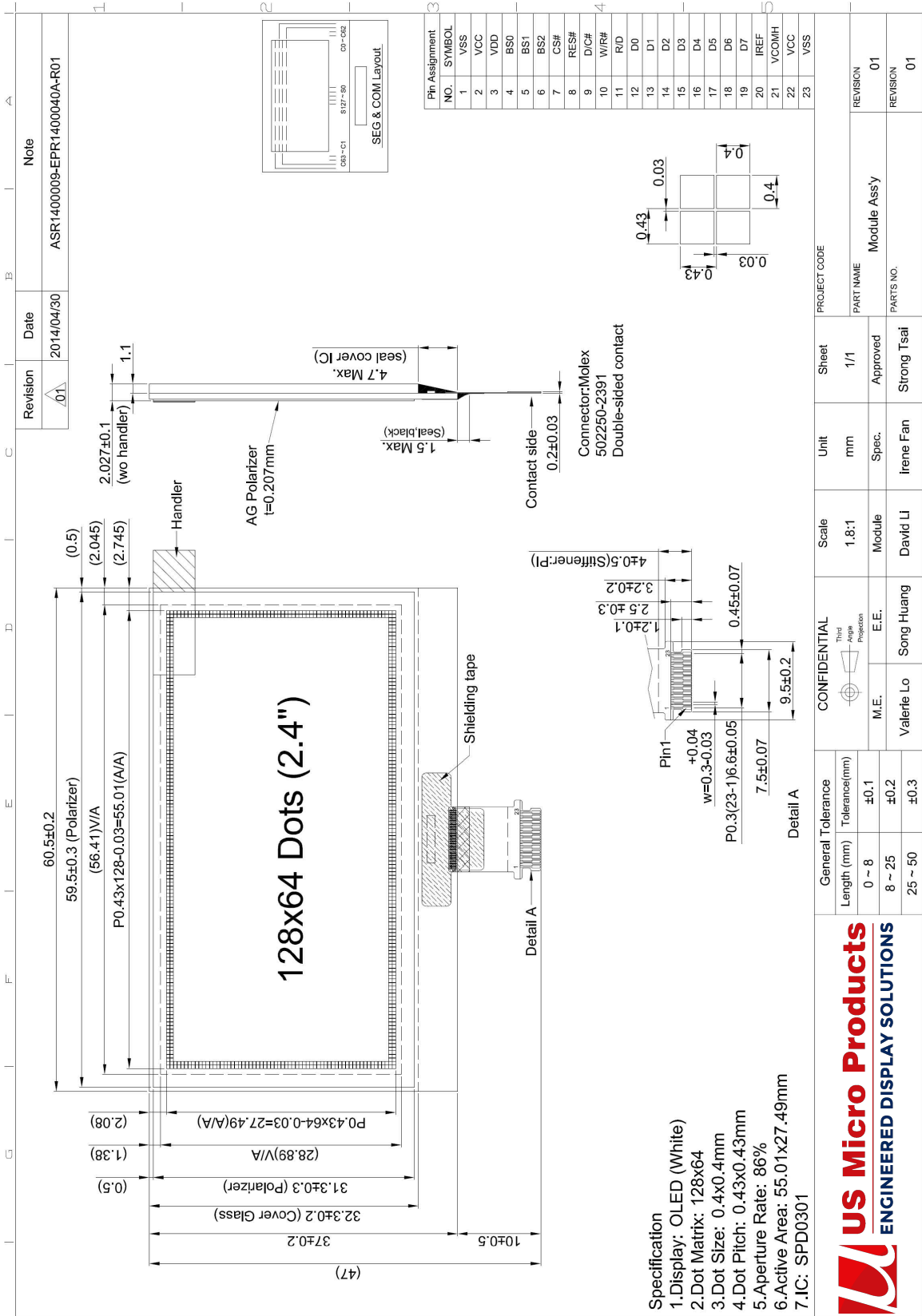
### **Test and measurement conditions**

1. All measurements shall not be started until the specimens attain to temperature stability.
2. All-pixels-on is used as operation test pattern.
3. The degradation of Polarizer are ignored for item 1, 4 & 5.

### **Evaluation criteria**

1. The function test is OK.
2. No observable defects.
3. Luminance: > 50% of initial value.
4. Current consumption: within  $\pm$  50% of initial value.

# 10. EXTERNAL DIMENSION





# 11. PACKING SPECIFICATION

	Revision	Date	Note
△01	2014/05/15	Packing Tray Instruction	

① P/N: Face Up  
旋轉放置

② Packing Tray  
P/N: 3008000106  
330x270x8.7mm, t=0.7mm

③ 5G 矽膠乾膜劑  
P/N: 3010000003  
x4

④ 真空包裝袋 ONY/LDPE  
P/N: 3003000012  
480x285x90mm  
抽真空4秒

⑤ Antistatic Bubble Bag  
P/N: 3003000016  
440x(350+450)mm

⑥ Pizza Box  
P/N: 3001000005  
345x285x88, B浪

⑦ 單色 Carton  
P/N: 3000000009  
385x305x203mm

⑧ Label  
P/N: 3006000000  
x2 pcs

⑨ 封箱膠帶  
P/N: 3208000125

x 1 pcs (empty)

x 15 pcs  
旋轉堆疊

x 16 pcs

x 2 pcs

Item	Part No.	Description	QTY
1		Module Assy White	480
2	3008000106	Tray 330x270x8.7mm, t=0.7mm	32
3	3010000003	5G 矽膠乾膜劑	8
4	3003000012	真空包裝袋 480x285x90mm	2
5	3003000016	Antistatic Bubble Bag 440x(350+450)mm	2
6	3001000005	Pizza Box 345x285x88, B浪	2
7	3000000009	單色 Carton, 385x305x203mm	1
8	3006000000	Label	3
9	3208000125	封箱膠帶	

General Tolerance		Scale		Unit		Sheet	
Length (mm)	Tolerance(mm)	1:9	Module	mm	1/1	PROJECT CODE	
0 ~ 8	±0.1			Spec.	Approved	PART NAME	
8 ~ 25	±0.2			Module	David Li	Packing Tray Instruction	
25 ~ 50	±0.3			Spec.	Strong Tsai	PARTS NO.	
				Module		REVISION	
				Module		01	
				Module		REVISION	
				Module		01	



## **12. APPENDIXES**

### **APPENDIX 1: DEFINITIONS**

#### **A. DEFINITION OF CHROMATICITY COORDINATE**

The chromaticity coordinate is defined as the coordinate value on the CIE 1931 color chart for R, G, B, W.

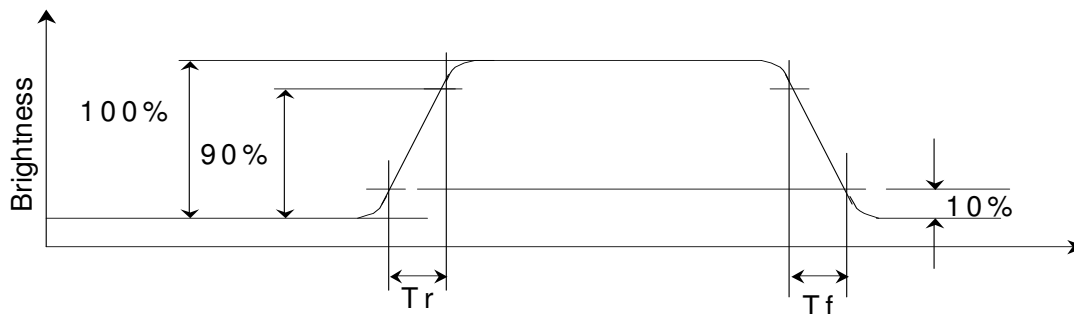
#### **B. DEFINITION OF CONTRAST RATIO**

The contrast ratio is defined as the following formula:

$$\text{Contrast Ratio} = \frac{\text{Luminance of all pixels on measurement}}{\text{Luminance of all pixels off measurement}}$$

#### **C. DEFINITION OF RESPONSE TIME**

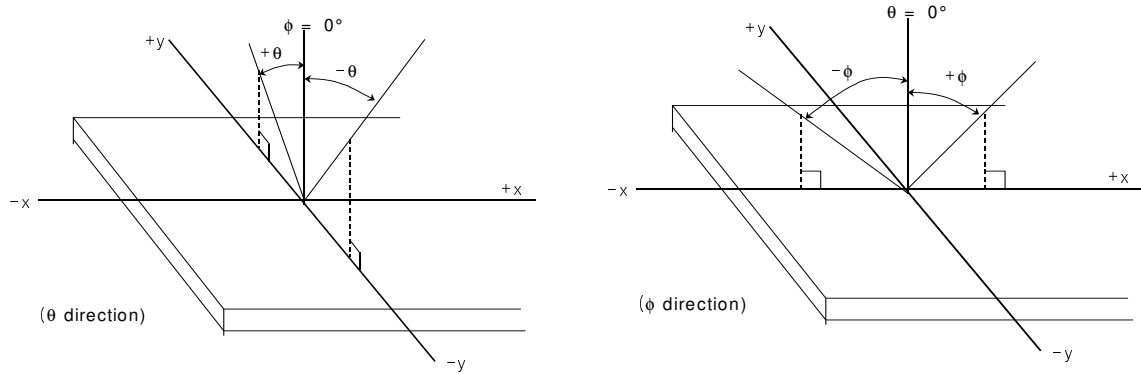
The definition of turn-on response time  $T_r$  is the time interval between a pixel reaching 10% of steady state luminance and 90% of steady state luminance. The definition of turn-off response time  $T_f$  is the time interval between a pixel reaching 90% of steady state luminance and 10% of steady state luminance. It is shown in Figure 2.



**Figure 2 Response time**

## D. DEFINITION OF VIEWING ANGLE

The viewing angle is defined as Figure 3. Horizontal and vertical (H & V) angles are determined for viewing directions where luminance varies by 50% of the perpendicular value.

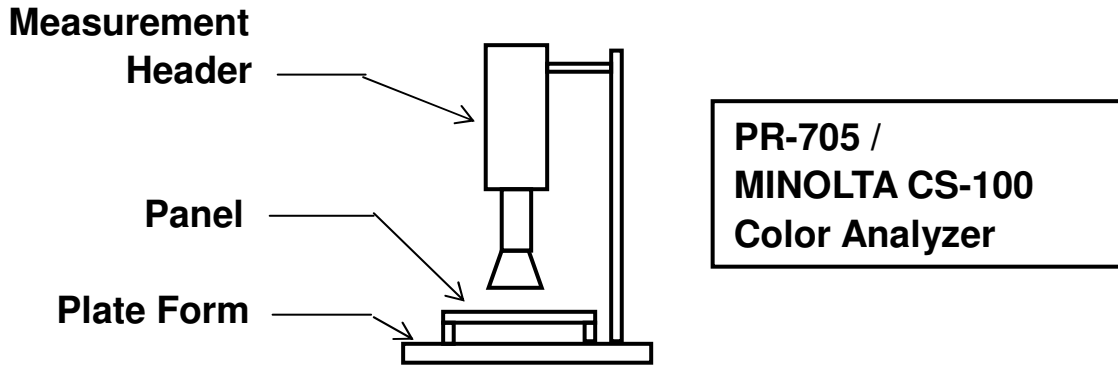


**Figure 3 Viewing angle**

## APPENDIX 2: MEASUREMENT APPARATUS

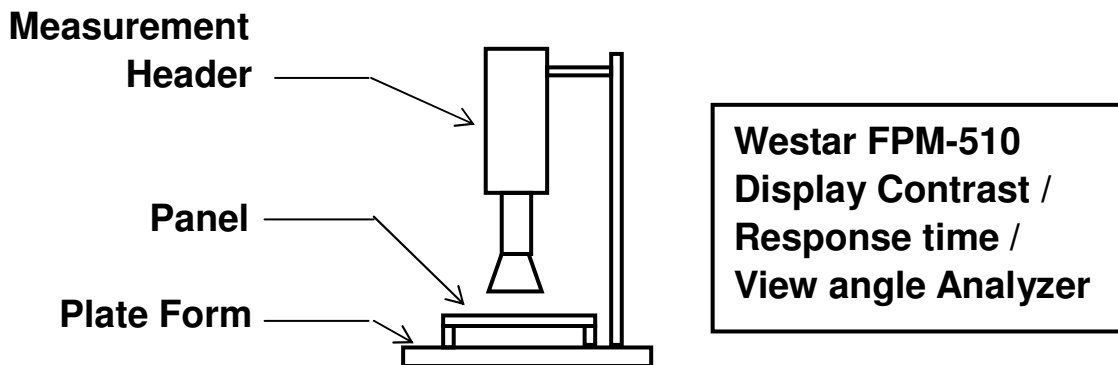
### A. LUMINANCE/COLOR COORDINATE

PHOTO RESEARCH PR-705, MINOLTA CS-100

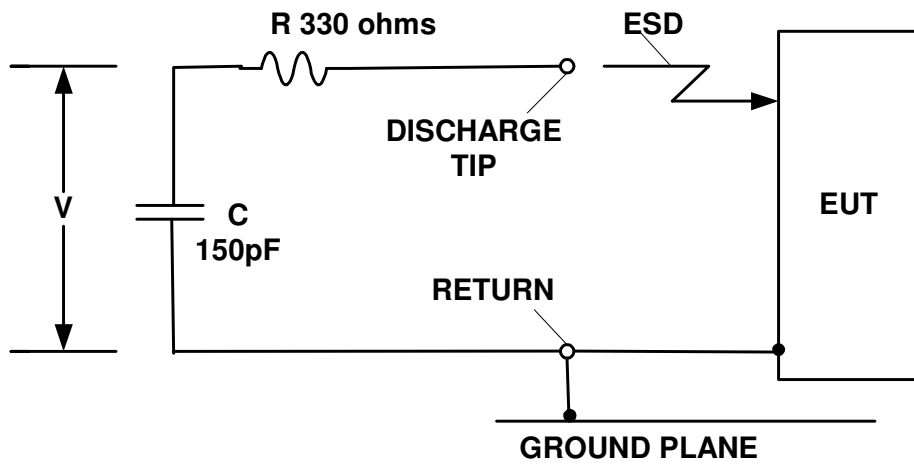


### B. CONTRAST / RESPONSE TIME / VIEWING ANGLE

WESTAR CORPORATION FPM-510



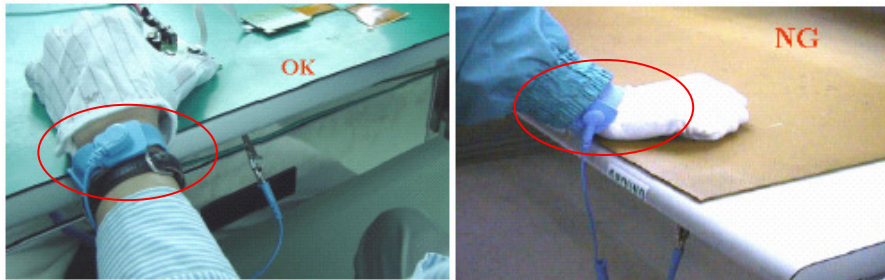
### C. ESD ON AIR DISCHARGE MODE



## APPENDIX 3: PRECAUTIONS FOR USING THE OLED MODULE

### *Precautions for Handling*

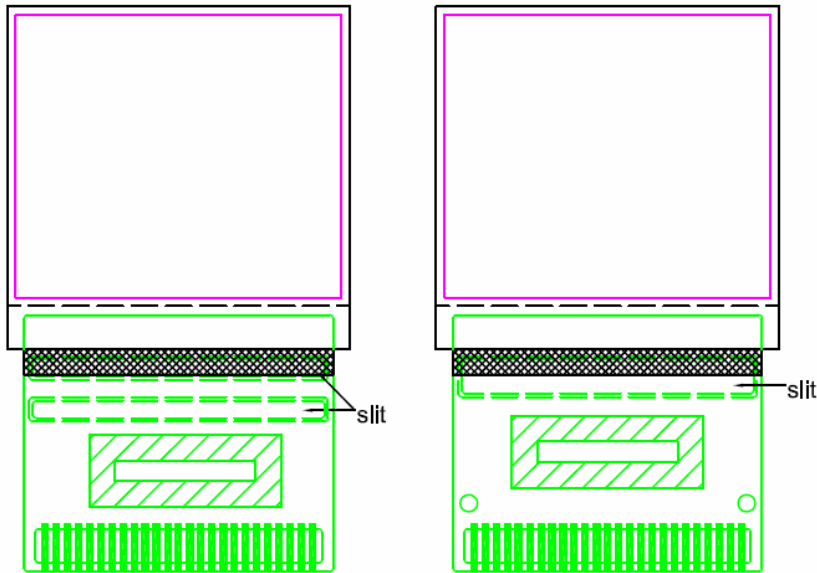
1. When handling the module, wear powder-free antistatic rubber finger cots, and be careful not to bend and twist it.
2. The OLED module is consisted of glass and film, and it should avoid pressure, strong impact, or being dropped from a high position.
3. The OLED module is an electronic component and is subject to damage caused by Electro Static Discharge (ESD). And hence normal ESD precautions must be taken when handling it. Also, appropriate ESD protective environment must be administered and maintained in the production line. When handling and assembling the panel, wear an antistatic wrist strap with the alligator clip attached to the ground to prevent ESD damage on the panel. Also, ground the tools being used for panel assembly and make sure the working environment is not too dry to cause ESD problems. Antistatic wrist strap should touch human body directly instead of gloves. (See below photos).



4. Take out the panel one by one from the holding trays for assembly, and never put the panel on top of another one to avoid the scratch.
5. Avoid jerk and excessive bend on TAB/FPC/COF, and be careful not to let foreign matter or bezel damage the film.
6. When handling and assembling the module (panel + IC), grab the panel, not the TAB/FPC/COF.
7. Use the tweezers to open the clicks on the connector of PCB before the insertion of FPC/COF, and click them back in. Once the FPC/COF sits properly in the connector, use the tweezers to avoid the damages.

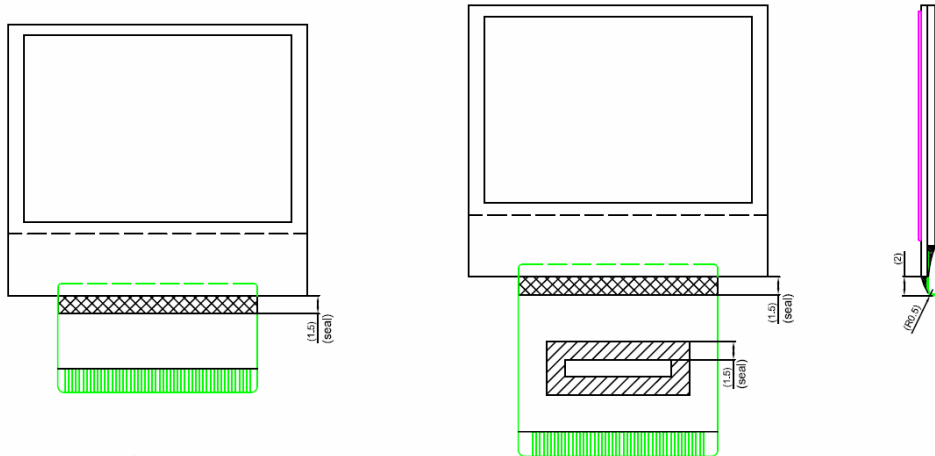


8. Please do not bend the film near the substrate glass. It could cause film peeling and TAB/FPC/COF damage. For TAB, It should bend the slit area as actual OLED it is. For FPC or COF, it is suggested to follow below pictures for instruction (distance between substrate glass and bending area  $>1.5\text{mm}$ ;  $R>0.5\text{mm}$ ).



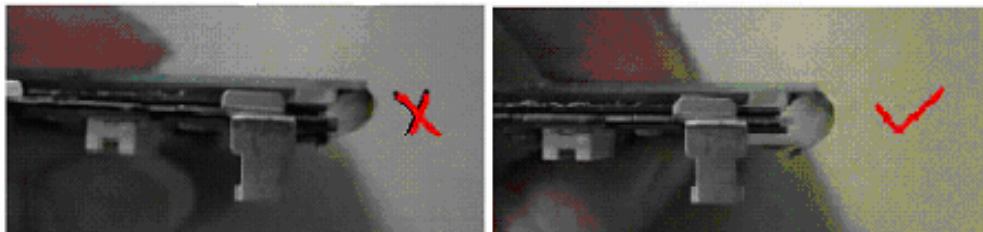
TAB

TAB

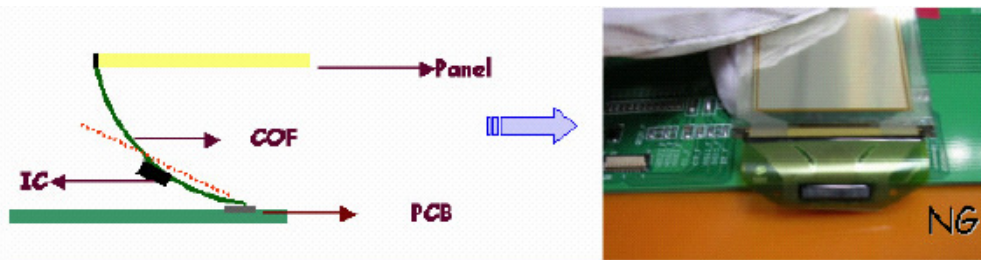
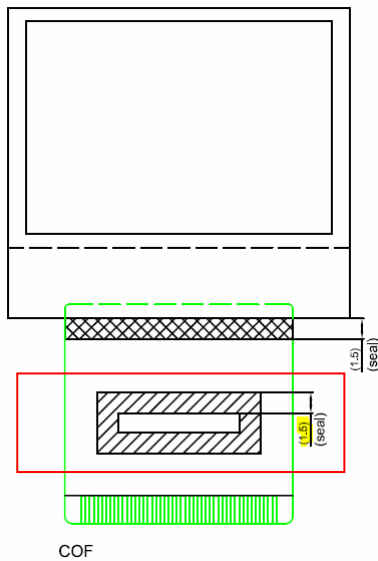


FPC

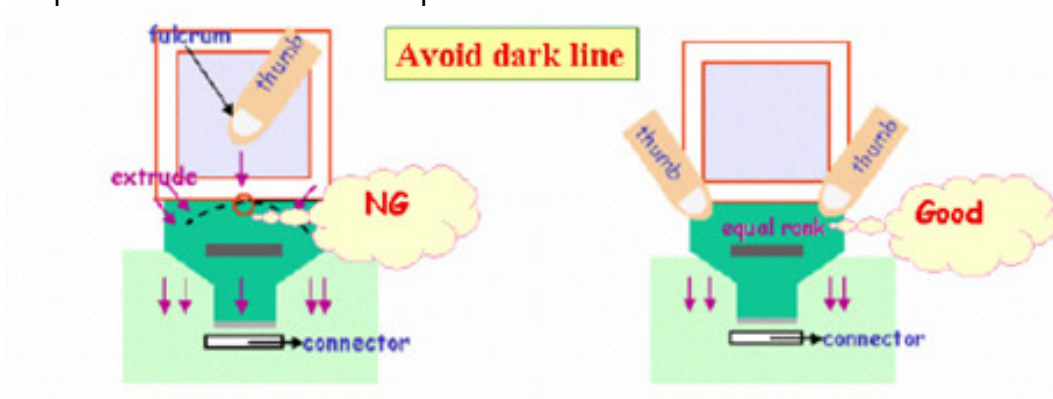
COF



9. Avoid bending the film at IC bonding area. It could damage the IC ILB bonding. It should avoid bending the IC seal area. Please keep the bending distance >1.5mm.



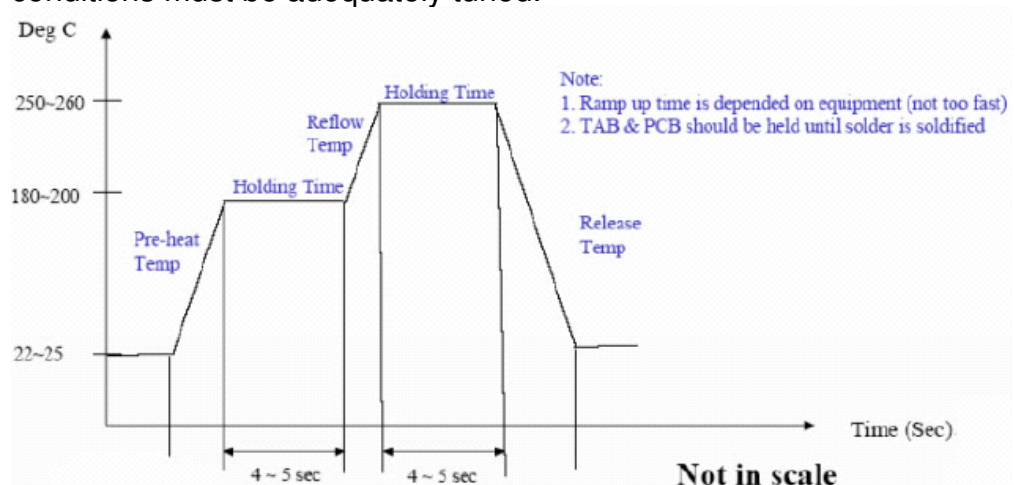
10. Use both thumbs to insert COF into the connector when assembling the panel. Please refer to the photo.



11. The working area for the panel should be kept clean. If the panel is accidentally dropped on the floor, do visual inspection of the panel first. Please use clean-room wiping cloth moistened with alcohol to wipe it off if dirt or grease stains the panel.



12. Do not wipe the pin of film and polarizer with the dry or hard materials that will damage the surface. When cleaning the display surface, use the soft cloth with solvent, IPA or alcohol, to clean.
13. Protection film is applied to the surface of OLED panel to avoid the scratch. Please remove the protective film before assembling it. If the OLED panel has been stored for a long time, the residue adhesive material of the protective film may remain on the display surface after remove the protective film. Please use the soft cloth with solvent, IPA or alcohol, to clean.
14. When hand or hot-bar soldering TAB/FPC onto PCB, make sure the temperature and timing profiles to meet the requirements of soldering specification (the specification depends on the application or optimized by customer) to prevent the damage of IC pins by inappropriate soldering.
15. Solder residues arise from soldering process have to be cleaned up thoroughly before the module assembly.
16. Use the voltage and current settings listed in the specification to do the function test after the module assembly.
17. Suggestion for soldering process:
  - i. TAB Lead- free soldering hot bar process
    1. Use pulse heated bonding tool equipment
    2. Material: Sn/Ag/Cu lead-free solder paste with typical 25um thickness on PCB pad. The TAB pin size and shape may be different, please base on the production line to adjust the thickness of PCB pad and temperature.
    3. Bonding Force:--4kg per centimeter square as the starting point.
    4. Suggested bonding tool temperature & time profile is as below for reference. Since there are differences in TAB soldering pins, soldering technicians' skills, mechanism...etc., the soldering conditions must be adequately tuned.



- ii. TAB Lead- free soldering wire process
  - In case of manual soldering (Lead- free solder wire)
  - 1. Solder wire contact iron directly:  $280\pm 5^{\circ}\text{C}$  at 3-5secs
  - 2. Solder wire contact TAB lead directly (near iron but not contact):  $380\pm 5^{\circ}\text{C}$ , 3-5secs
  - 3. Since there are differences in TAB soldering pins, soldering technicians' skills, mechanism...etc., the soldering conditions must be adequately tuned.
- iii. High temperature will result in rapid heat conduction to IC and might cause damage to IC, so please keep the temperature below  $380^{\circ}\text{C}$ . Also, avoid damaging the polyimide and solder resist which might take place at high temperatures. Refold cycles base on the de-soldering status, if the plating of pin was damaged, it can not be used again.

## Precautions for Electrical

### 1. Design using the settings in the specification

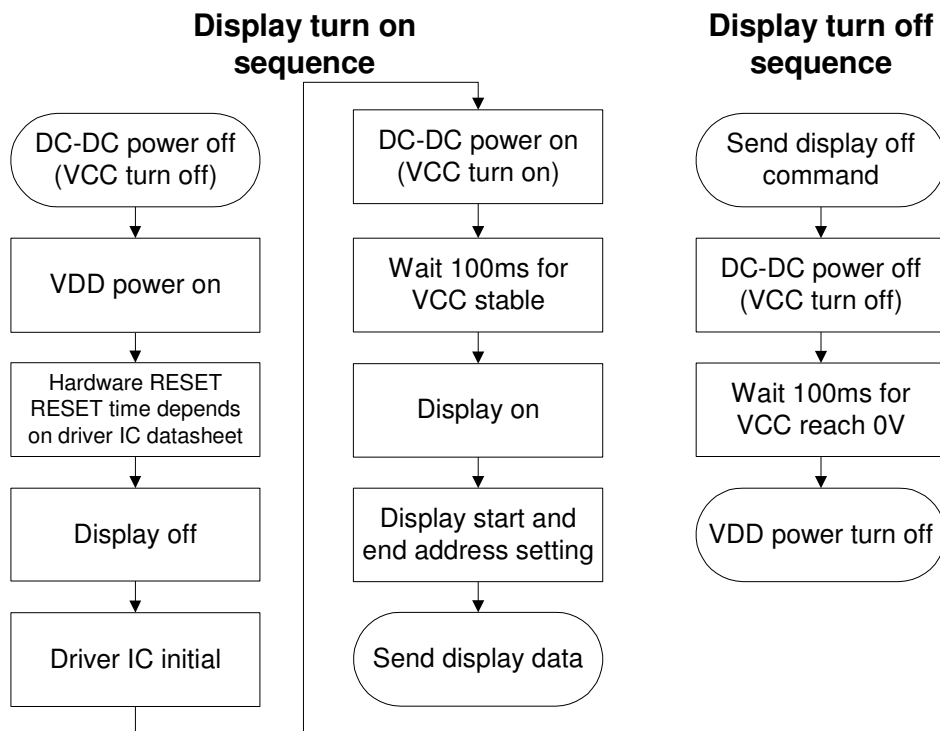
It is very important to design and operate the panel using the settings listed in the specification. It includes voltage, current, frame rate and duty cycle... etc. Operation the OLED outside the range of the specification should be entirely avoided to ensure proper operation of the OLED.

### 2. Maximum Ratings

To ensure the proper operation of the panel, never design the panel with parameters running over the maximum ratings listed in the specification. Also the logic voltages such as VIL and VIH have to be within the specified range in the specification to prevent any improper operation of the panel.

### 3. Power on/off procedure

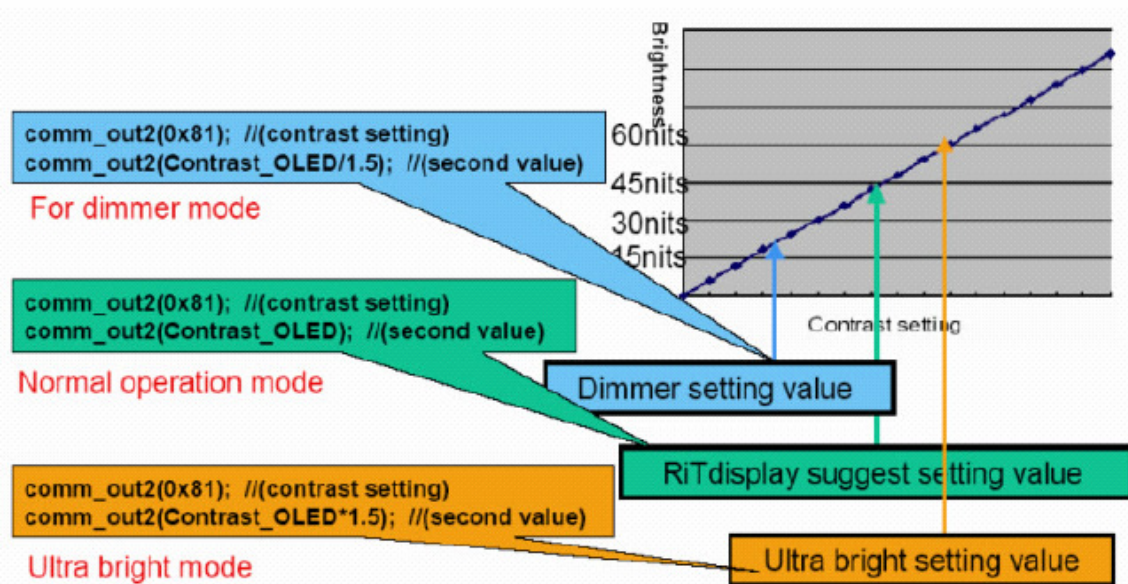
To avoid any inadvertent effects resulting from inappropriate power on/off operations, please follow the directions of power on/off procedure on page 6. Any operation that does not comply with the procedure could cause permanent damage of the IC and should be avoided. When the logic power is not on, do not activate any input signal. Abrupt shutdown of power to the module, while the OLED panel is on, would cause OLED panel malfunction.



#### 4. Power savings

To save power consumption of the OLED, please use partial display or sleep mode when the panel is not fully activated. Also, if possible, make the black background to save power.

The OLED is a self-luminous device and a particular pixel cluster or image can be lit on via software control. So power savings can be achieved by partial display or dimming down the luminance. Depending on the application, the user can choose among Ultra Bright Mode, Normal Operation Mode, and Sleeping Mode. The power consumption is almost in directly proportion to the brightness of the panel, and also in directly proportion to the number of pixels lit on the panel. The customer can save the power by the use of black background and sleeping mode. One benefit from using these design schemes is the extension of the OLED lifetime.



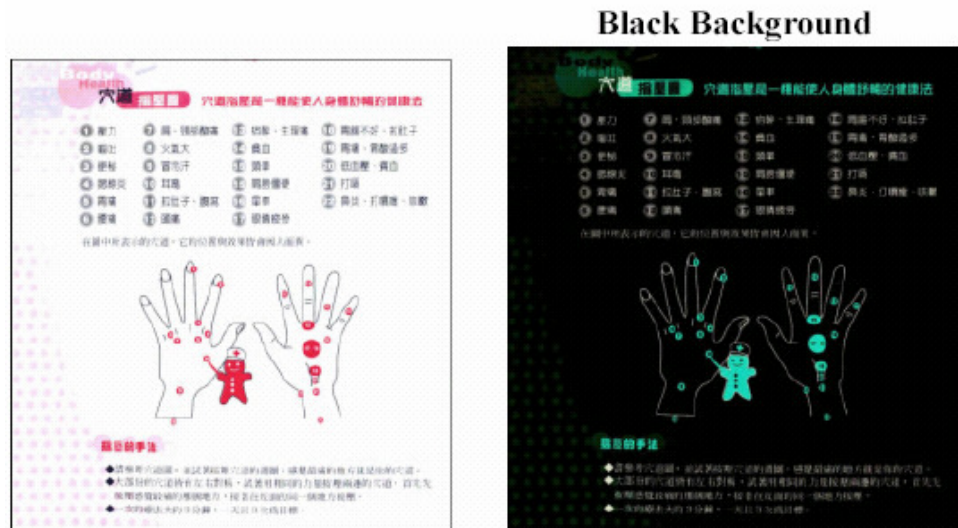
#### 5. Adjusting the luminance of the panel

Although there are a couple of ways to adjust the luminance of the panel, it is strongly recommended that the customer change the contrast setting to adjust the luminance of the panel. Adjusting voltages to achieve desired luminance is not allowed. Be aware that the adjustment of luminance would accompany the change of lifetime of the panel and its power consumption as well.

#### 6. Residual Image (Image Sticking)

The OLED is a self-emissive device. As with other self-emissive device or displays consisting of self-emissive pixels, when a static image frozen for a long period of time is changed to another one with all-pixels-on background, residual image or image sticking is noticed by the human eye. Image sticking is due to the luminance difference or contrast between the pixels that were previously turned on and the pixels that are newly turned on. Image sticking depends on the luminance decay curve of the display. The slower the decay, the less prominent the image sticking is. It is strongly recommended that the user employ the following three strategies to minimize image sticking.

1. Employ image scrolling or animation to even out the lit-on time of each and every pixel on the display, also could use sleeping mode for reduced the residual image and extend the power capacity.
2. Minimize the use of all-pixels-on or full white background in their application because when the panel is turned on full white, the image sticking from previously shown patterns is the most revealing. Black background is the best for power savings, greatest visibility, eye appealing, and dazzling displays
3. If a static logo is used in the reliability test, change the pattern into its inverse (i.e., turn off the while pixels and turn on the previously unlit pixels) and freeze the inverse pattern as long as the original logo is used, so every pixel on the panel can be lit on for about the same time to minimize image sticking, caused by the differential turn-on time between the original and its reverse patterns.



**Scrolling example**

**Example: setup and start**

```

comm_out2(0x26); // scrolling setup
comm_out2(0x08); // scrolling numbers/step
comm_out2(0x00); // start page
comm_out2(0x00); // scrolling step/frame
comm_out2(0x08); // end page
comm_out2(0x2F); // start
    
```

**Example: stop**

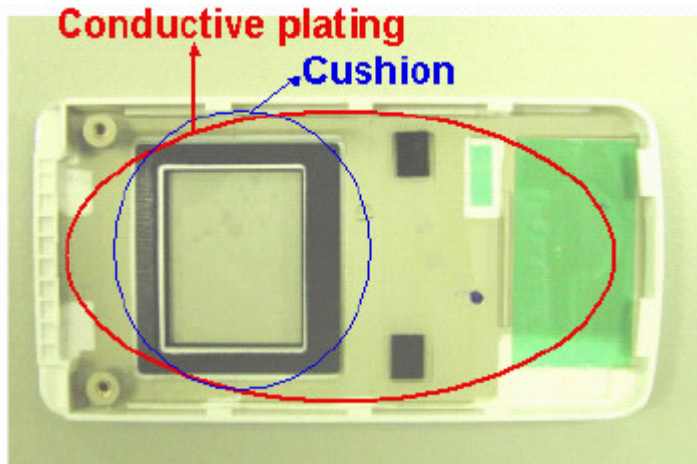
```

comm_out2(0x2E); //stop
    
```

## *Precautions for Mechanical*

### **1. Cushion or Buffer tape on the cover glass**

It is strongly recommended to have a cushion or buffer tape to apply on the panel backside and front side when assembling OLED panel into module to protect it from damage due to excessive extraneous forces.



It is recommended that a plating conductive layer be used in the housing for EMI/EMC protection. And, the enough space should be reserved for the IC placement if the IC thickness is thicker than the TAB film when customer design the PCB.

### **2. Avoid excessive bending of film when handling or designing the panel into the product**

The bending of TAB/COF/FPC has to follow the precautions indicated in the specification, extra bending or excessive extraneous forces should be avoided to minimize the chances of film damage. If bending the film is necessary, please bend the designated bending area only. Please refer to items 8 and 9 of Precautions for Handling for more information.

## *Precautions for Storage and Reliability Test*

### **1. Storage**

Store the packed cartons or packages at  $25^{\circ}\text{C} \pm 5^{\circ}\text{C}$ ,  $55\% \pm 10\% \text{RH}$ . Do not store the OLED module under direct sunlight or UV light. For best panel performance, unpack the cartons and start the production of the panels within six months after the reception of them.

### **2. Reliability Test**

USMP only guarantees the reliability of the OLEDs under the test conditions and durations listed in the specification.