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96x96 White OLED Application Notes

MANUFACTURED BY RITDISPLAY

RITEK GROUP
RiTdisplay Corporation

PART NUMBER:	**USMP-P24001**
DESCRIPTION:	1.0", 96 x 96, White, COG, SSD1327

ISSUE DATE	APPROVED BY (Customer Use Only)	CHECKED BY	PREPARED BY
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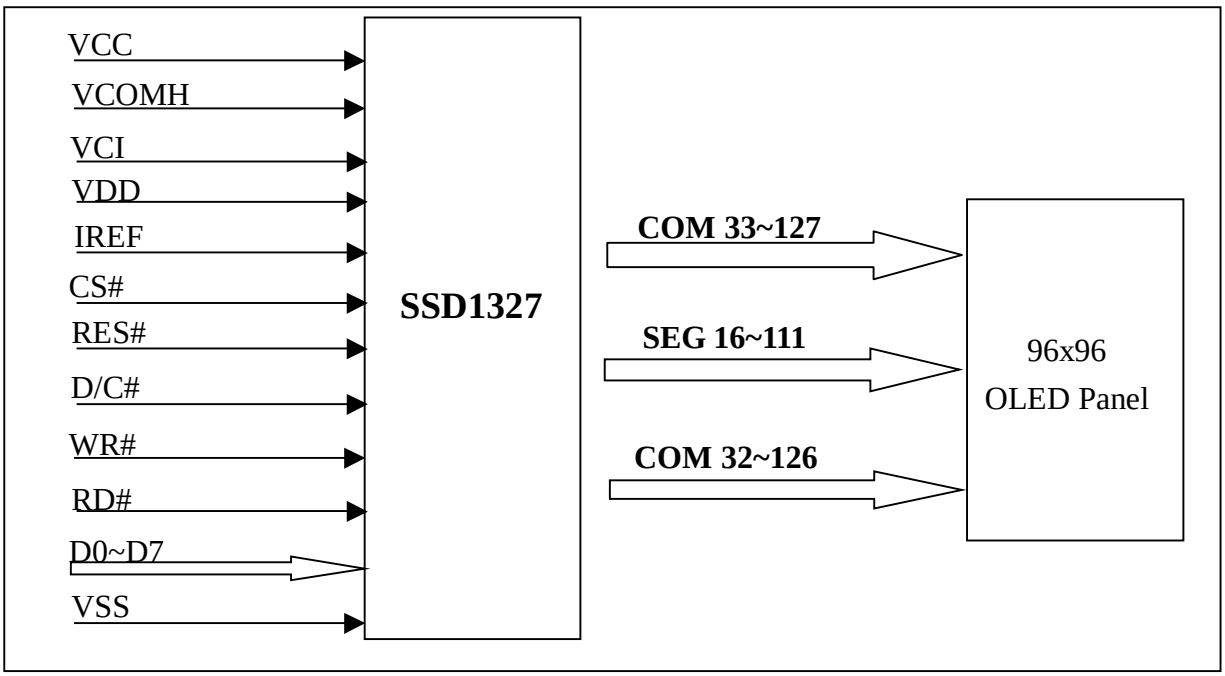
DESCRIPTION

P24001 is a 96X96 dot matrix 16 grayscale OLED module with controller for many compact portable applications.

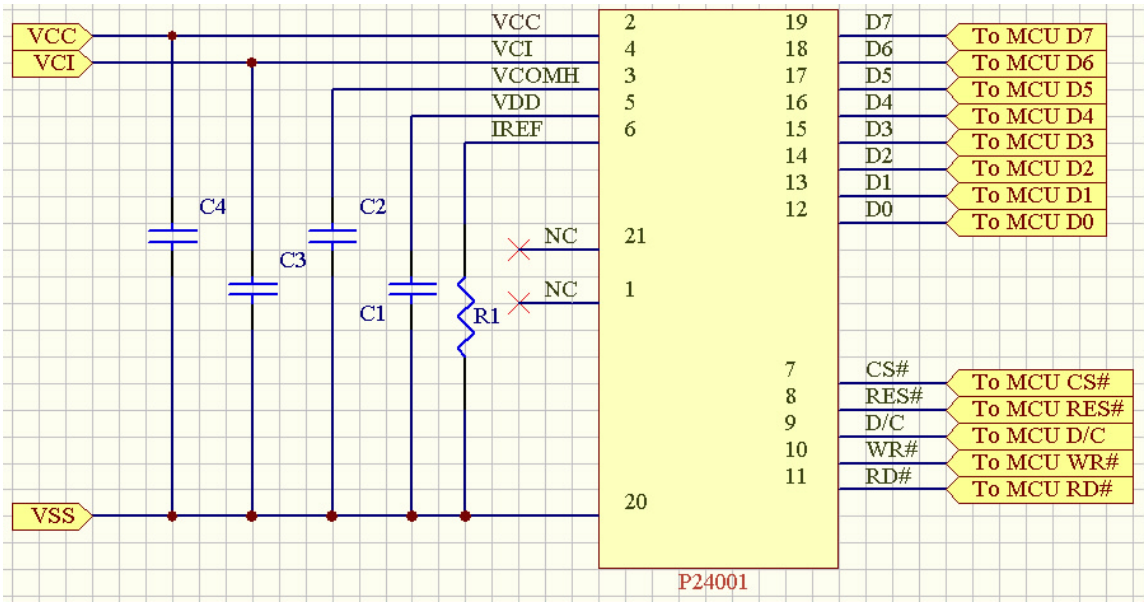
FEATURE

- Panel matrix：96X96.
- Driver IC：SSD1327.
- 16 gray scale.
- High voltage supply：VCC=15V.
- Logic voltage supply：VCI=2.6~3.5V.
- 8-bit 8080-series Parallel Interface.
- Embedded 128x128x4 bit SRAM display buffer.
- Screen saving continuous scrolling function in both horizontal and vertical direction.
- Row Re-mapping and Column Re-mapping
- Programmable Frame Rate and Multiplexing Ratio.

FUNCTION BLOCK DIAGRAM



APPLICATION CIRCUIT



Recommend components：

C1：1uF/16V(0805)

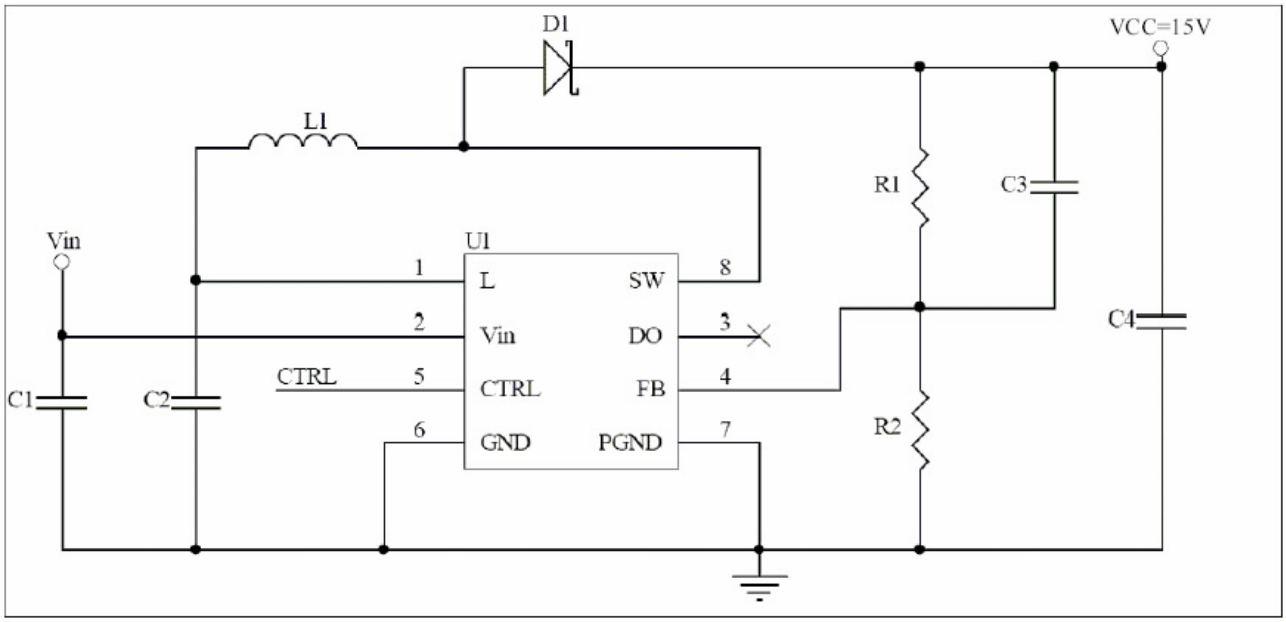
C3：4.7uF/16V(0805)

C2、C4：4.7uF/35V(Tantalum Type)　or　VISHAY(572D475X0025A2T)

R1：1M ohm (0603) 1%

This circuit is for 8080 8bits interface.

EXTERNAL DC-DC APPLICATION CIRCUIT



Recommend components：

The C1：0.1uF/6.3V.

The C2：4.7 uF/6.3V.

The C3：22pF/16V.

The C4：4.7uF/35V Tantalum type capacitor.

The R1：1.27M ohm1%.

The R2：113K ohm1%.

The D1：SCHOTTY diode.

The L1：10uH.

The U1：HPA00483DRBR

The R1, R2 and C3 value should be fine tune by customer.

NOTE：

a. The HPA00483DRBR is low cost DC/DC for TI.

b. The HPA00483DRBR spec. is same as TPS61045.

PIN ASSIGNMENT

Pin Name	Pin No.	Type	Description
NC	1	--	No connection.
VCC	2	I	Power supply for panel driving voltage.
VCOMH	3	O	COM signal deselected voltage level. A capacitor should be connected between this pin and Vss.
VCI	4	I	Voltage power supply for logic.
VDD	5	I	Power supply pin for core logic operation.
IREF	6	I	Reference current input pin. A resistor should be connected between this pin and Vss.
CS#	7	I	This is chip select control pin.
RES#	8	I	Reset signal input. When the pin is pulled LOW, initialization of the chip is executed.
D/C	9	I	This is Data/Command control pin. H：Data input、L：Command input.
WR#	10	I	Data write operation is initiated when this pin is pulled LOW.
RD#	11	I	Read operation is initiated when this pin is pulled LOW.
D0	12	I/O	This pin is bi-direction data signal.
D1	13		
D2	14		
D3	15		
D4	16		
D5	17		
D6	18		
D7	19		
VSS	20	I	Ground.
NC	21	-	No connection.

Application Initial Setting

```
void init_SSD1327 ( void )
{
comm_out ( 0xae ) ; //Set display off
comm_out ( 0xa0 ) ; //Set re-map
comm_out ( 0x42 ) ; //Second byte
comm_out ( 0xa1 ) ; //Set display start line
comm_out ( 0x00 ) ; //Second byte
comm_out ( 0xa2 ) ; //Set display offset
comm_out ( 0x60 ) ; //Second byte
comm_out ( 0xa4 ) ; //Normal Display
comm_out ( 0xa8 ) ; //Set multiplex ratio
comm_out ( 0x5f ) ; //Second byte
comm_out ( 0x81 ) ; //Set contrast
comm_out ( 0x49 ) ; //Second byte
comm_out ( 0xb1 ) ; //Set Phase Length
comm_out ( 0x32 ) ; //Second byte
comm_out ( 0xb3 ) ; //Set Front Clock Divider /Oscillator Frequency
comm_out ( 0x51 ) ; //Second byte
comm_out ( 0xb4 ) ; //For Brightness enhancement
comm_out ( 0xb5 ) ; //Second byte
comm_out ( 0xbc ) ; //Set Pre-charge voltage
comm_out ( 0x07 ) ; //Second byte
comm_out ( 0xbe ) ; //Set VCOMH
comm_out ( 0x07 ) ; //Second byte
comm_out ( 0xaf ) ; //Display on
}
```

After initial the driver IC, user must clear the whole DDRAM.

```
void cleanDDR ( void )
    {
      int i,j ;
      comm_out ( 0x15 ) ; //Set column address
      comm_out ( 0x00 ) ; //Column Start Address
      comm_out ( 0x3f ) ; //Column End Address
      comm_out ( 0x75 ) ; //Set row address
      comm_out ( 0x00 ) ; //Row Start Address
      comm_out ( 0x7f ) ; //Row End Address

      for( i=0 ; i<128 ; i++ )
        {
          for ( j=0 ; j<64 ; j++ )  {  data_out(0x00) ;  }
        }
    }

void show_data ( char a )
    {
      int i,j ;
      comm_out ( 0x15 ) ; //Set column address
      comm_out ( 0x08 ) ; //Column Start Address
      comm_out ( 0x37 ) ; //Column End Address
      comm_out ( 0x75 ) ; //Set row address
      comm_out ( 0x00 ) ; //Row Start Address
      comm_out ( 0x5f ) ; //Row End Address
      for ( i=0 ; i<96 ; i++ )
        {
          for ( j=0 ; j<48 ; j++ )  { data_out(a) ; }
        }
    }
```

Graphic Display Data RAM Address Map

The GDDRAM is a bit mapped static RAM holding the bit pattern to be displayed. The size of the RAM is 128x128x4 bits. For mechanical flexibility, re-mapping on both Segment and Common outputs can be selected by software. The GDDRAM address maps below tables show some examples on using the command "Set Re-map" A0h to re-map the GDDRAM. In the following tables, the lower nibble and higher nibble of D0,D1,D2 … D8189,D8190,D8191 represent the 128x128 data bytes in the GDDRAM.

The GDDRAM map under the following condition：

- Command "Set Re-map" A0h is set to：
  - Disable Column Address Re-map (A [0]=0)
  - Disable Nibble Re-map (A [1]=0)
  - Enable Horizontal Address Increment (A [2]=0)
  - Disable COM Re-map (A [4]=0)
- Display Start Line=00h
- Data byte sequence：D0,D1,D2…D8191

GDDRAM address map 1

		SEG0	SEG1	SEG2	SEG3		SEG124	SEG125	SEG126	SEG127
		00		01			3E		3F	
COM0	00	D0[3:0]	D0[7:4]	D1[3:0]	D1[7:4]		D62[3:0]	D62[7:4]	D63[3:0]	D63[7:4]
COM1	01	D64[3:0]	D64[7:4]	D65[3:0]	D65[7:4]		D126[3:0]	D126[7:4]	D127[3:0]	D127[7:4]
⋮	⋮									
COM126	7E	D8064[3:0]	D8064[7:4]	D8065[3:0]	D8065[7:4]		D8126[3:0]	D8126[7:4]	D8127[3:0]	D8127[7:4]
COM127	7F	D8128[3:0]	D8128[7:4]	D8129[3:0]	D8129[7:4]		D8190[3:0]	D8190[7:4]	D8191[3:0]	D8191[7:4]

SEG Outputs
Column Address (HEX)

COM Outputs
Row Address (HEX)

Nibble re-map A[1]=0

The GDDRAM map under the following condition：

- Command "Set Re-map" A0h is set to：
  - Disable Column Address Re-map (A [0]=0)
  - Disable Nibble Re-map (A [1]=0)
  - Enable Vertical Address Increment (A [2]=1)
  - Disable COM Re-map (A [4]=0)
- Display Start Line=00h
- Data byte sequence：D0, D1, D2 … D8191

GDDRAM address map 2

		SEG0	SEG1	SEG2	SEG3		SEG124	SEG125	SEG126	SEG127	SEG Outputs
		00		01			3E		3F		Column Address
COM0	00	D0[3:0]	D0[7:4]	D128[3:0]	D128[7:4]		D7936[3:0]	D7936[7:4]	D8064[3:0]	D8064[7:4]	(HEX)
COM1	01	D1[3:0]	D1[7:4]	D129[3:0]	D129[7:4]		D7937[3:0]	D7937[7:4]	D8065[3:0]	D8065[7:4]	
|	|									
COM126	7E	D126[3:0]	D126[7:4]	D254[3:0]	D254[7:4]		D8062[3:0]	D8062[7:4]	D8190[3:0]	D8190[7:4]	
COM127	7F	D127[3:0]	D127[7:4]	D255[3:0]	D255[7:4]		D8063[3:0]	D8063[7:4]	D8191[3:0]	D8191[7:4]	

COM Outputs / Row Address (HEX)

(Display Startline=0)

Nibble re-map A[1]=0

The GDDRAM map under the following condition：

- Command “Set Re-map” A0h is set to：
  - Enable Column Address Re-map (A [0]=1)
  - Enable Nibble Re-map (A [1]=1)
  - Enable Horizontal Address Increment (A [2]=0)
  - Disable COM Re-map (A [4]=0)
- Display Start Line=00h
- Data byte sequence：D0,D1,D2…D8191

GDDRAM address map 3

		SEG0	SEG1	SEG2	SEG3		SEG124	SEG125	SEG126	SEG127	SEG Outputs
		3F		3E			01		00		Column Address
COM0	00	D63[7:4]	D63[3:0]	D62[7:4]	D62[3:0]		D1[7:4]	D1[3:0]	D0[7:4]	D0[3:0]	(HEX)
COM1	01	D127[7:4]	D127[3:0]	D126[7:4]	D126[3:0]		D65[7:4]	D65[3:0]	D64[7:4]	D64[3:0]	
|	|									
COM126	7E	D8127[7:4]	D8127[3:0]	D8126[7:4]	D8126[3:0]		D8065[7:4]	D8065[3:0]	D8064[7:4]	D8064[3:0]	
COM127	7F	D8191[7:4]	D8191[3:0]	D8190[7:4]	D8190[3:0]		D8129[7:4]	D8129[3:0]	D8128[7:4]	D8128[3:0]	

COM Outputs / Row Address (HEX)

(Display Startline=0)

Nibble re-map A[1]=1

The example in which the display start line register is set to 10h with the following condition：

- Command “Set Re-map” A0h is set to：
  - Disable Column Address Re-map (A [0]=0)
  - Disable Nibble Re-map (A [1]=0)
  - Enable Horizontal Address Increment (A [2]=0)
  - Enable COM Re-map (A [4]=1)

- Display Start Line=78h (corresponds to COM119)
- Data byte sequence：D0,D1,D2…D8191

GDDRAM address map 4

		SEG0	SEG1	SEG2	SEG3		SEG124	SEG125	SEG126	SEG127
		00		01			3E		3F	
COM119	00	D0[3:0]	D0[7:4]	D1[3:0]	D1[7:4]		D62[3:0]	D62[7:4]	D63[3:0]	D63[7:4]
COM118	01	D1[3:0]	D64[7:4]	D65[3:0]	D65[7:4]		D126[3:0]	D126[7:4]	D127[3:0]	D127[7:4]
⋮	⋮									
COM121	7E	D126[3:0]	D8064[7:4]	D8065[3:0]	D8065[7:4]		D8126[3:0]	D8126[7:4]	D8127[3:0]	D8127[7:4]
COM120	7F	D127[3:0]	D8128[7:4]	D8129[3:0]	D8129[7:4]		D8190[3:0]	D8190[7:4]	D8191[3:0]	D8191[7:4]

SEG Outputs
Column Address
(HEX)

COM Outputs
Row Address (HEX)
(Display Startline=78H)

Nibble re-map A[1]=0

The GDDRAM map under the following condition：

- Command “Set Re-map” A0h is set to：
  - Disable Column Address Re-map (A [0]=0)
  - Disable Nibble Re-map (A [1]=0)
  - Enable Horizontal Address Increment (A [2]=0)
  - Disable COM Re-map (A [4]=0)
- Display Start Line=00h
- Column Start Address=01h
- Column End Address=3Eh
- Row Start Address=01h
- Row End Address=7Eh
- Data byte sequence：D0,D1,D2…D7811

GDDRAM address map 5

		SEG0	SEG1	SEG2	SEG3		SEG124	SEG125	SEG126	SEG127
		00		01			3E		3F	
COM0	00									
COM1	01			D0[3:0]	D0[7:4]		D61[3:0]	D61[7:4]		
⋮	⋮									
COM126	7E			D7750[3:0]	D7750[7:4]		D7811[3:0]	D7811[7:4]		
COM127	7F									

SEG Outputs
Column Address
(HEX)

COM Outputs
Row Address (HEX)
(Display Startline=0)

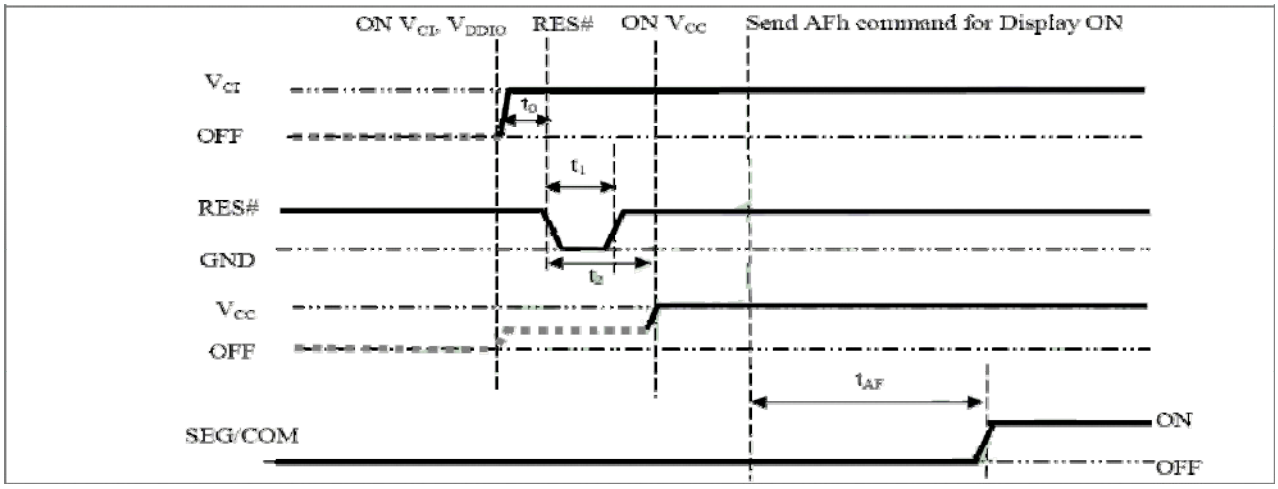
Nibble re-map A[1]=0

Power ON / OFF Sequence

Power ON sequence：

1. Power ON V_{CI}.
2. After V_{CI} becomes stable, set wait time at least 1ms (t_0) for internal V_{DD} become stable. Then set RES# pin LOW (logic low) for at least 100us (t_1) (4) and then HIGH (logic high).
3. After set RES# pin LOW (logic low), wait for at least 100us (t_2). Then Power ON V_{CC}.(1)
4. After V_{CC} become stable, send command AFh for display ON. SEG/COM will be ON after 200ms(t_{AF}).

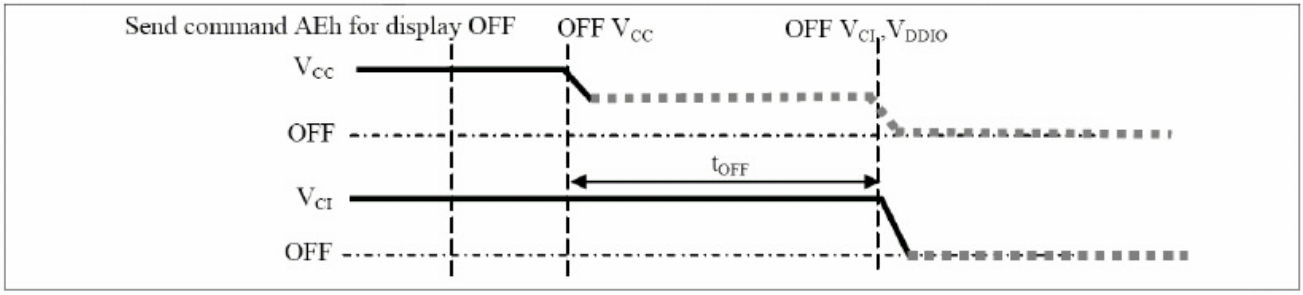
The Power ON sequence.



Power OFF sequence：

1. Send command AEh for display OFF.
2. Power OFF V_{CC}.(1), (2), (3)
3. Wait for t_{OFF}. Power OFF V_{CI}. (Where Minimum t_{OFF}=80ms (5), Typical t_{OFF}=100ms)

The Power OFF sequence



Note：

(1) Since an ESD protection circuit is connected between V_{CI} and V_{CC}, V_{CC} becomes lower than V_{CI} whenever V_{CI} is ON and V_{CC} is OFF as shown in the dotted line of V_{CC} in above figures.

(2) V_{CC} should be kept disable when it is OFF.

(3) Power pins (V_{CI}, V_{CC}) can never be pulled to ground under any circumstance.

(4) The register values are reset after t_1.

(5) V_{CI} should not be Power OFF before V_{CC} Power OFF.

THANK YOU